

A 0.6 μm CMOS bandgap voltage reference circuit

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Abstract: On the basis of mutual compensation of mobility and threshold voltage temperature effects, a stable CMOS band-gap voltage reference circuit was designed and fabricated in CSMC-HJ 0.6 μm CMOS technology. Operating from 0 to 85 °C under a supply voltage ranging from 4.5 to 5.5 V, the voltage reference circuit offers an output reference voltage ranging from 1.122 to 1.176 V and a voltage variation less than ± 3.70%. The chip size including bonding pads is only 0.4 mm × 0.4 mm and the power dissipation falls inside the scope of 28.3 to 48.8 mW operating at a supply voltage of 4.5 to 5.5 V.

Key words: CMOS; mutual compensation; mobility and threshold voltage temperature effects

For the stable operation of such ICs as high-stability voltage sources and low-shifting amplifiers, nearly constant reference voltage should be introduced. As a reference voltage module, its temperature coefficient should be extremely small and the output voltage variation should be ignored approximately over a wide temperature range, typically from 0 to 85 °C, and a large supply voltage variation, for instance ± 10% of supply voltage.

It is well known that there is mutual compensation of mobility and threshold voltage temperature effects in field-effect transistors. The detailed investigation of this compensation resulting in the so-called zero temperature coefficient (ZTC) point in MOS trans-conductance characteristics was done by I.M. Filanovsky and A. Allam^[1]. Recently, it was confirmed that the ZTC point exists for a series of industrial sub-micron CMOS technologies^[2-5]. Therefore, it is possible to realize high-stability reference voltage sources in various CMOS technologies.

In this work, a band-gap reference voltage circuit was realized in CSMC-HJ 0.6 μm CMOS technology. It provides an output reference voltage ranging from 1.122 to 1.176 V, over a temperature range from 0 to 85 °C and a 5 V supply voltage with a ± 10% variation.

1 Circuit Design

At first, we have to identify the ZTC point in the trans-conductance characteristic curves through

V_{DS} -sweeping of the diode-connected transistor MN_1 shown in Fig.1 over the temperature range from − 40 to + 120 °C with a step of 20 °C. As shown in Fig.2, a ZTC point (V_{GSF} , I_{DF}) = (1.099 8 V, 127.6 μA) has been obtained in the NMOS trans-conductance with characteristics of MN_1 with $W/L = 15/1$. A simple band-gap circuit shown in Fig.1 was employed to realize a high-stability reference voltage source. In this circuit, MN_1 is biased at the ZTC point (V_{GSF} , I_{DF}) = (1.099 8 V, 127.6 μA) through choosing appropriate values of R_1 , R_2 and R_3 . These resistors should satisfy the relationships of $I_{D1} = I_{DF} = V_{GS1} R_2/R_1 R_3$ and $V_{REF} = V_{GS1} + I_{D1} R_3 = V_{GSF} + I_{DF} R_3$. Thus, with the increase of temperature, for the decrease of mobility indeed compensates the decrease of the threshold voltage. The output reference voltage is nearly independent of the operating temperature and the fluctuation of supply voltage.

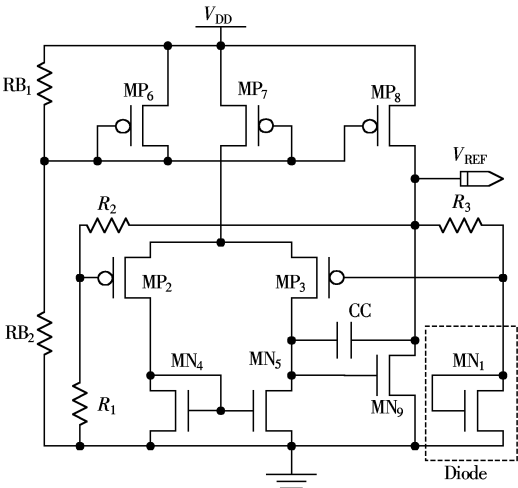


Fig.1 Schematic of voltage reference circuit

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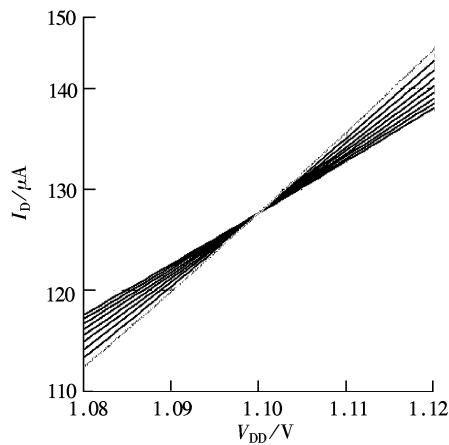


Fig.2 Trans-conductance characteristics of MN₁ near the ZTC point

2 IC Fabrications

The reference voltage source circuit was designed using the 0.6 μm double-poly double-metal N-well CMOS technology and fabricated in CSMC-HJ Semiconductor Co., Ltd, Wuxi, China. The chip microphotograph of the die is shown in Fig.3. The chip size including bonding pads is 0.4 mm × 0.4 mm. On the chip, only four ninths of the total chip area is used for the active part. In fact, the large Miller compensation capacitor used in operational amplifier occupies most of the area of the active part.

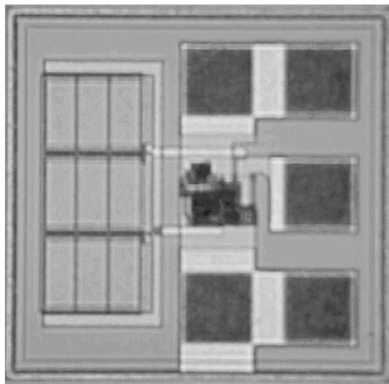


Fig.3 Microphotograph of voltage reference chip

It should be pointed out that the voltage reference chip was firstly realized in mainland China all by native resources such as the Panda system, a layout EDA tool from CIDC (China Integrated Circuit Design Center), the IC foundry of CSMC-HJ Semiconductor Co., Ltd. Wuxi, China. All design kits were developed by IROI (Institute of RF-& OE-ICs), Southeast University and the MPW (multiple project wafer) support of IC fabrication was provided by Shanghai ICC (integrated circuit center).

3 Measurement Results and Discussions

The performance of the packaged reference voltage source circuit shown in Fig.4 was evaluated using an advantest R6142 programmable DC voltage/current generator. The DC current of the reference voltage source circuit operating in a temperature range of 0 to 85 °C is from 5.66 to 9.76 mA with the supply voltage increasing from 4.5 to 5.5 V. An approximately linear dependence between supply current I_{DD} and the supply voltage V_{DD} was obtained. At the same time, the reference voltage increases slowly with the increasing supply voltage and the reference voltage depends lonely a little on the operating temperature, as shown in Fig. 5. The measurement results are summarized in Tab.1 and Tab.2.

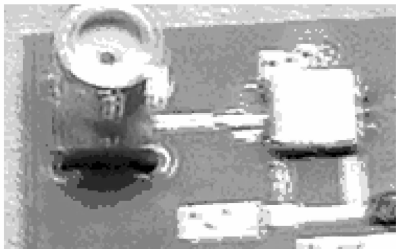


Fig.4 Photograph of the packaged chip

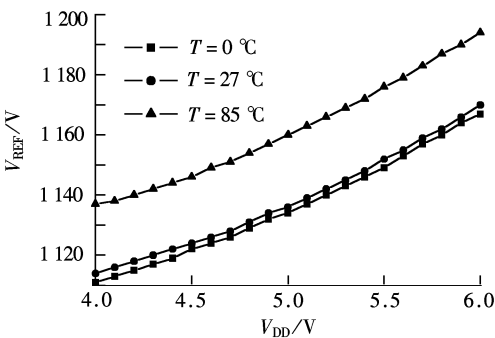


Fig.5 Dependence curve of V_{DD} - V_{REF}

Tab.1 Comparison between simulation performance and testing performance

Item	Output V_{REF} /mV	Range of V_{REF} /mV	Variation ratio of V_{REF}	Power dispersion/mW
Simulation data	1 250	1 248 to 1 251	$< \pm 0.16\%$	24.1 to 40.1
Testing data	1 136	1 122 to 1 176	$< \pm 3.7\%$	28.3 to 48.8

Tab.2 Comparison between simulation data and testing data of polyz resistors

Poly2 resistor	Simulation data/kΩ	Testing data/kΩ	Variation ratio
R_3	1.177	1.214	3.2%
$R_2 + R_3$	2.354	2.302	- 2.2%
$R_1 + R_2 + R_3$	10.973	12.903	17.6%

According to Fig.5 and Tab.1, there is a rather large gap between the testing data and the simulation data using the “TT” corner model parameters supplied by CSMC-HJ. In other words, the function of the mutual compensation of mobility and threshold voltage temperature effects is not as good as it is supposed to be. There are possibly several major sources which induce a rather large deviation of reference voltage. Firstly, the operating point of the MN_1 deviates somewhat from the ZTC point due to the sheet resistance variation of poly-resistors shown in Tab.2, which is inevitable for almost all CMOS technology. Secondly, possible process variation may result in notable changes for such device parameters as effective channel length and threshold voltage given in Tab.3, which can greatly affect the operating point of the MN_1 transistor and other MOS transistors. Thirdly, the operational amplifier employed here perhaps is another victim, which also suffers from possible process fluctuation. Therefore, the power supply rejection ratio and temperature compensation effect will degrade. Lastly, the effects of various non-idealities, including gate resistance, g_m mismatch, g_m variations with temperature, g_m variations with bias current also perhaps contribute some offset to output reference voltage. By the comparison between the testing data in Tab.1 and simulation data in Tab.3, there is a remarkable disparity between the actual process parameters and the parameters listed in “FF”, “FS”, “TT”, “SF” and “SS” corner models employed in our simulations. As a result, the temperature stability of the realized reference voltage circuit suffering from the process fluctuation is necessarily not as perfect as it should be. However, if more accurate model parameters can be employed in circuit simulations and the layout is further optimized, much better performance should be achieved. Even so, this circuit still operates well at 0 to 85 $^{\circ}\text{C}$ under a supply voltage of 4 to 6 V only with a reference voltage variation of 83 mV.

Tab.3 Simulation data with different corner model parameters

Corner models	Range of V_{REF}/mV	Variation ratio of V_{REF}	V_{THN}/V	V_{THP}/V	$L_{\text{EFFN}}/\mu\text{m}$	$L_{\text{EFFP}}/\mu\text{m}$
FF	1 174 to 1 183	Less than $\pm 0.51\%$	0.680	- 0.830	0.40	0.47
FS	1 189 to 1 199	Less than $\pm 0.58\%$	0.700	- 1.100	0.40	0.74
TT	1 248 to 1 251	Less than $\pm 0.16\%$	0.728	- 1.017	0.54	0.60
SF	1 423 to 1 432	Less than $\pm 0.42\%$	0.850	- 0.900	0.67	0.47
SS	1 622 to 1 644	Less than $\pm 0.92\%$	0.990	- 1.230	0.67	0.74

Based on the measurement results and above discussions, we are confident that the realized reference voltage source circuit in CSMC-HJ 0.6 μm CMOS technology can meet the requirement of such import applications as DC bias of amplifier current sources, reference voltage of signal loss detection circuits, D/A conversion circuits, and the like.

4 Conclusion

A band-gap reference voltage source circuit for wide use of D/A conversion circuits, signal loss detection circuits and low-shifting amplifiers are realized using CSMC-HJ 0.6 μm double-poly double-metal N-well CMOS technology. It supplies an output voltage of 1.136 V ($V_{\text{DD}} = 5 \text{ V}$, $T = 27^{\circ}\text{C}$) and a voltage variation less than $\pm 3.70\%$ ($V_{\text{DD}} = 5 \text{ V}$ with a $\pm 10\%$ variation and $T = 0 - 85^{\circ}\text{C}$). According to the measurement results and detailed discussions, we are confident that the realized reference voltage source circuit can meet the requirements of some import applications.

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一种 0.6 μm CMOS 带隙参考电压源

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摘 要 利用 CMOS 晶体管迁移率和阈值电压温度效应相互补偿的原理, 采用 CSMC-HJ 0.6 μm CMOS 技术设计了一种稳定的带隙参考电压源, 该带隙参考电压源可以在 0 ~ 85 $^{\circ}\text{C}$ 、电源电压 4.5 ~ 5.5 V 的范围内正常工作, 输出参考电压为 1.122 ~ 1.176 V, 输出参考电压浮动比例小于 $\pm 3.70\%$. 包括键合用的焊盘在内, 芯片的总面积仅为 0.4 mm \times 0.4 mm, 当电源电压在 4.5 ~ 5.5 V 范围内变化时, 电路总的功率消耗在 28.3 ~ 48.8 mW 之间浮动.

关键词 CMOS; 相互补偿; 迁移率和阈值电压温度效应

中图分类号 TN722