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A low-phase-noise and low-power crystal oscillator for RF tuner

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Abstract: A 37.5 MHz differential complementary metal oxide semiconductor (CMOS) crystal oscillator with low power and low phase noise for the radio frequency tuner of digital radio broadcasting digital radio mondiale (DRM) and digital audio broadcasting (DAB) systems is realized and characterized. The conventional cross-coupled n-type metal oxide semiconductor (NMOS) transistors are replaced by p-type metal oxide semiconductor (PMOS) transistors to decrease the phase noise in the core part of the crystal oscillator. A symmetry structure of the current mirror is adopted to increase the stability of direct current. The amplitude detecting circuit made up of a single-stage CMOS operational transconductance amplifier (OTA) and a simple amplitude detector is used to improve the current accuracy of the output signals. The chip is fabricated in a 0.18-μm CMOS process, and the total chip size is 0.35 mm × 0.3 mm. Under a supply voltage of 1.8 V, the measured power consumption is 3.6 mW including the output buffer for 50 Ω testing loads. The proposed crystal oscillator exhibits a low phase noise of −134.7 dBc/Hz at 1-kHz offset from the center frequency of 37.5 MHz.

Key words: complementary metal oxide semiconductor (CMOS); crystal oscillator; phase noise; power consumption

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With the rapid development of new types of transmission methods, the digital radio mondiale (DRM)[1] and the digital audio broadcasting (DAB)[2] have become the best choices to overcome the weaknesses of the traditional analog radio broadcasting. The DRM covers the frequency range from 148 kHz to 27 MHz, with the latest version DRM + up to 108 MHz. The DAB covers Band Ⅲ (174 to 240 MHz) and Band L (1.452 to 1.492 GHz). Thus, the front-end must operate over a wide frequency range to be compatible with both the DRM and the DAB. Taking account of many factors, an IF of 37.5 MHz is suitable for the proposed dual frequency conversion receiver[3].

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Crystal oscillators are widely used to generate standard reference frequencies in modern electronic systems. It is well known that almost all the crystal oscillators are based on the three-point oscillators, which have many advantages. But in the proposed DRM/DAB tuner chip, all the signals are differential in order to reject the common-mode noise and improve its performance. The differential reference frequency sources are needed by the phase-locked loop providing local oscillates (LO) signals for the tuner. So the three-point oscillators cannot meet the demands and it is very urgent to design differential output crystal oscillators.

This paper presents the design of a low-power and the low-phase-noise CMOS crystal oscillator for DRM/DAB tuners. First, the design of the circuit is described and design considerations are discussed. Then, the realization and the measurement of the crystal oscillators are discussed. Finally, conclusions are given.

1 Circuit Techniques

1.1 Comparison of the three-point and differential crystal oscillator

A conventional crystal oscillator based on Pierce's circuit[4] is shown in Fig. 1. In the circuit, the crystal is the only external component off the chip. The crystal resonator is made up of R_s (series resistor), L_s (series inductor), C_s (series capacitor) and C_p (plate or package capacitances)[5]. The bias is introduced via a current source I_B and a gate biasing voltage V_B via resistor R_b. C_1 and C_2 are two functional loading capacitors. A single biased transistor provides the necessary negative transconductance to overcome the resonator losses. Impedance presented by

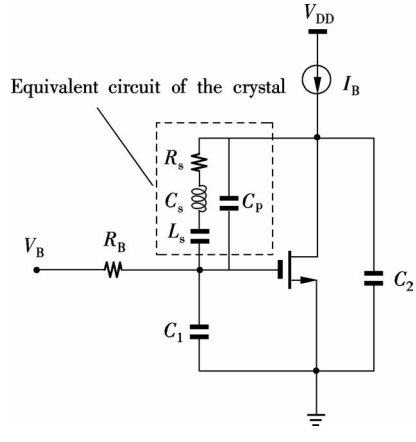

Fig. 1 Conventional crystal oscillator based on Pierce's circuit

this circuit including the static capacitance of the resonator leads to a bilinear function of g_m and a circle in the complex plane which allows the determination of the oscillator critical current, the exact frequency of oscillation, the maximum start-up current and the function between current and frequency. In order to obtain a smaller pulling factor and high stability, large loading capacitors are required, which will increase the oscillator power consumption.

An important parameter of an oscillator is the phase noise in the vicinity of the center frequency f_o. The output phase noise at an offset Δf from f_o can be calculated by[6]

$$L\{\Delta f\} = kT(1 + A) Z_o \frac{1}{Q}\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{V_{rms}^2} \tag{1}$$

where k is the Boltzmann constant; T is the absolute temperature; A is the noise factor to ensure the oscillation start-up; V_{rms} is the root-mean-square voltage at the oscillation node; $Z_0 = (L/C_{total})^{1/2}$ is the characteristic impedance of the crystal resonant tank; and Q is the quality factor. It indicates that maximizing the quality factor of the tank circuit will improve the noise performance considerably.

The equivalent circuit of a differential crystal oscillator is shown in Fig. 2. If the circuit structure of the 3-point Pierce oscillator is duplicated and rendered symmetrically, the differential Pierce oscillator can be obtained. At low frequencies, the impedance of the capacitor C is so large that no oscillation can be built up. At high frequencies, the negative impedance is presented to the crystal. The two sources of the cross-coupled transistors are DC (direct current) separated and capacitively coupled at high frequencies. They yield positive feedback only above a given frequency and are DC stable. Besides the crystal, the oscillation frequency is set by the rail currents, capacitor C and the limiting voltage[7].

It can be obtained from Fig. 2 that

$$R_{eq} = \frac{R_S^2 + (1/(\omega C_S) - \omega L_S)^2}{R_S} \tag{2}$$

$$C_{eq} = C_L + 2C_{DG} + C_P + \frac{1/(\omega C_S) - \omega L_S}{R_S^2 + (1/(\omega C_S) - \omega L_S)^2} \tag{3}$$

$$R_1 = 2R \tag{4}$$

$$C_2 = -\frac{g_m^2 C}{g_m^2 + 4\omega^2 C^2} \tag{5}$$

$$R_2 = -\frac{g_m^2 + 4\omega^2 C^2}{2g_m\omega^2 C^2} \tag{6}$$

where C_{DG} is the equivalent capacitance between two drains and gates of the cross-coupled NMOS transistors and C_L is the loading capacitance. The transconductance of each transistor is g_m. The total transconductance of the active part of the oscillator can be derived by

$$Y_C = -\frac{2g_m\omega^2 C^2}{g_m^2 + 4\omega^2 C^2} + \frac{1}{2R} - j\omega\frac{g_m^2 C}{g_m^2 + 4\omega^2 C^2} \tag{7}$$

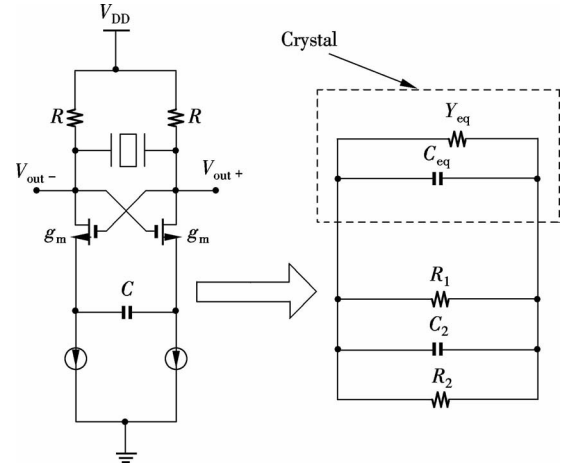

Fig. 2 Equivalent circuit of a conventional differential crystal oscillator

For any given oscillating amplitude, a higher g_m requires a higher biasing current. This requirement leads to a tradeoff between the power consumption and the start-up time. A shorter start-up time requires higher power consumption[8].

1.2 The proposed differential crystal oscillator

The topology of the proposed crystal oscillator is shown in Fig. 3. Compared with the conventional topology shown in Fig. 2, the cross-coupled NMOS transistors are replaced by the PMOS transistors P_1/P_2, which can compensate for the loss of the crystal resonant tank and decrease phase noise. The transistors P_3/P_4, whose gates are connected to two terminals of the crystal, work in the triode region as current followers forcing the current delivered by R_1, R_2 across the cross-coupled transistors. Owing to the symmetry structure and the DC stability, the common-mode voltages at the crystal ports can be kept at the same voltage before an oscillation is built up. There is

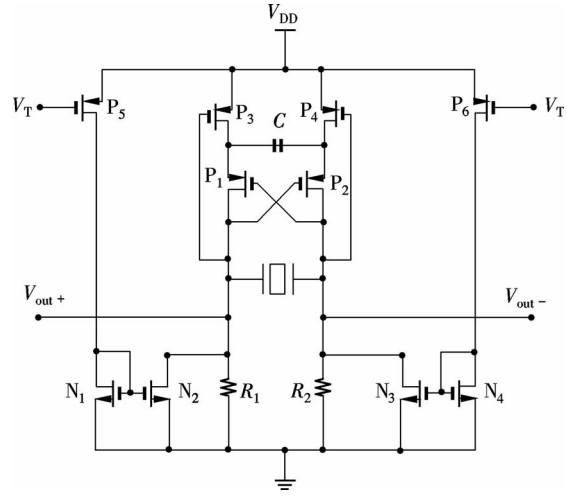

Fig. 3 The proposed differential oscillator circuit

a diode-connected stack of two transistors identical to that of one branch.

N_1/N_2 and N_3/N_4 are two current mirror transistors and their current is defined by transistors P_5 and P_6, respectively. The current flowing through P_5 and P_6 is controlled by the start-up hasten circuit. N_2 and N_3, which provide an additional current path at the beginning of the oscillation building up, are paralleled with biasing resistors R_1 and R_2. As the amplitude of the oscillator grows, the current flowing through N_2 and N_3 begins to decrease until equilibrium is reached or the current drops to zero. By this means, a higher transconductance g_m can be obtained when the oscillation is built up, and a lower transconductance g_m can be obtained after the oscillation is built up[9].

As shown in Fig. 3, the additional current flowing through N_2 and N_3 is controlled by V_T (the gate voltage of P_5 and P_6). V_T is generated by the amplitude detecting circuit shown in Fig. 4. It consists of a single-stage CMOS OTA (operational transconductance amplifier) and a simple amplitude detector. The OTA simultaneously provides a high enough input impedance and a suitable gain. As the amplitude of the oscillation grows, the output voltage grows accordingly. This effect is exacerbated by the non-linearity of N_3. The transistor is operated in the sub-threshold region. Thus, the current increases obviously while the gate voltage increases. Meanwhile, the current drops slightly as the gate voltage drops. Then, the average current increases with an AC input.

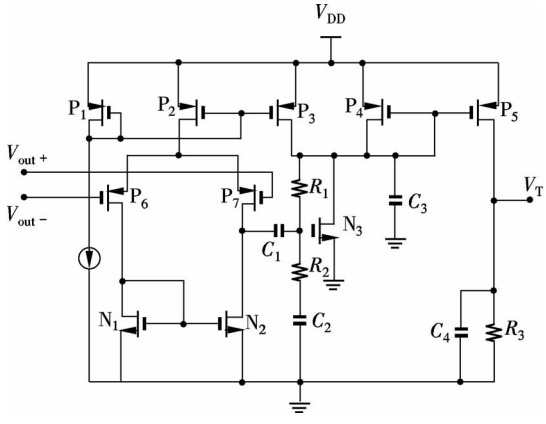

Fig. 4 The proposed amplitude detection circuit

The RLC model of the off-chip crystal was measured from hundreds of quartzes. The measurement was done by the manufacturer of the AT-cut crystal. The average values of these parameters are shown in Tab. 1.

Tab. 1 Average values of crystal's RLC model

Component parameter	R_S/Ω	L_S/mH	C_S/fF	C_P/pF
Average value	8.436	1.097	16.477	4.447

2 Experimental Results

The oscillator is implemented in a 0.18-μm CMOS process with a 1.8-V power supply. The chip microphotograph is shown in Fig. 5. The chip area is about 0.35 mm × 0.3 mm.

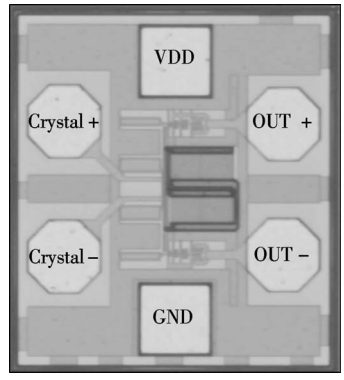

Fig. 5 Chip microphotograph of the crystal oscillator

The test PCB bonded with the oscillator chip is shown in Fig. 6. The off-chip components such as the crystal, SMA-type microwave connectors and so on are welded onto the PCB. The output signals are measured by a signal source spectrum analyzer.

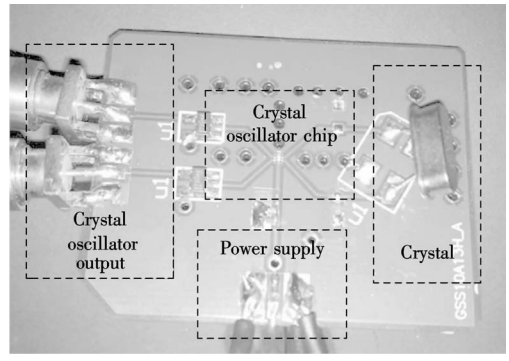

Fig. 6 Photograph of the test PCB

The voltage of the power supply for the measurement is 1.8 V. The chip draws a current of 2 mA from the power supply, 0.2 mA for the oscillator core, and 1.8 mA for the output buffers. The output buffer is used to drive the 50-Ω load of the measurement equipment.

The measured phase noise of the oscillator output signal at 37.5 MHz is shown in Fig. 7. It can be seen that the phase noise is –134.7 dBc/Hz at 1 kHz off the center frequency. The range of the power supply of the chip is as wide as 1.2 to 2.5 V. The phase noise changes only less than 1 dB at the same time.

The performance of the proposed circuit is summarized in Tab. 2 with several recently published works for comparison.

Tab. 2 Performance comparison with other published works

Paper	Technology	f_{osc}/MHz	Power supply/V	Phase noise at 1-kHz offset
Ref. [10]	3-μm SiGe	20.5	5	–110 dBc/Hz
Ref. [11]	0.35-μm SiGe	12.8	2.7	–134 dBc/Hz
This paper	0.18-μm CMOS	37.5	1.8	–134.7 dBc/Hz

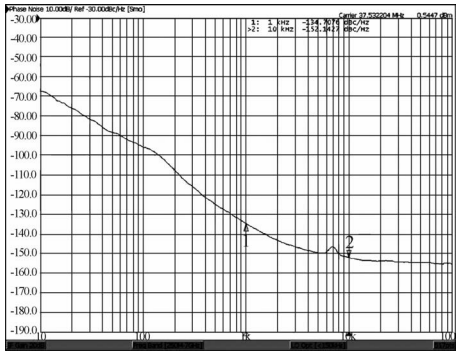

Fig. 7 Measured phase noise of the oscillator's output signal

3 Conclusion

A low power differential crystal oscillator circuit realized in a 0.18-μm CMOS process is proposed in this paper. Several new circuit techniques are adopted to improve its performance. In the core part of the crystal oscillator, the conventional cross-coupled NMOS transistors are replaced by PMOS transistors to decrease the phase noise. A symmetry structure of the current mirror is adopted to increase the DC stability. Furthermore, the amplitude detecting circuit made up of a single-stage CMOS OTA and a simple amplitude detector is used to improve the current accuracy of the output signals. The measured results show that the center frequency of the crystal oscillator is 37.5 MHz and the phase noise is −134.7 dBc/Hz at 1 kHz offset off the center frequency. The experimental results provide the feasibility of the technology in the design of a low-phase-noise and low-power CMOS crystal oscillator for the RF tuner.

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一种用于射频调谐器的低相位噪声低功耗晶体振荡器

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摘要: 实现了一种基于 CMOS 工艺的用于 DRM 与 DAB 数字广播射频调谐器的具有低相位噪声与低功耗的工作在 37.5 MHz 的差分结构晶体振荡器. 在晶体振荡器的核心部分采用了 PMOS 晶体管来代替传统的 NMOS 晶体管以降低相位噪声. 采用了对称结构的电流镜以提高直流稳定度. 采用了由一阶 CMOS 运算跨导放大器和简单的幅度探测器构成的幅度探测电路以提高输出信号的电流精确度. 芯片采用 0.18-μm CMOS 工艺实现,芯片面积为 0.35 mm × 0.3 mm. 芯片包含用于驱动 50 Ω 测试的负载接口电路,在 1.8 V 供电电压下,所测得的芯片功耗仅为 3.6 mW. 晶体振荡器的工作输出信号在距离其中心频率 37.5 MHz 频偏 1 kHz 处的相位噪声为 −134.7 dBc/Hz.

关键词: CMOS;晶体振荡器;相位噪声;功耗

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