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A 12 Gbit/s limiting amplifier using 2 μm GaAs HBT technology for fiber-optic transmission system

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Abstract: A 12 Gbit/s limiting amplifier for fiber-optic transmission system is realized in a 2 μm GaAs HBT technology. The whole circuit consists of an input buffer, three similar amplifier cells, an output buffer for driving 50 Ω transmission lines and a pair of feedback networks for offset cancellation. At a positive supply voltage of 2 V and a negative supply voltage of − 2V, the power dissipation is about 280 mW. The small-signal gain is higher than 46 dB and the input dynamic range is about 40 dB with a constant single-ended output voltage swing of 400 mV. Satisfactory eye-diagrams are obtained at the bit rate of 12 Gbit/s limited by the test set-up. The chip area is 1.15 mm × 0.7 mm.

Key words: optical receiver; limiting amplifier; GaAs HBT technology

High-speed limiting amplifiers are widely used in fiber-optic transmission systems, radar systems, and satellite communication systems, etc. In optic-fiber links, a limiting amplifier has several possible applications. First, it can be used as the main amplifier of the optical receiver. Secondly, it can be used in the clock recovery circuit with a passive filter to restrain amplitude variation of the clock signal detected from the input data. Thirdly, it can be used as input or output buffer for data and clock signal reshaping[1]. To satisfy the requirements of various applications, a limiting amplifier must provide an output eye-diagram that is independent of the input data amplitude ranging from millivolts to about one volt. The design of a high-speed limiting amplifier with high gain and a wide input dynamic range therefore plays an important role in the realization of high-speed data systems. In this paper, the design and realization of a 12 Gbit/s limiting amplifier in a 2 μm GaAs HBT technology is presented.

1 Circuit Design

The main amplifier is one of the key circuits in an optical receiver. Its task is to amplify the output signal from the low noise pre-amplifier to a constant level, to satisfy the requirement of the subsequent data decision and clock recovery circuit. Besides high-speed and high-gain, another important specification of the main amplifier is a wide input dynamic range, i.e. the output amplitude must be independent of the input amplitude over a wide dynamic range. As one of the realization forms of the main amplifier, the limiting amplifier has the following advantages: ease of design, lower power dissipation, smaller chip size and fewer external components[2].

Fig.1 shows the block diagram of the limiting amplifier we realized. The whole circuit consists of an input buffer, three similar amplifier cells, an output buffer for driving 50 Ω transmission lines and a pair of feedback networks for offset cancellation. The whole circuit is DC-coupled, fully differential and fully balanced. The non-linearity of ECL-like current amplifiers is used for the limiting function.

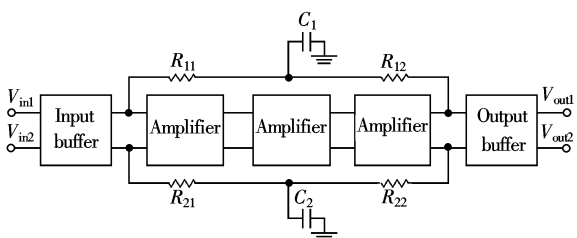

Fig.1 Block diagram of the limiting amplifier

For systems applications, chips are connected with 50 Ω transmission lines to eliminate loss of power induced by signal reflection. The input buffer provides the function of impedance matching to 50 Ω transmission lines at the input terminal, to reduce reflection of the incident wave and increase the transmission efficiency. Besides, it provides a suitable DC level for internal circuit. The input buffer is realized with a pair of emitter followers.

The output buffer provides PCML output level, and provides the function of impedance matching to

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50 Ω transmission lines at the output terminal. The output buffer is realized with an emitter-coupled transistor pair.

The gain of each amplifier cell should be large enough, so that even with small input amplitude the last amplifier cell can enter the limiting region, thereby increasing the input dynamic range of the limiting amplifier. Besides, the bandwidth of the amplifier should be large enough, so that it can operate at the specified bit rate. As shown in Fig.2, a differential structure is used to realize the basic amplifier cell of the limiting amplifier, so that the circuit becomes less sensitive to variation of temperature and supply voltage. In addition, the differential form can restrain interference better under conditions of broad-band and high-gain. To achieve broad-band and low-noise, resistors are used as loads. Q_1 and Q_2 form the main amplifying transistor pair with R_{C1} and R_{C2} as loads on them. R_{ref}, Q_5 and Q_6 form a basic mirror current source to provide current for Q_1 and Q_2. Q_3, Q_4, R_{E3}, and R_{E4} form a pair of emitter followers to provide the function of level shifting and impedance conversion.

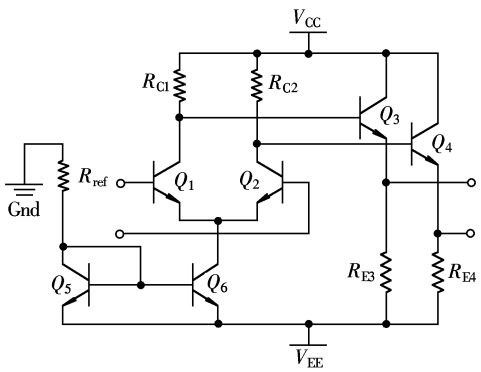

Fig.2 Basic amplifier cell

Since each stage of the limiting amplifier is DC-coupled and the limiting amplifier has a very high gain, a very small DC offset voltage caused by devices and layout mismatches can be amplified to such a large level that the following stages up to the output buffer go into saturation, making the output signal clipped. The resistors R_{11}, R_{12}, R_{21}, R_{22} and the capacitances C_1, C_2 in Fig.1 form an offset cancelling circuit to reduce the influence of mismatches.

2 Fabrication

At present, circuits for optical communication systems working at the bit rate of 2.5 – 10 Gbit/s are mostly realized with III-V compounds, including GaAs-based and InP-based metal semiconductor field effect transistors (MESFET), high electron mobility transistors (HEMT) and Heterojunction bipolar transistors (HBT). HBTs are among the most attractive devices for use in high-speed circuitry. High saturation velocity and high mobility in III-V compounds result in short carrier transit times. In HBTs, wide bandgap emitters allow a variety of device improvement. Base doping in HBTs is much higher than that in Si bipolar transistors, and this serves to lower the base resistance; the greater injection efficiency provided by the heterojunction also allows the emitter doping to be lowered, which reduces the base-emitter capacitance. The shielding of the base-emitter junction by the heavily doped base results in a low output conductance[3]. Since HBTs possess the additional advantages of lower base resistance, lower emitter junction capacitance, higher injection efficiency, higher transconductance and drive capacity, we select 2 μm GaAs HBT technology to realize the limiting amplifier; the transit frequency f_T of it is lower than 40 GHz. The resistors are made from thin NiCr film with sheet resistance of 50 Ω per square. And only two metal layers are used to interconnect.

The chip has been fabricated through a foundry technology in Taiwan; the chip microphotograph is shown in Fig.3; the chip area is 1.15 mm × 0.7 mm.

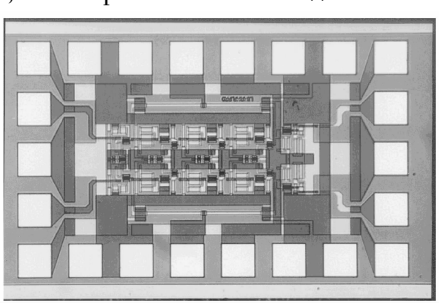

Fig.3 Chip microphotograph of the limiting amplifier

3 Experimental Result

The fabricated circuits have been measured on-wafers using RF probes. The test set-up is shown in Fig.4.

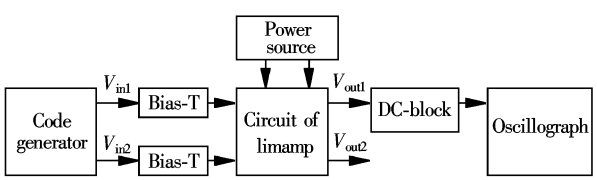

Fig.4 Test set-up of the limiting amplifier

According to the design scheme, the chip is powered by double supply sources. The positive supply voltage is 2 V, and the negative is – 2 V. The DC

power dissipation is about 280 mW.

Data signals with different input voltages and at different bit rates are applied to the circuit, so that the input dynamic range is obtained. Fig.5 shows the measured eye-diagrams of one single-ended output signal of the limiting amplifier, with an input voltage swing of 10 mV and 1 V. The voltage swing at each single-ended output is 400 mV.

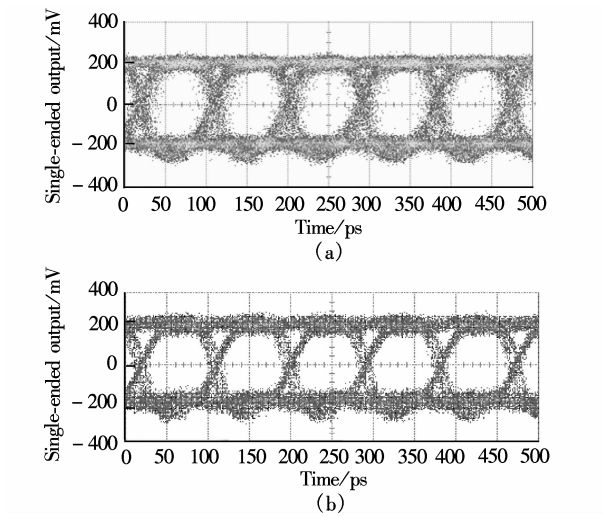

Fig.5 12Gbit/s eye-diagrams of single-ended output. (a) Input:10 mV, output:400 mV; (b) Input:1 V, output:400 mV

Based on these measured results, we are confident that a limiting amplifier designed by using 2 μm GaAs HBT technology can operate at a bit rate higher than 12 Gbit/s, and the input dynamic range would be about 40 dB.

4 Conclusion

A 12 Gbit/s limiting amplifier for fiber-optic transmission system has been realized by using 2 μm GaAs HBT technology. The limiting amplifier has a gain higher than 46 dB and a dynamic range of 40 dB. The limited single-ended output voltage swing is 400 mV. At a positive supply voltage of 2 V and a negative supply voltage of – 2 V, the power dissipation is about 280 mW. The highest data speed of 12 Gbit/s is reached.

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12 Gbit/s 用于光纤传输系统的 GaAs HBT 限幅放大器

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摘 要 用 2 μm GaAs HBT 工艺实现了 12 Gbit/s 用于光纤传输系统的限幅放大器.整个系统包括一级输入缓冲、三级放大、一级用于驱动 50 Ω 传输线的输出缓冲和失调电压补偿回路 4 个部分.采用双电源供电,正电源为 2 V,负电源为 – 2 V,功耗为 280 mW.小信号增益大于 46 dB,输入信号比特率为 12 Gbit/s 时,在输出电压幅度保持恒定(单端峰峰值 400 mV)的条件下,输入动态范围约为 40 dB,眼图性能良好.芯片面积为 1.15 mm × 0.7 mm.

关键词 光接收机; 限幅放大器; GaAs HBT 工艺

中图分类号 TN492