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Design considerations for the improved current-doubler-rectifier ZVS PWM full-bridge converter

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Abstract: The improved current-doubler-rectifier zero-voltage-switching PWM full-bridge converter (CDR ZVS PWM FB converter) achieves ZVS for the switches in a wide load range with the use of the energy stored in the output filter inductances, and the rectifier diodes commute naturally, therefore no oscillation and voltage spike occurs. The transformer needs no special manufacture method to limit the leakage inductance. The ZVS achievement and the design considerations for the output filter inductances and the blocking capacitor are discussed for the improved CDR ZVS PWM FB converter. A 540 W prototype converter is built in the lab to verify the operational principle and design considerations for the improved converter, the experimental results are also included.

Key words: full-bridge converter; zero-voltage-switching; pulse-width-modulation; current-doubler-rectifier

Full-bridge (FB) DC/DC converter is widely used in medium-to-high power application. In the past twenty years, a variety of soft-switching FB converters were proposed. Phase-shifted zero-voltage-switching (ZVS) PWM FB converters[1,2] and phase-shifted zero-voltage and zero-current-switching (ZVZCS) PWM FB converters[3,4] realize soft-switching for the switches. Phase-shifted ZVS PWM FB converters utilize the leakage inductance and the output capacitors of the power switches to realize ZVS for the switches[1,2]. However, the lagging leg is very difficult to realize ZVS because only the energy stored in the leakage inductance is used. In order to realize ZVS for the lagging leg in a wide load range, we can increase the leakage inductance or introduce a resonant inductance in series with the primary winding of the transformer. But duty cycle loss occurs in the process. The issue of the reverse recovery of the rectifier diodes still exists in phase-shifted ZVS and ZVZCS PWM FB converters, which results in oscillation and voltage spike on the rectifier diodes. In order to depress the oscillation, several active or passive clamp circuits were proposed, but these circuits need large clamp capacitors, which result in large current spikes in the switches[5-7].

CDR ZVS PWM full-bridge converter[8] realizes ZVS for the switches in a wide load range with the use of the energy stored in the two output filter inductances, and the rectifier diodes commute naturally, thus the oscillation is eliminated. However, the primary current should decay rapidly during the zero state, and it is only the conduction voltage drop of the switches that forces the primary current to decay. The conduction voltage drop is too small, so the leakage inductance should be very small, which requires special manufacturing method to produce the transformer.

An improved CDR ZVS PWM FB converter, which keeps all the advantages of the original counterpart, was proposed in Ref.[9]. Based on the original CDR ZVS PWM FB converter, a blocking capacitor C_b is introduced in series with the primary winding. The voltage of the blocking capacitor, which is considerably larger than the conduction voltage drop of the switches, is used to force the primary current to decay rapidly even when the leakage inductance is relatively large, therefore there is no special limit to the leakage inductance.

The paper focuses on design considerations for the improved CDR ZVS PWM FB converter. The realization and optimums of the performances are ensured by the elaborate design of the key parameters: ① The output filter inductance; ② The blocking capacitor.

1 Features of ZVS Achievement for the Switches

The improved CDR ZVS PWM FB converter is shown in Fig.1(a). In Fig.1(a), Q_1 to Q_4 are the power switches, D_1 to D_4 are body diodes of Q_1 to Q_4. C_1 to C_4 are the intrinsic capacitors of Q_1 to Q_4, L_{lk} is the leakage inductance of the transformer, D_{R1} and D_{R2}

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are the rectifier diodes, L_{f1} and L_{f2} are the output filter inductance, C_f is the output filter capacitor, R_{Ld} is the load. The converter employs the phase-shifted modulation strategy. Q_1 and Q_3 form the leading leg, and Q_4 and Q_2 form the lagging leg.

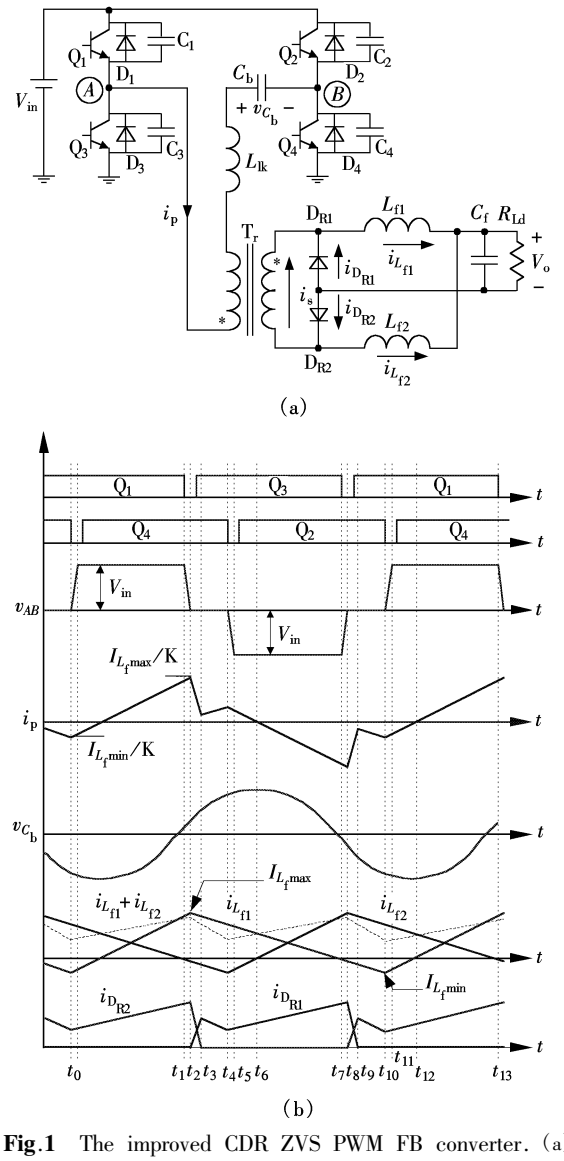

Fig.1 The improved CDR ZVS PWM FB converter. (a) Main circuit; (b) Key waveforms

From the operation principle of the improved CDR ZVS PWM FB converter, we can know that the leading leg realizes ZVS using the energy stored in the output filter inductance when the current of output filter inductance reaches its maximum value $I_{L_{f\max}}$, e.g., at t_1 or t_7; and the lagging leg realizes ZVS using the energy stored in the output filter inductance when the current of output filter inductance reaches its minimum value $I_{L_{f\min}}$, e.g., at t_4 or t_{10}, see Fig.1(b). Please note that $I_{L_{f\min}}$ is a negative value.

$I_{L_{f\max}}$ and $I_{L_{f\min}}$ can be obtained as

$$I_{L_{f\max}} = \frac{I_o}{2} + \frac{V_o(2-D)T_s}{4L_f} \tag{1}$$

$$I_{L_{f\min}} = \frac{I_o}{2} - \frac{V_o(2-D)T_s}{4L_f} \tag{2}$$

where T_s is the switching period; D is the duty cycle of the converter represented by $D = \dfrac{2(t_1 - t_0)}{T_s}$.

From (1) and (2), we can know that ① the larger the output current is, the larger $I_{L_{f\max}}$ is, and the smaller $|I_{L_{f\min}}|$ is, so the leading leg is easier to realize ZVS at heavy loads than at light loads, the lagging leg is easier to realize ZVS at light loads than at heavy loads; and ② because $I_{L_{f\max}} > |I_{L_{f\min}}|$, the leading leg is easier to realize ZVS than the lagging leg if the intrinsic capacitors of the switches of the leading leg and the lagging leg are equal. So the worst case is to achieve ZVS for the lagging leg at full load. The design considerations should be set out from this point.

2 Design Considerations

This section discusses the design of the converter, especially the design of the output filter inductance and the blocking capacitor.

The specifications of the prototype converter are:

- DC input voltage: $V_{in} = (250 \pm 20\%)$V;
- DC output voltage: $V_o = 54$ V;
- Output current: $I_o = 10$ A;
- Switching frequency: $f_s = 100$ kHz;
- Leakage inductance measured at the switching frequency $L_{lk} = 0.46\,\mu$H.

2.1 Determination of *K*

The relationship between the output voltage and the input voltage for the CDR FB converter in continuous current mode (CCM) is

$$K = \frac{DV_{in}}{2V_o} \tag{3}$$

here CCM means that the sum of the two filter inductance currents is greater than zero, i.e., $i_{L_{f1}} + i_{L_{f2}} > 0$ when $v_{AB} = 0$ as shown in Fig.1(b).

Let $D_{max} = 0.8$ at the lowest input voltage, then $K = 1.48$. We choose $K = 1.5$.

2.2 Output filter inductance

As a filter inductance, it is better to be large enough to reduce its current ripple. However in order to realize ZVS for the lagging switches at full load, it should be quite small so that the filter inductance current can flow in the negative direction. So we

should determine the maximum value of the filter inductance to ensure ZVS for the lagging switches at full load.

From mode $[t_4, t_5]$, when the lagging switch turns off, the time for the voltage of C_2 to decrease to zero is $t_{4,5}$.

$$t_{4,5} = \frac{2C_{\text{lag}}V_{\text{in}}}{I_{\text{p}}(t_4)} = \frac{2C_{\text{lag}}V_{\text{in}}}{-\frac{I_{L_{\text{f}}\min}}{K}} \tag{4}$$

As I_{o} increases, $|I_{L_{\text{f}}\min}|$ decreases, $t_{4,5}$ increases. From (2), (3) and (4), L_{fmax} can be derived as

$$L_{\text{fmax}} = \frac{t_{4,5}V_{\text{o}}(V_{\text{in}} - KV_{\text{o}})}{4KC_{\text{lag}}V_{\text{in}}^2 f_{\text{s}} + t_{4,5}V_{\text{in}}I_{\text{omax}}f_{\text{s}}} \tag{5}$$

Eq.(5) illustrates that L_{f} is determined by V_{in} and $t_{4,5}$. In order to reduce the turn-off loss of the lagging switches at light load, a tradeoff is needed. We choose $t_{4,5} = 7t_{\text{f}}$ at full load, where t_{f} is the turn-off time of the lagging switch. Here IRF450 (from IXYS corporation) is selected as the power switch with $C_{\text{oss}}(= C_{\text{lag}}) = 300$ pF and $t_{\text{f}} = 44$ ns.

Once $t_{4,5}$ is determined, then L_{f} is determined by V_{in}. Fig.2 shows the plot of L_{fmax} versus the input voltage, from which we choose $L_{\text{f}} = 28\ \mu$H.

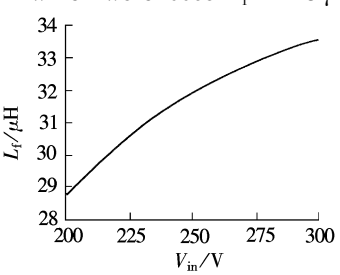

Fig.2 The maximum filter inductance under different input voltages

As the filter inductance is determined, we can calculate $I_{L_{\text{f}}\max}$ and $I_{L_{\text{f}}\min}$. When the improved converter operates in CCM, $I_{L_{\text{f}}\max}$ and $I_{L_{\text{f}}\min}$ can be derived from (1), (2) and (3).

$$I_{L_{\text{f}}\max\_\text{CCM}} = \frac{I_{\text{o}}}{2} + \frac{V_{\text{o}}(V_{\text{in}} - KV_{\text{o}})T_{\text{s}}}{2V_{\text{in}}L_{\text{f}}} \tag{6}$$

$$I_{L_{\text{f}}\min\_\text{CCM}} = \frac{I_{\text{o}}}{2} - \frac{V_{\text{o}}(V_{\text{in}} - KV_{\text{o}})T_{\text{s}}}{2V_{\text{in}}L_{\text{f}}} \tag{7}$$

When the load becomes light, the improved converter will operate in discontinuing current mode (DCM), where the sum of the two filter inductance currents reduces to zero when $v_{AB} = 0$, the load is supplied by the filter capacitor, which is shown in Fig.3. $I_{L_{\text{f}}\max}$ and $I_{L_{\text{f}}\min}$ in DCM are given in (8) and (9) respectively and are derived in the appendix.

$$I_{L_{\text{f}}\min\_\text{DCM}} = -\sqrt{\frac{V_{\text{in}}T_{\text{s}}V_{\text{o}}I_{\text{o}}}{8L_{\text{f}}(V_{\text{in}} - 2KV_{\text{o}})}} \tag{8}$$

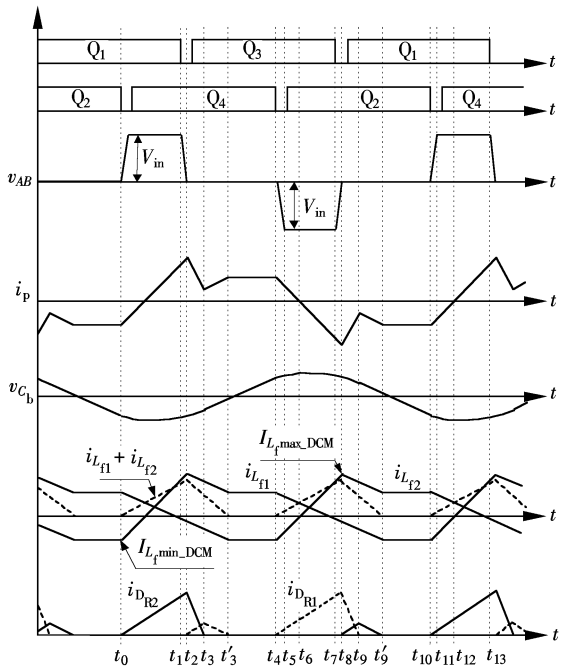

Fig.3 Key waveforms in DCM

$$I_{L_{\text{f}}\max\_\text{DCM}} = \left(3 - \frac{4KV_{\text{o}}}{V_{\text{in}}}\right)\sqrt{\frac{V_{\text{in}}T_{\text{s}}V_{\text{o}}I_{\text{o}}}{8L_f(V_{\text{in}} - 2KV_{\text{o}})}} \tag{9}$$

The critical output current between CCM and DCM is I_{G}, which is given in (10) and is derived in appendix.

$$I_{\text{G}} = \frac{V_{\text{o}}(V_{\text{in}} - 2KV_{\text{o}})T_{\text{s}}}{2L_{\text{f}}V_{\text{in}}} \tag{10}$$

Fig.4 gives the $I_{L_{\text{f}}\max}$ and $-I_{L_{\text{f}}\min}$ at different load currents under the minimum, nominal and maximum input voltages. There is an inflexion in each curve, the corresponding current of the inflexion is the critical output current. On the left of the inflexion, the converter operates in DCM, and on the right of the inflexion, the converter operates in CCM. Fig.4 illustrates that once we determine the value of filter inductance according to (5), the lagging leg realizes ZVS not only at the worst case in CCM but also at nearly open load in DCM. So both the leading leg and the lagging leg can realize ZVS from nearly open load to full load under the input voltage range.

2.3 Blocking capacitor

The blocking capacitor C_{b} is used to force the primary current to decay rapidly when $v_{AB} = 0$, and it ensures that the rectifier diodes commute naturally, no oscillation and voltage spike on the rectifier diodes occur. From this point, C_{b} should be as small as possible, but a small C_{b} results in high peak voltage of C_{b} and increases the voltage stress of the rectifier diodes. So C_{b} should be large enough, which is just to

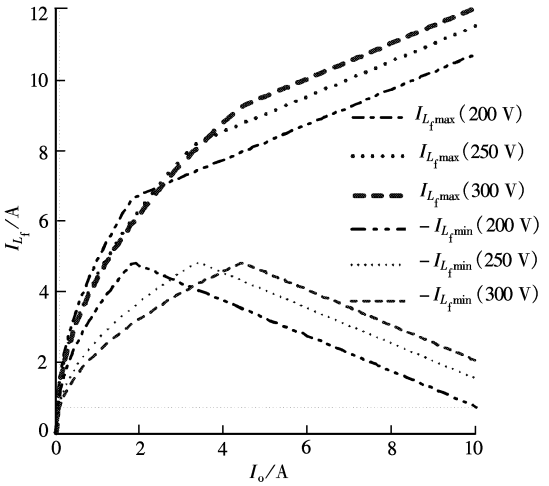

Fig.4 $I_{L_{f\max}}$ and $I_{L_{f\min}}$ at different load currents under the minimum, nominal and maximum input voltages

ensure the commutation of the two rectifier diodes.

As shown in Fig.1(b), the rectifier diodes finish commutation at t_3. The worst case is that $t_3 = t_4$, in which i_p reduces to $-I_{L_{f\min}}/K$, i.e.,

$$I_p(t_4) = \frac{-I_{L_{f\min}}}{K} \tag{11}$$

During $[t_2, t_3]$, v_{AB} is fully applied to L_{lk}, C_b resonates with L_{lk}.

$$i_p(t) = -\frac{V_{C_b}(t_2)}{\omega L_{lk}}\sin\omega(t-t_2) + I_p(t_2)\cos\omega(t-t_2) \tag{12}$$

$$v_{C_b}(t) = \omega L_{lk} I_p(t_2)\sin\omega(t-t_2) + V_{C_b}(t_2)\cos\omega(t-t_2) \tag{13}$$

where $\omega = \dfrac{1}{\sqrt{L_{lk}C_b}}$;

$$I_p(t_2) = I_{L_{f\max}}/K \tag{14}$$

Substituting (11) and (14) into (12), we can obtain

$$I_p(t_4) = -\frac{V_{C_b}(t_2)}{\omega L_{lk}}\sin\omega(t_4-t_2) + \frac{I_{L_{f\max}}}{K}\cos\omega(t_4-t_2) \leqslant -\frac{I_{L_{f\min}}}{K} \tag{15}$$

Inequality (15) is the condition for the rectifier diodes to finish commutation at t_4, it is related with $V_{C_b}(t_2)$.

During $[t_0, t_2]$,

$$i_p(t) = \frac{1}{K}\left[I_{L_{f\min}} + \frac{\frac{V_{in}}{K} - V_o}{L_f}(t-t_0)\right] \tag{16}$$

At t_2,

$$V_{C_b}(t_2) = V_{C_b}(t_0) + \frac{1}{C_b}\int_{t_0}^{t_2} i_p(t)\,dt = V_{C_b}(t_0) + \frac{1}{C_b}\frac{I_o}{2K}(t_2-t_0) = V_{C_b}(t_0) + \frac{I_o DT_s}{4KC_b} \tag{17}$$

From (13), we can obtain

$$V_{C_b}(t_4) = \omega L_{lk} I_p(t_2)\sin\omega(t_4-t_2) + V_{C_b}(t_2)\cos\omega(t_4-t_2) \tag{18}$$

It can be seen in Fig.1(b) that

$$V_{C_b}(t_4) = -V_{C_b}(t_0) \tag{19}$$

From (17), (18) and (19), $V_{C_b}(t_2)$ is derived as

$$V_{C_b}(t_2) = \frac{\frac{I_o DT_s}{4KC_b} - \omega L_{lk} I_p(t_2)\sin\omega(t_4-t_2)}{1+\cos\omega(t_4-t_2)} \tag{20}$$

where $t_4 - t_2 = [(1-D)T_s]/2$.

From (1), (2), (14), (15) and (20), we can obtain

$$y(C_b, V_{in}) = \frac{DT_s}{\sqrt{L_{lk}C_b}}\tan\frac{t_4-t_2}{2\sqrt{L_{lk}C_b}} - 4 \geqslant 0 \tag{21}$$

From (21), we can know that ① The design of C_b is not related with output current I_o; ② When the converter operates under the same condition else, the relationship between C_b and L_{lk} is

$$L_{lk}C_b = \text{const} \tag{22}$$

From (22), we can obtain that $L_{lk}C_b$ should be kept constant in order to ensure that when the rectifier diodes commute naturally. Therefore, we can adjust the design of C_b according to (22) under different leakage inductances of the transformer. And (22) proves that there is no special limit to the leakage inductances, the conventional transformer can be employed.

Fig.5 shows the plot of the left side of inequality (21) versus C_b under different input voltages, it illustrates that in order to satisfy (21), C_b should be smaller than 2.3 μF at the lowest input voltage V_{inmin} = 200 V. That is because at the lowest input voltage, the

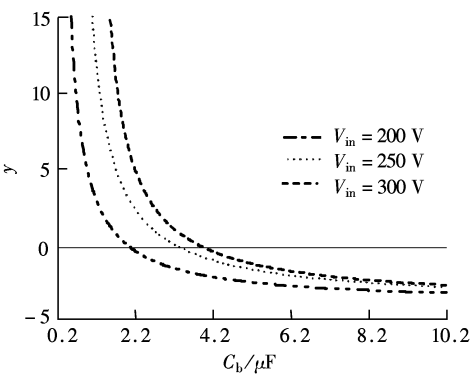

Fig.5 The plot of the left side of inequality (21) versus C_b under different input voltages

duty cycle is maximum, the time for i_p to decay is the shortest. We choose $C_b = 1.5\ \mu F$.

3 Experimental Results

A 540 W output power (54 V, 10 A) prototype converter is built in the lab to verify the operation principle of the improved CDR ZVS PWM FB converter and the parameter design. The parameters of the converter are: $V_{in} = 250$ V; Q_1 (D_1 and C_1) to Q_4 (D_4 and C_4): IRF450; D_{R1} and D_{R2}: DSEI12-06A; $K = 1.5$; $L_{lk} = 0.46\ \mu H$; $C_b = 1.5\ \mu F$; $L_{f1} = L_{f2} = 28\ \mu H$; $C_f = 6\,600\ \mu F$; switching frequency $f_s = 100$ kHz.

Fig.6 shows the experimental results at full load. Fig.6(a) gives v_{AB}, the primary current i_p, the blocking capacitor voltage v_{C_b} and the current of the two filter inductances $i_{L_{f1}}$ and $i_{L_{f2}}$, which illustrates that when $v_{AB} = 0$, v_{C_b} forces i_p to decay rapidly to make the rectifier diodes commute naturally. Fig.6(b) shows the voltage of the rectifier diode $v_{D_{R1}}$ and the rectifier diode currents $i_{D_{R1}}$ and $i_{D_{R2}}$, from which we can see that there is no oscillation and voltage spike on the rectifier diodes. Fig.6(c) and (d) shows the gate drive signal and its voltage across the drain and source of the leading switch and lagging switch respectively, which illustrate that both the leading switch and the lagging switch realize ZVS.

Fig.7 and Fig.8 show the experimental results at half load (5 A) and light load (1 A). From Fig.6 to Fig.8, we know that the switches can realize ZVS in a wide load range, and the oscillation caused by the reverse recovery of the rectifier diodes is eliminated.

Fig.9(a) shows the conversion efficiency at different load currents under the nominal input voltage. The efficiency is 92.4% at full load.

Fig.9(b) shows the efficiency at full load under different input voltages, which illustrates the efficiency decreases when the input voltage increases. This is because there is idle current during zero state (when $v_{AB} = 0$), which results in conduction loss in the switches and the primary winding. The higher the input voltage is, the longer zero state is, thus the higher conduction loss is, and the lower the efficiency is.

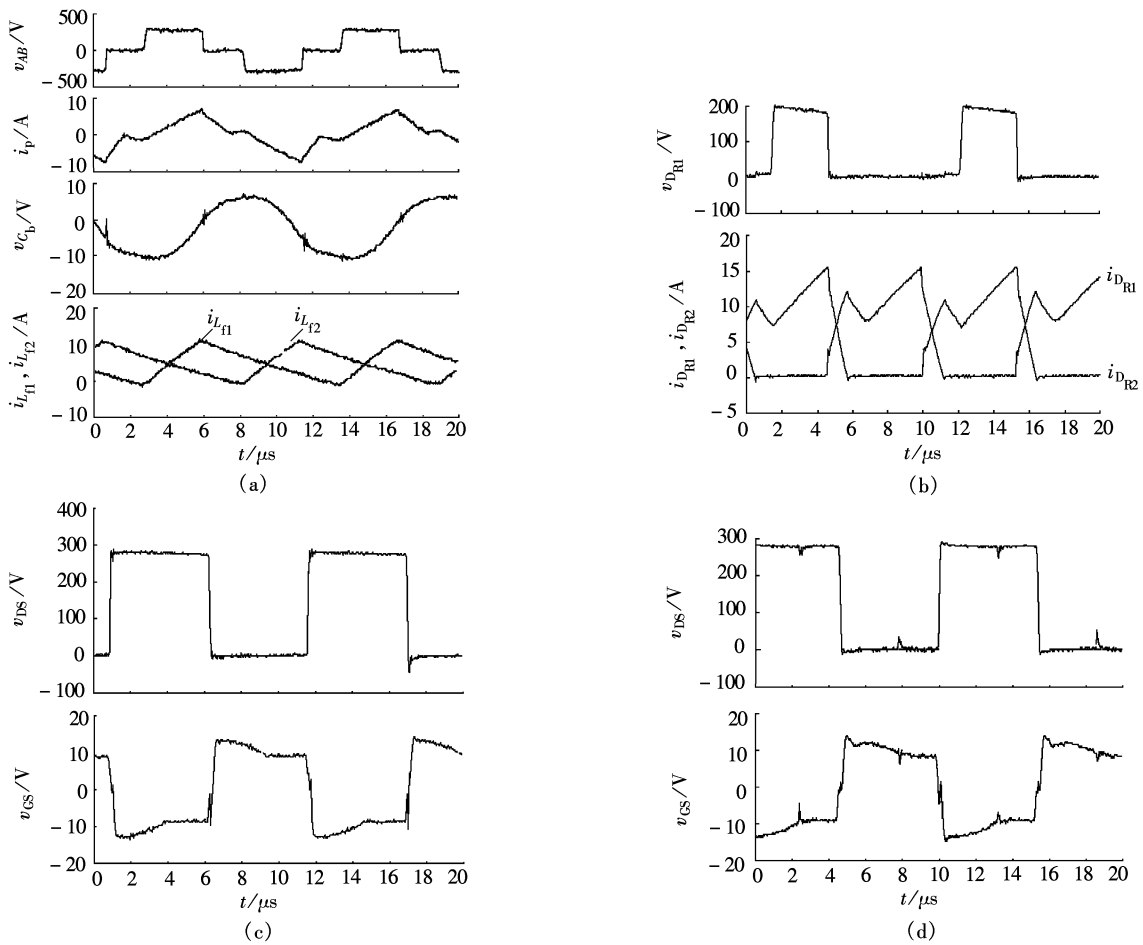

Fig.6 Experimental results at full load (10 A). (a) v_{AB}, i_p, v_{C_b}, $i_{L_{f1}}$ and $i_{L_{f2}}$; (b) $v_{D_{R1}}$, $i_{D_{R1}}$ and $i_{D_{R2}}$; (c) v_{DS} and v_{GS} of Q_3; (d) v_{DS} and v_{GS} of Q_4

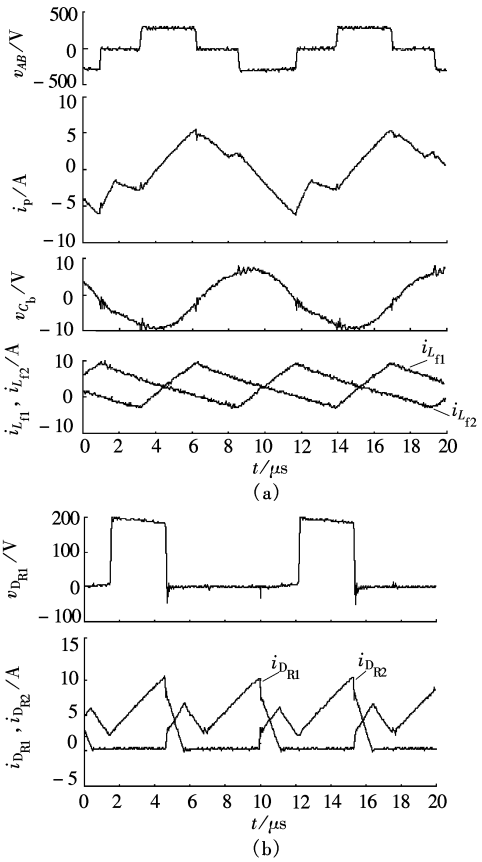

Fig.7 Experimental results at half load (5 A). (a) v_{AB}, i_p, v_{C_b}, $i_{L_{f1}}$ and $i_{L_{f2}}$; (b) $v_{D_{R1}}$, $i_{D_{R1}}$ and $i_{D_{R2}}$

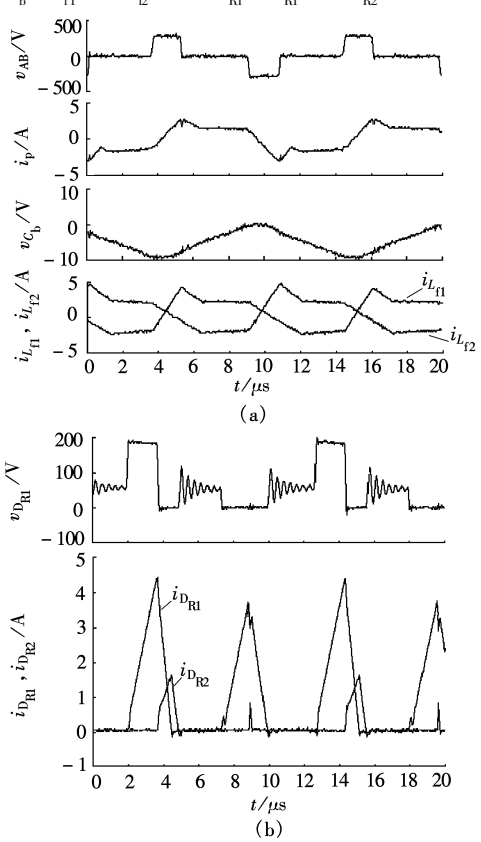

Fig.8 Experimental results at light load (1 A). (a) v_{AB}, i_p, v_{C_b}, $i_{L_{f1}}$ and $i_{L_{f2}}$; (b) $v_{D_{R1}}$, $i_{D_{R1}}$ and $i_{D_{R2}}$

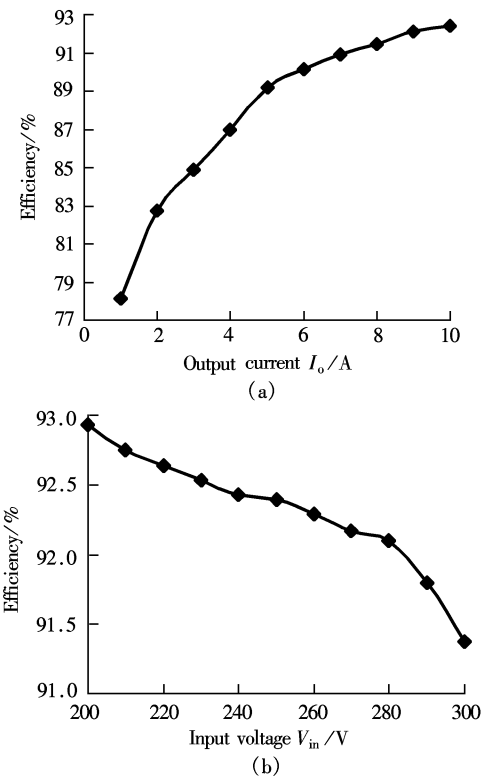

Fig.9 Conversion efficiency of the improved CDR ZVS PWM FB converter. (a) Conversion efficiency at different load currents under the nominal voltage; (b) Conversion efficiency at full load under different input voltages

4 Conclusions

This paper gives the features of the ZVS achievement for the switches and the design of the filter inductance and the blocking capacitor in details for the improved CDR ZVS PWM FB converter. The improved converter keeps all the advantages of the original counterpart:

1) The switches realize ZVS in a wide load range with the use of the energy stored in the filter inductances.

2) The rectifier diodes commute naturally without oscillation and voltage spike. Furthermore, the introduced blocking capacitor forces the primary current to decay rapidly without the restricted limit to the leakage inductance. A 540 W prototype converter verifies the principle of the improved converter and the parameter design. The experimental results are also presented.

Appendix

This appendix is provided to derive ① $I_{L_f\text{min\_DCM}}$ and $I_{L_f\text{max\_DCM}}$, the maximum value and minimum value of the filter inductance current when the CDR ZVS PWM FB converter is operating in DCM, and ② I_G, the critical output current at the DCM boundary.

When the output current decreases, the sum of the two filter inductance currents will reduce to zero when $v_{AB} = 0$, the load is supplied by the output filter capacitor. At this time CDR ZVS PWM FB converter operates in DCM. The key waveforms are shown in Fig.3.

During $[t_0, t_2]$, $i_{L_{f1}}$ increases linearly from $I_{L_{f}min\_DCM}$, and $i_{L_{f2}}$ decreases linearly from $-I_{L_{f}min\_DCM}$.

$$i_{L_{f1}}(t) = I_{L_{f}min\_DCM} + \frac{\frac{V_{in}}{K} - V_o}{L_f}(t - t_0) \quad (A1)$$

$$i_{L_{f2}}(t) = -I_{L_{f}min\_DCM} - \frac{V_o}{L_f}(t - t_0) \quad (A2)$$

At t_2, the sum of the two filter inductance currents is

$$I_{L_{f1}}(t_2) + I_{L_{f2}}(t_2) = \frac{\frac{V_{in}}{K} - 2V_o}{L_f}(t_2 - t_0) \quad (A3)$$

$i_{L_{f1}}$ increase to $I_{L_{f}max\_DCM}$

$$I_{L_{f1}}(t_2) = I_{L_{f}max\_DCM} = I_{L_{f}min\_DCM} + \frac{\frac{V_{in}}{K} - V_o}{L_f(t_2 - t_0)} \quad (A4)$$

where

$$t_2 - t_0 = DT_s/2 \quad (A5)$$

During $[t_2, t_3']$, $i_{L_{f1}}$ and $i_{L_{f2}}$ decreases linearly,

$$i_{L_{f1}}(t) = I_{L_{f1}}(t_2) - \frac{V_o}{L_f}(t - t_2) \quad (A6)$$

$$i_{L_{f2}}(t) = I_{L_{f2}}(t_2) - \frac{V_o}{L_f}(t - t_2) \quad (A7)$$

$$i_{L_{f1}}(t) + i_{L_{f2}}(t) = I_{L_{f1}}(t_2) + I_{L_{f2}}(t_2) - \frac{2V_o}{L_f}(t - t_2) \quad (A8)$$

At t_3', $i_{L_{f1}} = -I_{L_{f}min\_DCM}$, $i_{L_{f2}} = I_{L_{f}min\_DCM}$ and $i_{L_{f1}} + i_{L_{f2}} = 0$, so

$$t_3' - t_2 = \frac{L_f[I_{L_{f1}}(t_2) + I_{L_{f2}}(t_2)]}{2V_o} \quad (A9)$$

$$I_{L_{f2}}(t_3') = I_{L_{f}min\_DCM} = I_{L_{f2}}(t_2) - \frac{V_o}{L_f}(t - t_2) =$$

$$-I_{L_{f}min\_DCM} - \frac{V_o}{L_f}[(t_2 - t_0) + (t_3' - t_2)] \quad (A10)$$

Substituting (A3) and (A5) into (A9), yields

$$t_3' - t_2 = \frac{\frac{V_{in}}{K} - 2V_o}{4V_o}DT_s \quad (A11)$$

From (A5), (A10) and (A11), we can obtain

$$I_{L_{f}min\_DCM} = -\frac{V_{in}DT_s}{8KL_f} \quad (A12)$$

Substituting (A5) and (A12) into (A4), yields

$$I_{L_{f}max\_DCM} = \frac{3V_{in} - 4KV_o}{8KL_f}DT_s \quad (A13)$$

The output current is the average value of the sum of the two filter inductance currents, i.e.,

$$I_o = \overline{i_{L_{f1}} + i_{L_{f2}}} = \frac{[I_{L_{f1}}(t_2) + I_{L_{f2}}(t_2)][(t_3' - t_2) + (t_2 - t_0)]}{T_s} \quad (A14)$$

From (A3), (A5), (A11) and (A14), the duty cycle in DCM is derived as

$$D = \sqrt{\frac{8V_oI_oL_f}{\left(\frac{V_{in}^2}{K^2} - \frac{2V_{in}V_o}{K}\right)T_s}} \quad (A15)$$

Substituting (A15) into (A12) and (A13) respectively, yields

$$I_{L_{f}min\_DCM} = -\sqrt{\frac{V_{in}T_sV_oI_o}{8L_f(V_{in} - 2KV_o)}} \quad (A16)$$

$$I_{L_{f}max\_DCM} = \left(3 - \frac{4KV_o}{V_{in}}\right)\sqrt{\frac{V_{in}T_sV_oI_o}{8L_f(V_{in} - 2KV_o)}} \quad (A17)$$

If $t_3' = t_4$, then the converter operates within DCM boundaries, $t_3' - t_0 = \frac{T_s}{2}$, and $K = \frac{DV_{in}}{2V_o}$, so the critical output current I_G can be derived from (3), (A3), (A5) and (A14),

$$I_G = \frac{V_o(V_{in} - 2KV_o)T_s}{2L_fV_{in}} \quad (A18)$$

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改进型倍流整流方式 ZVS PWM 全桥变换器的设计

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摘　要　针对改进型倍流整流电路零电压开关 PWM 全桥变换器(CDR ZVS PWM FB 变换器),讨论了超前管和滞后管各自实现 ZVS 的特点,对滤波电感的电感值和阻断电容的电容值进行了优化选择,使变换器在很宽的负载和输入电压范围内实现开关管的 ZVS,输出整流二极管实现自然换流,没有电压尖峰,同时对变压器的漏感没有严格要求.通过一个 540 W 的原理样机验证改进型变换器的工作原理和设计的正确性,最后给出了实验结果.

关键词　全桥变换器; 零电压开关; 脉宽调制; 倍流整流电路

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