A resistorless CMOS bandgap reference with below 1 V output

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Abstract: This paper proposes a resistorless CMOS bandgap reference (BGR) circuit capable of generating a voltage less than 1V and presents a high performance start-up circuit that can make the BGR circuit achieve the correct operation point at power on. The simulation with Hspice was carried out using a 0.25 μm CMOS process. The results indicate that the proposed BGR circuit can operate on a 2.2 to 3.3 V power supply and its output voltage has a variation of 11 mV at – 10 to 80 ℃.

Key words: bandgap reference; start-up circuit; CMOS; low voltage

Reference voltage generators with low sensitivity to the temperature and supply are commonly required both in analog and digital circuits. Since the conventional implementation of the bandgap reference (BGR) provides an output voltage almost equal to the silicon energy gap, measured in electron volts, it limits its application to those applications where below 1 V reference voltage is needed. A recently reported current-mode realization of the BGR in the CMOS process[1] can produce a reference voltage less than 1 V, however, its output voltage is adjusted by the ratio of the resistors. The presence of resistors is a drawback for some applications. In a standard digital CMOS process, the resistivity is not guaranteed by some foundries and can vary with the process. Also, in a digital process, the area of such resistors is increased because silicide is often used to reduce the sheet resistance of the polysilicon and diffusion layers. The BGR described in Ref.[2] gave a good solution to the above problems: a bandgap reference without resistors. However its output voltage was about 1.2 V. In this paper, a resistorless CMOS BGR circuit capable of generating a voltage less than 1 V is presented and a new start-up circuit is discussed.

1 Known BGR Circuit

In the conventional BGR circuit, the output voltage is the sum of the built-in voltage of the diode and the thermal voltage multiplied by a constant factor. Fig.1 shows the schematic of BGR without resistors based on this principle[2].

Since resistors are not used, the required constant factor is obtained by using radioed transistors together with the inverse function technique[3]. Here, the

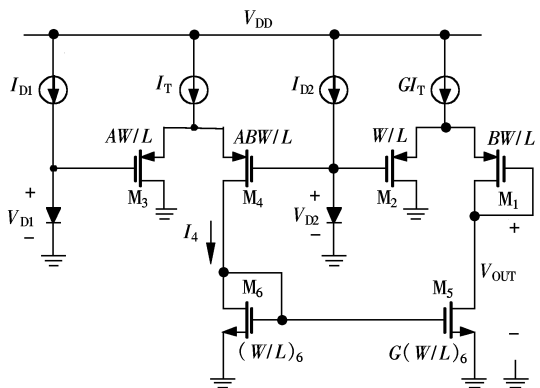

Fig.1 Schematic of the core of the resistorless bandgap reference

proportional to absolute temperature (PTAT) voltage $\Delta V_D = V_{D2} - V_{D1}$ is applied across the differential pair M_3-M_4, the resulting current is multiplied by G using current mirror M_6-M_5 and is delivered to the differential pair M_1-M_2. It is assumed that all the MOS transistors work in strong inversion; we can get the following expressions:

$$\Delta V_D = V_{GS3} - V_{GS4} = \sqrt{\frac{2}{k'SA}}\left(\sqrt{I_T - I_4} - \sqrt{\frac{I_4}{B}}\right) \quad (1)$$

$$V_{GS2} - V_{GS1} = \sqrt{\frac{2G}{k'S}}\left(\sqrt{I_T - I_4} - \sqrt{\frac{I_4}{B}}\right) \quad (2)$$

where $k' = \mu C_{ox}$, μ is the mobility of carrier, C_{ox} is the gate oxide capacitance per unit area; S is the W/L ratio. It follows from (1), (2) and Fig.1 that

$$V_{OUT} = V_{D2} + \sqrt{AG}\Delta V_D \quad (3)$$

where $\Delta V_D = V_T \ln \frac{I_{D2}}{I_{D1}}$; V_T is the thermal voltage. Here V_{D2} has a negative temperature coefficient of – 2 mV/℃, whereas V_T has a positive temperature coefficient of 0.086 mV/℃. Thus in order to get a voltage with low sensitivity to the temperature, the V_{OUT} must be about 1.2 V.

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2 Proposed BGR Circuit

The concept of the proposed BGR is to let two voltages, V_{D2} and ΔV_D, have the same constant factor. Fig.2 shows the schematic of the core of the resistorless BGR with below 1 V output. All the MOS transistors work in strong inversion. From Fig.2, we can obtain

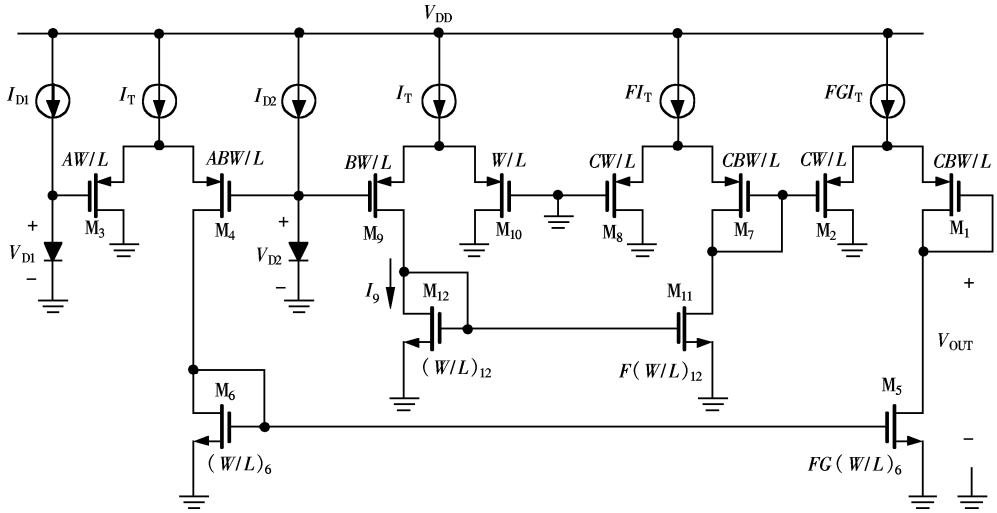

Fig.2 Schematic of the core of the resistorless BGR with below 1 V output

$$V_{D2} = V_{GS10} - V_{GS9} = \sqrt{\frac{2}{k'S}}\left(\sqrt{I_T - I_9} - \sqrt{\frac{I_9}{B}}\right) \quad (4)$$

$$V_{GS8} - V_{GS7} = \sqrt{\frac{2G}{k'SC}}\left(\sqrt{I_T - I_9} - \sqrt{\frac{I_9}{B}}\right) \quad (5)$$

It follows from (4) and (5) that

$$V_{GS8} - V_{GS7} = \sqrt{\frac{F}{C}}V_{D2} \quad (6)$$

According to the same method, we can get

$$V_{GS2} - V_{GS1} = \sqrt{\frac{AGF}{C}}\Delta V_D \quad (7)$$

Since the output voltage is the sum of $V_{GS2} - V_{GS1}$ and $V_{GS8} - V_{GS7}$,

$$V_{OUT} = \sqrt{\frac{F}{C}}(V_{D2} + \sqrt{AG}\Delta V_D) \quad (8)$$

If the ratio F/C is chosen reasonably, the less than 1 V output voltage can be obtained. Fig.3 shows the complete circuit. Here, the PNP transistors, which can be easily fabricated by CMOS process, replace the diodes in Fig.2. Q_1 consists of n unit transistors in parallel, and Q_2 is a unit transistor. M_{b1}-M_{b7} act as a bias circuit that is a previously published circuit[4]. M_{s1}-M_{s3} constitutes the start-up circuit which forces the BGR to its correct operational point at power on and at the steady state, it is disconnected from the BGR, as if it does not exist. Now the output voltage can be expressed as

$$V_{OUT} = \sqrt{\frac{F}{C}}[V_{BE2} + V_T\sqrt{AG}\ln(mn)] \quad (9)$$

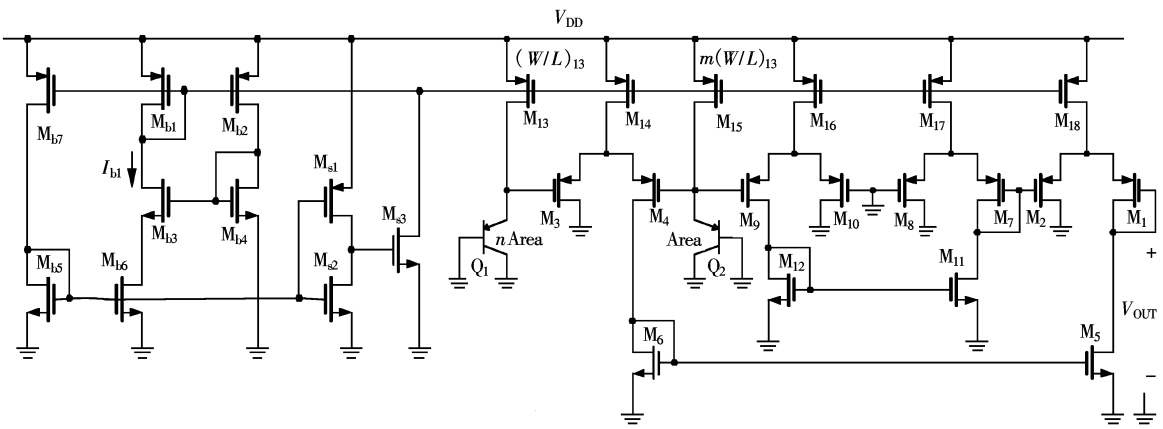

Fig.3 Complete schematic

3 Simulation Results

A simulation has been carried out using a 0.25 μm CMOS process of which the threshold voltage is 0.6 V for NMOS and − 0.8 V for PMOS. Tab.1 shows the sizes of all MOS transistors in Fig.3 and n is chosen as

8. The output voltage is sensitive to the threshold voltage mismatch of the differential pairs and the current mirrors so that the gate area of these transistors should be chosen a bit larger.

Tab.1 Device sizes μm

Device	W	L	Device	W	L	Device	W	L
M_{b1}	15	15	M_1	96	5	M_{11}	2	20
M_{b2}	15	15	M_2	24	5	M_{12}	2	20
M_{b3}	20	5	M_3	36	5	M_{13}	15	15
M_{b4}	20	5	M_4	144	5	M_{14}	75	15
M_{b5}	2	50	M_5	10	20	M_{15}	60	15
M_{b6}	9	50	M_6	2	20	M_{16}	75	15
M_{b7}	15	15	M_7	96	5	M_{17}	75	15
M_{s1}	2	20	M_8	24	5	M_{18}	375	15
M_{s2}	20	2	M_9	24	5			
M_{s3}	2	50	M_{10}	6	5			

Fig.4 presents the start transient of I_{b1} when V_{DD} = 2.5 V. Fig.5 shows the output voltage of the proposed BGR circuit as a function of temperature with a 2.5 V power supply. We observe that a variation of 11 mV at −10 to 80 ℃. Fig.6 demonstrates that the output voltage is varied with changes in the power supply. A better power supply rejection ratio would require the addition of a cascode stage or the increase of the channel length of the MOS transistors. The simulation indicates this circuit dissipates 0.3 mW power at 2.5 V power supply voltage.

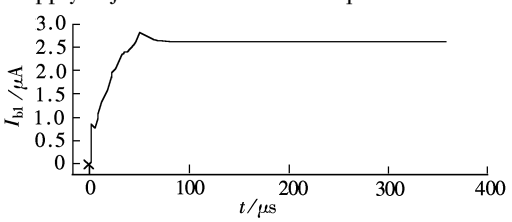

Fig.4 I_{b1} start transient (V_{DD} = 2.5 V)

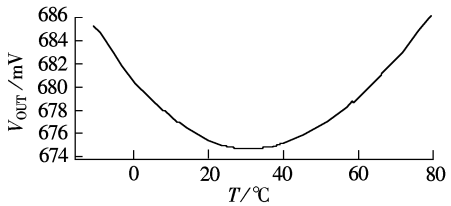

Fig.5 Output voltage vs. temperature (V_{DD} = 2.5 V)

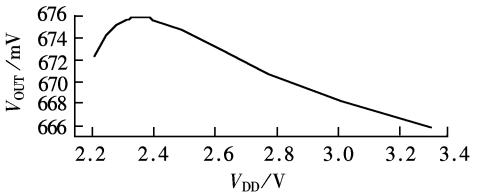

Fig.6 Output voltage vs. supply voltage

4 Conclusion

A CMOS BGR without resistors, which can output below 1 V voltage, has been proposed and simulated. It consumes less power compared with the BGR discussed in Ref.[2], and is suitable for low voltage operations. Since the BGR circuit has two stable operating points, a start-up circuit is added to ensure that the BGR ends up in the correct state. This start-up circuit takes the advantage of consuming zero static current.

References

[1] Banba H, Siga H, Umezawa A, et al. A CMOS bandgap reference circuit with sub-1-V operation [J]. *IEEE J of Solid-State Circuits*, 1999, **34**(5):670 - 674.

[2] Buck A, McDonald C, Lewis S, et al. A CMOS bandgap reference without resistors [J]. *IEEE J of Solid-State Circuits*, 2002, **37**(1):81 - 83.

[3] Orrance R R T, Viswanathan T R, Hanson J V. CMOS voltage to current transducers [J]. *IEEE Tran Circuits Sys*, 1985, **32**(11):1097 - 1104.

[4] Oguey H J, Aebischer D. CMOS current reference without resistance [J]. *IEEE J of Solid-State Circuits*, 1997, **32**(7):1132 - 1135.

输出电压低于 1 V 的无电阻 CMOS 带隙基准电压源

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摘　要　本文提出了一种带隙基准电压源,它能产生低于 1 V 的精确基准电压.该电路有较高性能的启动电路使电路在上电时能进入正确的状态.在 0.25 μm CMOS 工艺条件下,电路的各项性能指标采用 HSPICE 进行模拟验证.模拟结果表明该电路在 2.2 V ~ 3.3 V 的电源电压变化范围内、在 −10 ~ 80 ℃温度变化范围内,输出电压的变化不超过 11 mV.

关键词　带隙基准; 启动电路; CMOS; 低电压

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