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Key technologies of frequency-hopping frequency synthesizer for Bluetooth RF front-end

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Abstract: A scheme of a frequency-hopping frequency-synthesizer applied to a Bluetooth ratio frequency (RF) front-end is presented, and design of a voltage controlled oscillator (VCO) and dual-modulus prescaler are focused on. It is fabricated in a 0.18 μm mixed-signal CMOS (complementary metal-oxide-semiconductor transistor) process. The power dissipation of VCO is low and a stable performance is gained. The measured phase noise of VCO at 2.4 GHz is less than −114.32 dBc/Hz. The structure of the DMP is optimized and a novel D-latch integrated with "OR" logic gate is used. The measured results show that the chip can work well under a 1.8 V power supply. The power dissipation of the core part in a dual modulus prescaler is only 5.76 mW. An RMS jitter of 2 ps is measured on the output signal at 118.3 MHz. It is less than 0.02% of the clock period.

Key words: Bluetooth; frequency hopping; frequency synthesizer; voltage controlled oscillator (VCO); dual-modulus prescaler; programmable divider

Generally, it contains a phase locked loop (PLL) synthesizer, transmitting and receiving functions in a monolithic, integrated Bluetooth ratio frequency (RF) transceiver. The PLL is shared between the transmitter and the receiver, so it is a key section. Furthermore, the research and design of the PLL frequency synthesizer in the Bluetooth system are relatively difficult for frequency hopping (FH) one. The FH synthesizer is built with components such as a voltage controlled oscillator (VCO), dual-modulus prescaler (DMP), programmable divider, phase-frequency detector (PFD), charge pump (CP) and frequency comparator (FC), etc. This paper focuses on some vital blocks in the RF transceiver.

1 System Block of an FH Synthesizer

The design of a VCO and a DMP in FH synthesizer architecture is more difficult because of the high frequency and the high speed. In this paper, the design is focused on an FH synthesizer. As shown in Fig. 1, an off-chip passive loop filter is adopted to adjust loop bandwidth and damping factor. The frequency dividers are built up with both DMP and programmable divider. The scaling factor of DMP is V and $V+1$. The programmable divider block includes two programmable down counters, counter_A and counter_B[1-3]. The overall division ratio is $AV+B$. The FC block is used for comparing the reference frequency and the frequency of the VCO feedback signal to indicate PLL locked time. A pulse will appear when the PLL is locked.

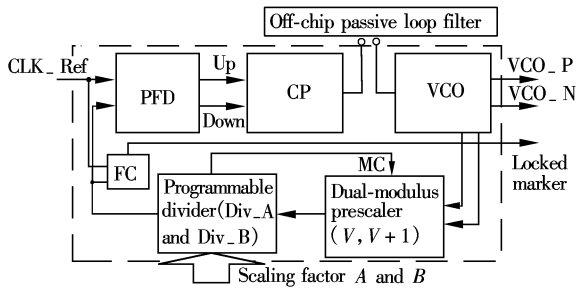

Fig. 1 System block of the FH synthesizer

2 VCO Design

It is a cross-coupled differential VCO with both PMOS and NMOS cross-coupled amplifying units, which generate a negative resistance to compensate the loss of the LC tank[3,4]. The LC tank consists of two rectangular spiral inductors made of thick AlCu metal, two MIM capacitors, and two MOS varactors made of thin oxide MOS structure with a three group gate. The VCO buffer is also an important circuit in the design of the VCO and it is used for improving driving capacity and isolation between the LC tank and the load. In this design, a symmetrical PMOS and NMOS buffer is used, different from conventional architecture. The main advantage of this VCO architecture is that symmetrical waveforms and lower distor-

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tion can be obtained[5,6].

A schematic of the VCO circuit is given in Fig. 2 and when operational frequency is 2.453 GHz, a transient wave of the VCO is shown in Fig. 3(a). The measured phase noise is −114.32 dBc/Hz at a frequency offset of 2.4 MHz as shown in Fig. 3(b).

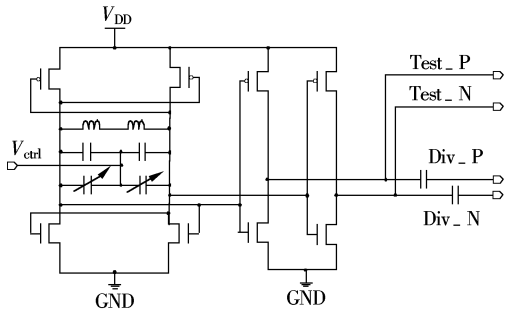
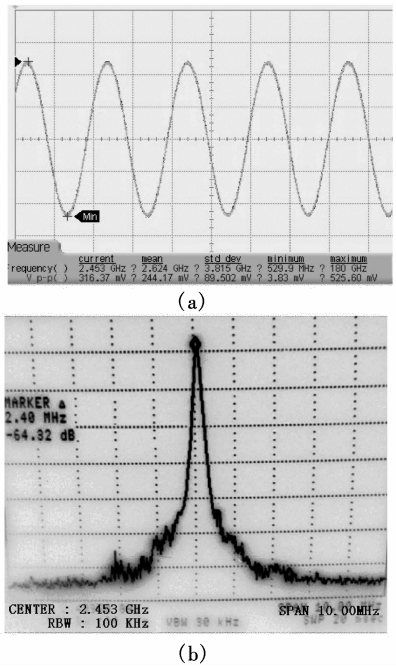


Fig. 2 Schematic of the VCO circuit



(a)

(b)

Fig. 3 Tested waves of VCO. (a) Transient waves; (b) Phase noise

3 DMP Design

Another block operating on the high frequency band is the DMP in the total synthesizer. In this paper, a novel D-latch architecture integrated with "OR" logic gate is presented. The implemented circuit of the DMP is shown in Fig. 4(a). Fig. 4(b) shows the D-latch circuit schematic integrated with "OR" logic gate. It is verified that the D-latch can work 20% faster than a normal D-latch without integrated logic gate[6-8].

The D-latch is made up of improved master/slave FSCL D-flip-flop. D_1 and D_2 form the input port of the integrated "OR" logic and VB is a bandgap reference 1 V voltage. The advantage of using complementary cross-couple pairs M_6, M_7 and M_8, M_9, instead of one NMOS cross-couple pair M_6, M_7, is to

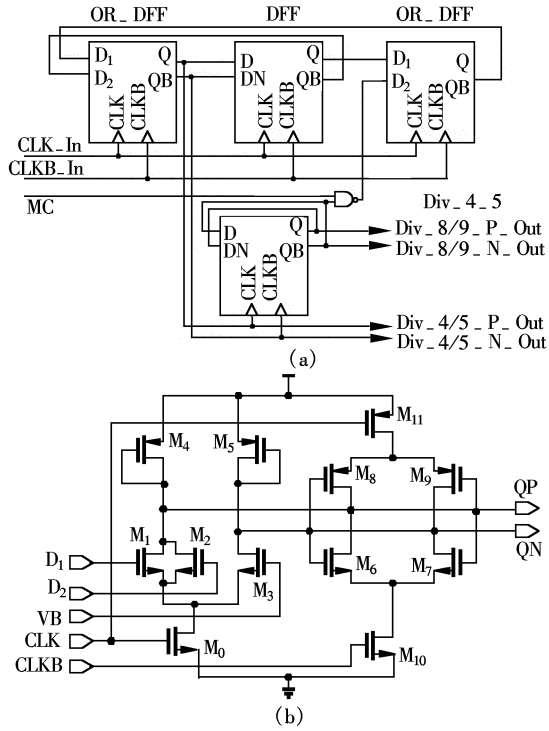


Fig. 4 Bolck of DMP and D-latch. (a) Block of DMP; (b) D-latch integrated with "OR"

increase the swing of output signals (QP, QN) under the condition that the speed of D-flip-flop is not decreased. The large swing output can directly drive the following block and no following amplifier is needed. Thus, the complexity of the circuit is decreased[9].

The measured output wave of the DMP is shown in Fig. 5, wherein the scaling factor is switched to the value $V+1$ ($=9$). An RMS jitter of only 2 ps was measured from the output signal at the frequency of 118.3 MHz, corresponding to 0.02% of the output clock period. The power dissipation of the core part in the dual modulus prescaler is only 5.76 mW.

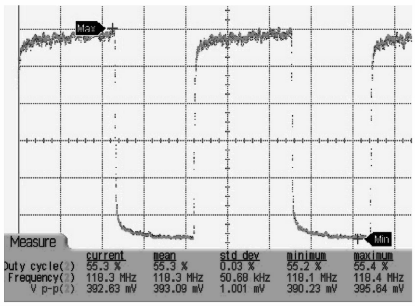


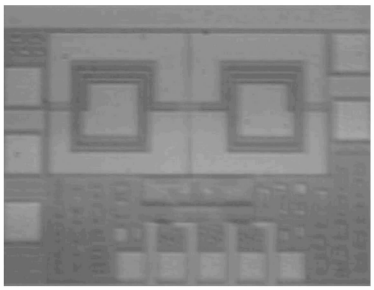
Fig. 5 Tested transient waves of the DMP

4 Programmable Divider and FC

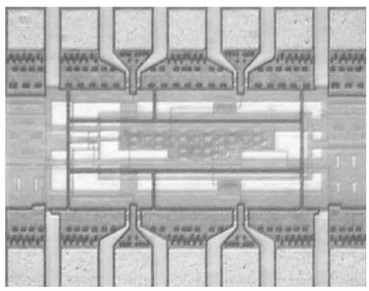
The programmable divider works at a lower frequency band than the prescaler. It includes two programmable counter-down units. They were synthesized by means of Verilog-HDL. The FC is a section used to indicate the settling time of the synthesizer, by comparing reference frequency with feedback frequen-

cy of the VCO. Two counters are used for the reference clock and the feedback clock. We make them count at the same factors (for example 1 024). Two clock frequencies are equal when two counters work at the same speed. A pulse would appear when these two clock frequencies were equal.

The VCO and the DMP have been fabricated successfully in 0.18 μm mixed-signal CMOS process and their die photos are shown in Figs. 6(a) and (b).



(a)



(b)

Fig. 6 Two die photos. (a) Photo of VCO; (b) Photo of DMP

5 Conclusion

The key technologies of the FH synthesizer in Bluetooth RF front-end are introduced. The VCO and the DMP have been fabricated successfully in 0.18 μm mixed-signal CMOS process. Measured results show that higher performance is gained.

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蓝牙射频前端跳频频综的几项关键技术

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摘要:提出了应用于蓝牙射频前端的跳频频率综合器的设计方案,并介绍了关键模块压控振荡器与双模预分频器的设计技术,采用混合 0.18 μm CMOS 工艺进行了流片验证. 设计的压控振荡器性能稳定,低功耗低相噪,频率在 2.4 GHz 时测试相位噪声达 -114.32 dBc/Hz@2.4 MHz. 对双模分频器进行了设计优化,并采用一种集成"或"逻辑的锁存器结构,降低了功耗,提高了电路速度. 测试结果显示电路在 1.8 V 时稳定工作双模分频器核心功耗仅5.76 mW;均方差抖动在输出周期为 118.3 MHz 时仅为 2 ps,约占输出周期的 0.02%.

关键词:蓝牙;跳频;频率综合;压控振荡器;双模预分频器;可编程分频器

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