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2.5 Gbit/s monolithic ICs for optical fiber transmitter and receiver in 0.35 μm CMOS process

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Abstract: 2.5 Gbit/s monolithic integrated circuits (ICs) for optical fiber transmitter and receiver in 0.35 μm CMOS (complementary metal-oxide-semiconductor transistor) process are presented. The transmitter, which includes a 4∶1 multiplexer and a laser diode driver (LDD), has four 622 Mbit/s random signals as its inputs and gets a 2.5 Gbit/s driving signal as its output; the receiver detects a 2.5 Gbit/s random signal and gets four 622 Mbit/s signals at the output. The main circuits include a trans-impedance amplifier (TIA), a limiting amplifier, a clock and data recovery (CDR) unit, and a 1∶4 demultiplexer (DEMUX). Test results prove the logic functions of the transmitter to be right, and the 10% to 90% rise and fall times of transmitter's output data eye diagram are 211.1 ps and 200 ps, respectively. The sensitivity of the receiver is measured to be better than 20 mV. The root mean square jitter of the DEMUX's output data is 15.6 ps and that of the clock after 1∶4 frequency dividing is 1.9 ps. Two chips are both applicable to 2.5 Gbit/s optical fiber communication systems.
Key words: optical fiber communication; monolithic; transmitter; receiver

With rapid development of CMOS technologies, it is possible to design ICs in CMOS for 2.5 to 10 Gbit/s optical data links. A 2.5 Gbit/s transceiver without LDD and TIA has been reported, fabricated in a 0.18 μm CMOS[1] and 2.4 to 2.5 Gbit/s receivers have been realized in a 40 GHz-f_T Si-bipolar[2], a 60 GHz-f_T SiGe-bipolar[3] and a 0.15 μm CMOS[4], respectively. In this paper we present a transmitter IC including a 4∶1 multiplexer and an LDD and a receiver IC including all functions of a TIA, a limiting amplifier, a clock and data recovery (CDR) unit, and a 1∶4 demultiplexer (DEMUX). They are realized in a standard 0.35 μm CMOS process with an f_T of about 13.5 GHz for two reasons: ① To integrate the LDD, which needs a high supply voltage of 5 V, ② To reduce the production cost. The successful integration is based on many efforts of our previous works[5-7].

1 Circuits Framework

Fig. 1 shows the diagram of an optical fiber transmission system for synchronous transfer mode (STM)-16, in which the dashed regions represent the transmitter and the receiver. The transmitter includes a 4∶1 multiplexer and an LDD. The receiver includes an amplifier, a CDR unit and a 1∶4 DEMUX. Source coupled logic (SCL) circuits are adopted widely.

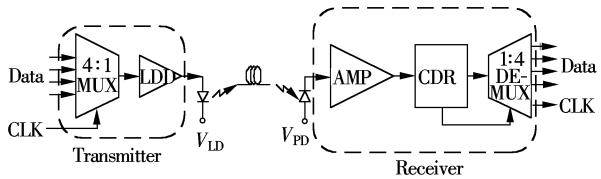

Fig. 1 Block diagram of an optical fiber transmission system

Fig. 2 presents the detailed structure of the transmitter. It consists of three 2∶1 multiplexers, two 1∶2 frequency dividers, one signal reshaping circuit and one LDD. Three 2∶1 multiplexers configure the desired 4∶1 multiplexer in a tree-type architecture and each 2∶1 multiplexer includes a master-slave D-type

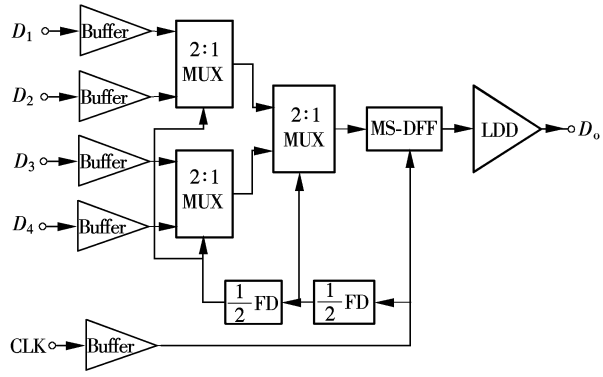

Fig. 2 Block diagram of the transmitter

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flip-flop (MS-DFF), a master-slave-slave D-type flip-flop (MSS-DFF) and a 2∶1 selector. This classical structure has been proved to achieve stable operation at ultra-high speeds. The additional MS-DFF, following the multiplexer, makes signal reshaping to determine the waveform and the phase relationship between data and clock, consequently allowing operation at the full bit rate. Due to the presence of a dead-zone in the multiplexer, it is a challenge to guarantee sufficient phase margin. Two different 1∶2 frequency dividers, constructed by an MS-DFF with feedback, generate required clocks whose phases should be controlled and carefully accommodated to the data edges. It is known that a differential amplifier has the advantages of common mode rejection, high-speed operation, etc. Although the LDD's output is single-ended, the driver uses cascaded differential amplifier and source followers for signal amplification and impedance match. In addition, the output current swing of the LDD can be controlled through an off-chip resistor.

As shown in Fig. 3, the receiver is composed of a TIA, a limiting amplifier, a clock recovery (CR), a data decision (DEC) and a 1∶4 DEMUX. The TIA adopts voltage parallel feedback to obtain adequate trans-impedance gain. For the single-ended to differential conversion, a linear controllable active resistor is utilized to configure a low-pass filter to avoid large resistor dimension. A six-stage differential amplifier with a DC feedback network constructs a limiting amplifier to get sufficient voltage gain. The non-linearity of the differential amplifier is used for limiting function.

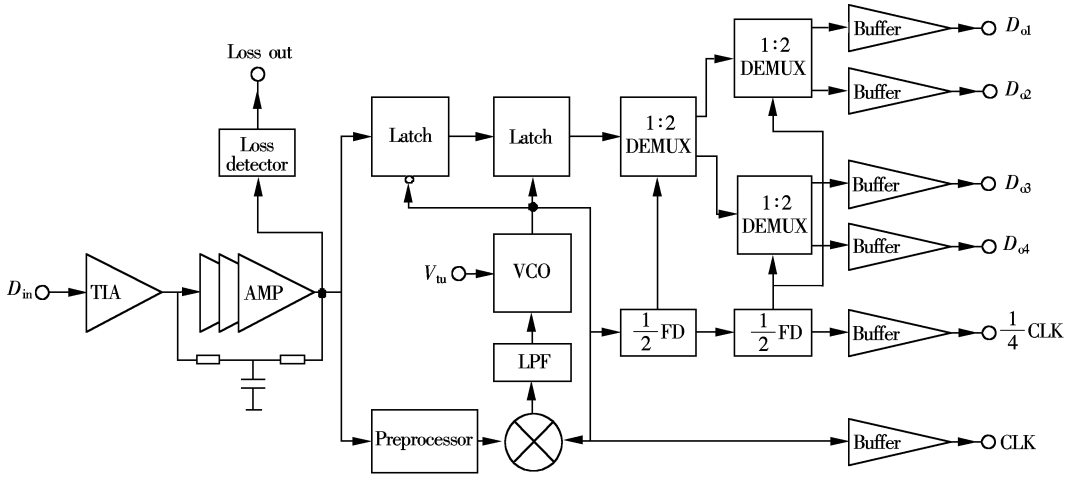


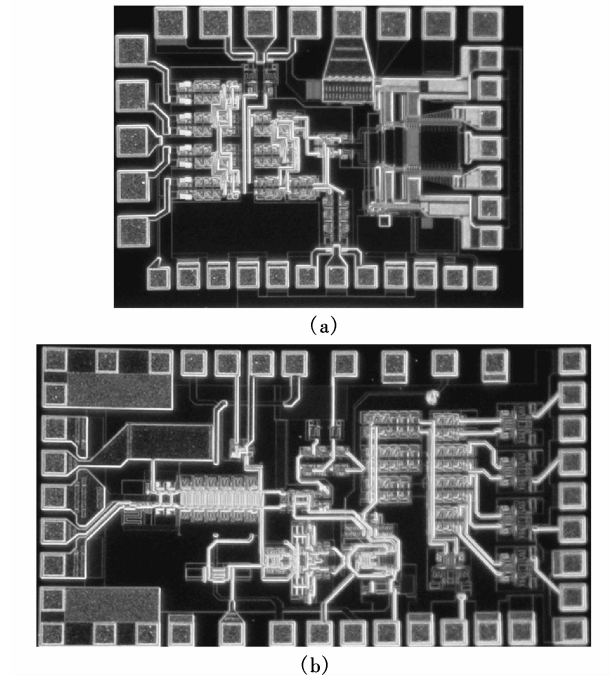
Fig. 3 Block diagram of the receiver

Usually, a tradeoff should be considered between gain and bandwidth. Benefiting from a spiral poly-silicon resistor, a small parasitic inductor compensates the gain loss in the high frequency range to achieve extended bandwidth with the same gain. The CR circuit consists of a preprocessor and a PLL. Due to lack of passive inductor modeling, an active inductor is more suitable for the band-pass filter in the preprocessor, with the probability it will obtain higher quality coefficient. The VCO integrated in the PLL has a ring-type architecture consisting of three stages of differential amplifiers. The waveform of the VCO's output signal is designed to be strictly symmetrical to achieve a high phase-noise performance. The main tasks of the DEC circuit are to retime and reshape the waveform of the data signal and to lock its phase to the clock, through the sampling and the latching function. The initial phase of the clock before sampling should be centralized in respect of the data to overcome the PLL's phase error suffering from variety in temperature, supply, process, etc. Similar to the multiplexer in a transmitter, the 1∶4 DEMUX in the receiver also has a tree-type architecture, composed of three 1∶2 DEMUXs and two 1∶2 frequency dividers.

2 Layout Design

Monolithic chips of the transmitter and the receiver are fabricated in a 0.35 μm standard CMOS process. Their microphotographs are shown in Fig. 4. The chip area of the transmitter is 1 mm × 1.36 mm and that of the receiver is 1.6 mm × 0.87 mm. The chips are laid out by using symmetrical cells to obtain equal differential signal paths and coplanar wave-

guides (CPW) along signal paths are utilized to eliminate crosstalk.



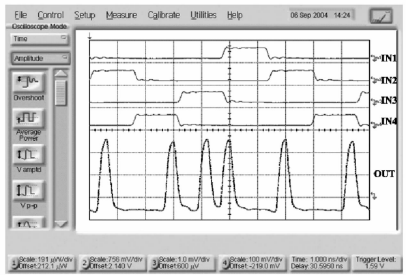
(a)

(b)

Fig. 4 Microphotographs. (a) The transmitter; (b) The receiver

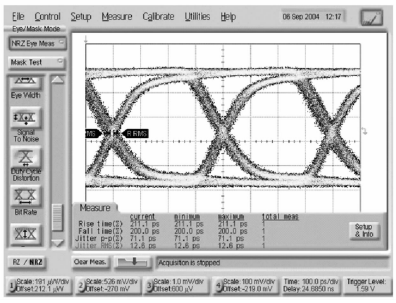
3 Experimental Results

The measurement has been made on-chip. Under one 5 V supply, the power consumptions of the transmitter and the receiver chips are 0.85 W and 2 W, respectively. With four 625 Mbit/s 4 bit word inputs, the input and output waveforms of the transmitter are presented in Fig. 5, which proves the logic function of the whole transmitter to be correct. Replacing the inputs with four 625 Mbit/s $2^{31}-1$ PRBS, a 2.5 Gbit/s output data eye diagram of the transmitter shown in Fig. 6 can be got, whose 10% to 90% rise and fall times are 211.1 ps and 200 ps, respectively. Measured results show that the LDD can provide a driving current from 20 mA to 65 mA through off-ship adjusting. The RMS and peak-peak jitters of the output voltage on a 50 Ω external load are 12.6 ps and 71.1 ps, respectively. In the same way, with a 2.488 Gbit/s 32 bit word input, the receiver can achieve four perfect output waveforms, as shown in Fig. 7. When the input is changed into 2.488 Gbit/s $2^{31}-1$ PRBS, the recovered clock after 1∶4 dividing shows an RMS jitter of 1.9 ps and a peak-peak jitter of 15.6 ps, presented in Fig. 8. The output data has an RMS jitter of 13 ps and a peak-peak jitter of 67 ps. The sensitivity of the receiver is measured to be better than 20 mV and the tracking range is more than 50 Mbit/s. The detailed performance of two chips is summarized in Tab. 1.



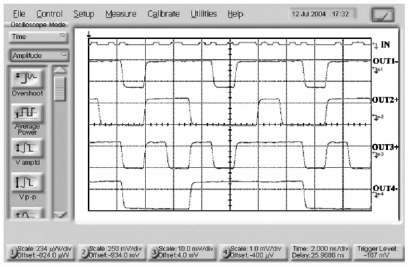
1 ns/div, 756 mV/div

Fig. 5 Input/output data waveforms of the transmitter



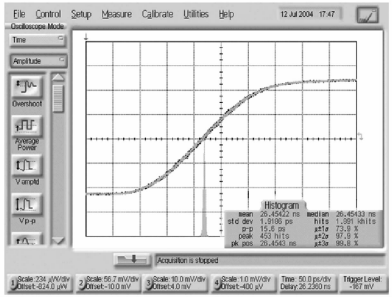
100 ps/div, 526 mV/div

Fig. 6 Output eye diagram of the transmitter



2 ns/div, 250 mV/div

Fig. 7 Input/output data waveforms of the receiver



50 ps/div, 56.7 mV/div

Fig. 8 Jitter histogram of the recovered clock after 1∶4 dividing

Tab. 1 Performance of the transmitter and the receiver

Transmitter	Supply voltage/V	5
	Supply current/mA	170
	Rise time (10% to 90%)/ps	211. 1
	Fall time (10% to 90%)/ps	200
	Output current/mA	20 to 65
	Jitter RMS/p-p of output data	12. 6 ps, 0. 031 5UI; 71. 1 ps, 0. 177 8UI
	Chip area/mm^2	1 × 1. 36
Receiver	Supply voltage/V	5
	Supply current/mA	400
	Sensitivity	< 20 mV, single-ended peak-to-peak
	Tracking range/(Gbit · s^{-1})	2. 46 to 2. 51
	Phase noise of recovered clock (622 MHz)	− 111 dBc/Hz@ 1 MHz
	Jitter RMS/p-p of recovered clock (622 MHz)	1. 9 ps, 0. 001 2UI; 15. 6 ps, 0. 009 7UI
	Jitter RMS/p-p of output data	13 ps, 0. 008 1UI; 67 ps, 0. 042UI
	Chip area/mm^2	1. 6 × 0. 87

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2. 5 Gbit/s 0. 35 μm CMOS 光纤通信用收发全集成电路

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摘要: 采用 0. 35 μm CMOS 工艺设计2. 5 Gbit/s速率光纤通信用收发全集成电路. 发射部分包括复接和激光驱动电路, 完成 4 路 622 Mbit/s 随机信号输入、1 路2. 5 Gbit/s驱动信号输出的功能; 接收部分完成 1 路 2. 5 Gbit/s 微弱随机信号输入、4 路 622 Mbit/s 分接输出功能. 主要电路包括前置放大、限幅放大、时钟恢复、数据判决和 1∶4 分接. 测试结果显示, 2. 5 Gbit/s 光纤通信用发射芯片逻辑功能正确, 激光驱动器输出数据眼图 10% ~90% 上升、下降沿时间分别为 211. 1 ps 和 200 ps; 2. 5 Gbit/s 光纤通信用接收芯片接收灵敏度优于 20 mV, 恢复出的数据和时钟分别经过 1∶4 数据分接和 1∶4 时钟分频后, 相位抖动的均方根值分别为 15. 6 ps 和 1. 9 ps. 两芯片均适用于 2. 5 Gbit/s 速率光纤通信系统.

关键词: 光纤通信; 全集成; 发射机; 接收机

中图分类号: TN402; TN492