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A kind of low-power 10 Gbit/s CMOS 1∶4 demultiplexer

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Abstract: A 10 Gbit/s 1∶4 demultiplexer(DEMUX) fabricated in 0.18 μm CMOS (complementary metal-oxide-semiconductor transistor) technology for optical-fiber-link is presented. The system is constructed in tree-type structure and it includes a high-speed 1∶2 DEMUX, two low-speed 1∶2 DEMUXs, a divider, and input and output buffers for data and clock. To improve the circuit performance and reduce the power consumption, a latch structure with a common-gate topology and a single clock phase is employed in the high-speed 1∶2 DEMUX and the 5 GHz 1∶2 on-chip frequency divider, while dynamic CMOS logic is adopted in the low-speed 1∶2 DEMUXs. Measured results at 10 Gbit/s by $2^{31}-1$ pseudo random bit sequences (PRBS) via on-wafer testing indicate that it can work well with a power dissipation of less than 100 mW at 1.8 V supply voltage. The die area of the DEMUX is 0.65 mm × 0.75 mm.

Key words: optical communication; CMOS; demultiplexer (DEMUX); low-power

The demultiplexer (DEMUX) used to convert single high-speed data stream to multiple low-speed data streams is a key building block in fiber communication receiver. A number of DEMUX-ICs ranging from several Gbit/s up to higher than 40 Gbit/s have been reported in various technologies[1-4], and research has been made to raise the speed of circuit modules. However, with the booming increment of operating speed, the issue of high power dissipation is gradually becoming a focus of attention. This paper illustrates the detailed realization of a 10 Gbit/s 1∶4 low-power DEMUX in TSMC 0.18 μm CMOS technology, in which a latch structure with single clock phase and dynamic CMOS logic were adopted. This circuit can operate at 10 Gbit/s with only 100 mW power consumption. The research is identified as being attractive in reducing cost and power consumption compared to the 0.18 μm CMOS realization of 10 Gbit/s DEMUX reported recently[5].

1 Circuit Design

The block diagram of the 1∶4 demultiplexer circuit is shown in Fig. 1, in which a conventional tree-type structure is employed. In the input, the high-speed DEMUX de-multiplexes 10 Gbit/s data D to two 5 Gbit/s data Q_1 and Q_2, while the 2.5 GHz clock is obtained from the 5 GHz clock (CLK) by a 1∶2 frequency divider. Buffers following the divider are utilized to obtain sufficient driving capability to meet the requirement of two low-speed DEMUXs and the out-buffer for measurement. Whilst, to ensure correct timing and thus acquire correct data, buffers connected to the output of the corresponding high-speed DEMUX are essential. Then the two 5 Gbit/s data Q_a, Q_b and one 2.5 GHz clock (CLK_1) are transmitted to two low-speed DEMUXs and four 2.5 Gbit/s data are finally obtained at the output. The 1∶2 high-speed DEMUX consists of master-slave-slave (MSS) and

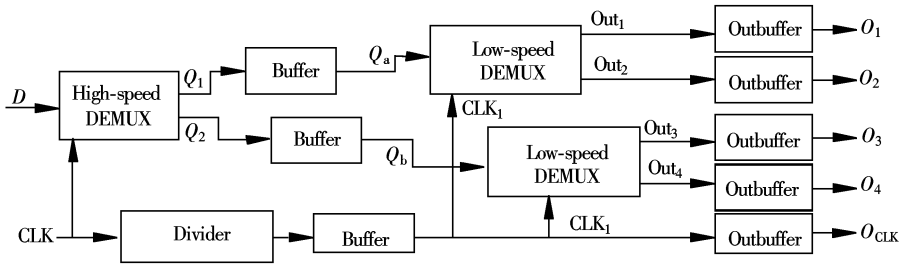

Fig. 1 Block diagram of 1∶4 DEMUX

master-slave (MS) D flip-flops as shown in Fig. 2. The input clock CLK is used to time the latches of the high-speed DEMUX, while the divided CLK_1 is used to time the latches of the low-speed DEMUX. This architecture is optimum in power consumption since, in the

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DEMUX, only the high-speed DEMUX operates at full rate. Moreover, subsequent demultiplexing can be implemented to lower the power dissipation of the DEMUX by using different structures. By using the low power latch structure shown in Fig. 3, we can reduce the DEMUX power further.

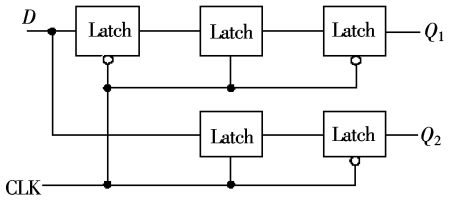

Fig. 2 Block diagram of the 1∶2 high-speed DEMUX

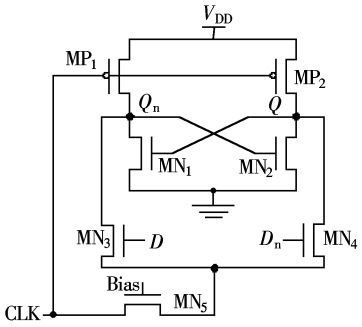

Fig. 3 Schematic of the latch

The traditional DEMUX, based on the SCFL (source coupled FET logic) structure[5], consumes more power since the working current is always being. Whereas the latch structure[6] used in the high-speed DEMUX and the divider, consumes nearly half the power of the SCFL latch, since its working current is provided in a switch mode. As shown in Fig. 3, the latch structure consists of a pair of PMOS dynamic loads (MP_1-MP_2), a latching pair (MN_1-MN_2), a sampling pair (MN_3-MN_4) and a clock switch transistor (MN_5). When CLK = L, MN_5 is on and the latch operates in the sampling mode. At this moment, the time constant is reduced significantly since the PMOS load transistors (MP_1-MP_2) operate in the linear region and their turn-on resistances are very small. And the chain reaction induced by the positive feedback loop which is made up of an NMOS cross-coupled transistor pair (MN_1 and MN_2) accelerates the process of transitions. Therefore, the input D is sampled to output within an instantaneous period.

When CLK = H, MN_5 is off and the latch works in the latching mode. PM_1-PM_2 are turned off; hence, there is a large RC time constant. Meanwhile, MN_1 and MN_2 hold the last sampled data. In this mode, the current of the latch approximates zero, thus leading to the reduction in power dissipation.

Another way to reduce the power in this DEMUX is to utilize dynamic CMOS logic[7] in the low-speed DEMUX operating at 2.5 GHz clock and 5 Gbit/s data rate. In dynamic CMOS logic (see Fig. 4), the capacitor C_P is used to store the input value, and thus retains its cross-voltage at input level until CLK_1 (half of CLK) goes to low level and the transmission gate turns off. C_p normally is not explicitly included, but it is the parasitic input capacitor of the inverter and the junction capacitance of the transmission gate.

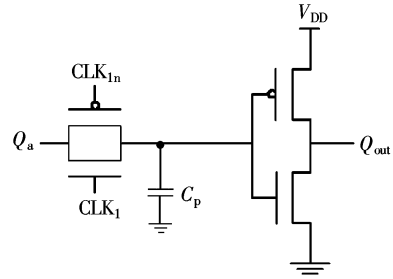

Fig. 4 Schematic of dynamic CMOS logic

The dynamic latch must be refreshed periodically, otherwise its value might be corrupted due to the leakage current of the transmission-gate junctions. Nevertheless, CLK_1/CLK_{1n} here is of 2.5 GHz, which is absolutely during the maximum refresh periods. As a result, the dynamic CMOS latch is adopted here considering its higher speed performance over the static one.

Master-slave-slave and master-slave D flip-flops are also used in the low-speed DEMUX as in the high-speed DEMUX. Different from Fig. 2, in Fig. 5, we take Q_{an} (one output of the high-speed DEMUX) as the input of MSS D flip-flops, and Q_a as the input of MS D flip-flops. Contrary phase is adopted to time the latches of the low-speed DEMUX.

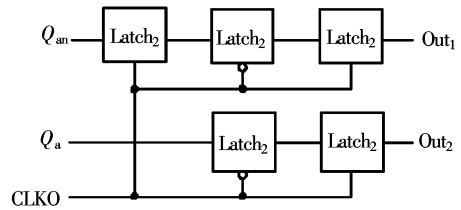

Fig. 5 Block diagram of the 1∶2 low-speed DEMUX

Between the high-speed DEMUX and the low-speed DEMUX, a hybrid of the differential amplifier and the CMOS static complementary circuit inverter shown in Fig. 6 is used to connect the two DEMUXs. The differential amplifier acts to lower the output potential of the high-speed DEMUX, and the CMOS static complementary circuit inverters amplify the output signal to full swing.

As shown in Fig. 7, the last stage with a drain-cur-

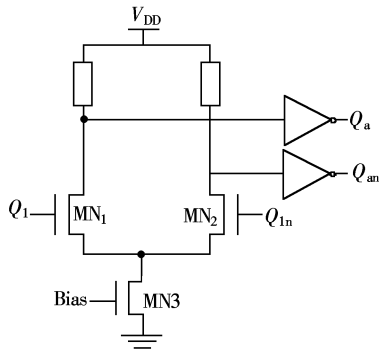

Fig. 6 Schematic of the buffer

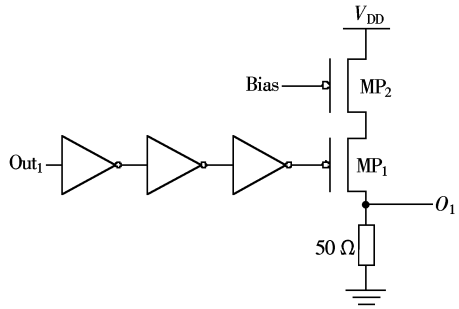

Fig. 7 Schematic of the output interface

rent output generates a 400 mV voltage on a 50 Ω resistor, which is the input-impedance of the testing equipment. Three tapered inverters afford sufficient driving capability to drive the output, and MP_2 is an 8 mA current source while MP_1 works as a switch.

2 Measurement Results and Discussions

Fig. 8 shows the micrograph of the DEMUX chip and its area is 0.65 mm × 0.75 mm. The DEMUX is tested on-wafer using high-speed microwave probes of Cascade Microtech Inc. The DC current of the DEMUX is less than 53 mA with 1.8 V supply voltage, corresponding to the power dissipation of less than 100 mW. The input clock is 5 GHz, and due to the restriction of our laboratory facilities, only a 5 Gbit/s is generated as the input test signal to the DEMUX. Fig. 9 shows the two outputs of measured waveforms of the 1∶4 DEMUX when the input 5 Gbit/s pattern is 1001 1110 0011 1001, taken as 1100 0011 1111 1100 0000 1111 1100 0011 at 10 Gbit/s. And the output eye diagram (shown signal-ended) under the input data of a 10 Gbit/s $2^{31}-1$ pseudo random bit sequence (PRBS) is presented in Fig. 10.

During the measurement, the function of the 1∶4 DEMUX is verified, but we can see random ripples which are not so perfect when the output data is "1" in the waveforms in Fig. 9. Simulation results show that the PMOS transistor current source PM_2 of the output interface (shown in Fig. 7) may result in such problems. Because the generated current is related with V_{GS} = bias − V_{DD}, as a result, it slightly changes with supply noise. An alternate output interface composed of NMOS transistors shown in Fig. 11 may solve this problem, since the V_{GS} of current source MN_2 has no direct relationship with V_{DD}.

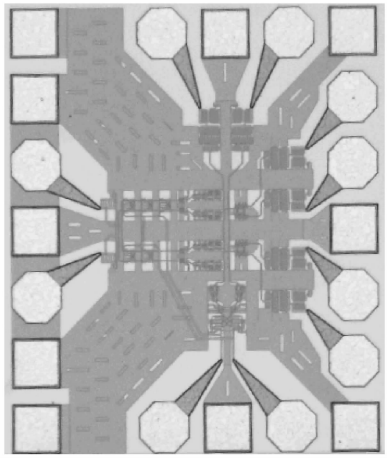

Fig. 8 Chip micrograph of the DEMUX

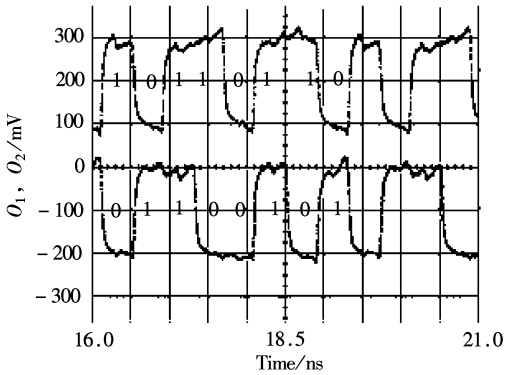

Fig. 9 Measured waveforms of 1∶4 DEMUX

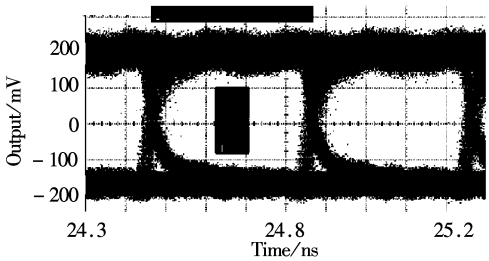

Fig. 10 2.5 Gbit/s output data eye diagram

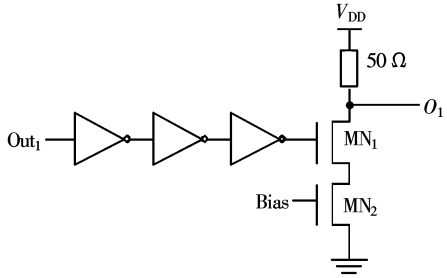

Fig. 11 Improved circuit of output interface

3 Conclusion

A 10 Gbit/s low-power 1∶4 demultiplexer has been realized in standard TSMC 0.18 μm CMOS technology for optical-fiber-link systems. Tree-type architecture makes it possible to reduce the speed by stages. The circuit is optimized by employing different latch structures in high-speed and low-speed DEMUXs. Both the common-gate topology latch structure and the dynamic CMOS latch contribute to the reduction of power consumption even with the higher power consumption of the interface circuits. Measured results indicate that it can work well at 10 Gbit/s with a power dissipation less than 100 mW at 1.8 V supply voltage. The area of the DEMUX is 0.65 mm × 0.75 mm. More improvement will be carried out in the future.

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一种低功耗的 10 Gbit/s CMOS 1∶4 分接器

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摘要：采用 TSMC 0.18 μm CMOS 工艺实现了一种应用于光纤通信系统 SDH STM-64 的 10 Gbit/s 1∶4分接器，整个系统采用树型结构，由 1 个高速 1∶2 分接器、2 个低速 1∶2 分接器、分频器以及数据和时钟输入输出缓冲组成. 为达到优化性能、降低功耗的目标，其中高速分接部分和 5 GHz 1∶2 分频器都采用共栅结构、单时钟输入的锁存器；而低速分接部分则由动态 CMOS 逻辑实现. 通过在片晶圆测试，该芯片在输入 10 Gbit/s、长度为 $2^{31}-1$ 的伪随机码流时工作性能良好，电源电压 1.8 V，功耗仅为 100 mW. 芯片面积为 0.65 mm × 0.75 mm.

关键词：光纤通信；CMOS；分接器；低功耗

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