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Gate breakdown of high-voltage P-LDMOS and improved methods

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Abstract: The failure experiments of the P-LDMOS (lateral double diffused metal oxide semiconductor) demonstrate that the high peak electrical fields in the channel region of high-voltage P-LDMOS will reinforce the hot-carrier effect, which can greatly reduce the reliability of the P-LDMOS. The electrical field distribution and two field peaks along the channel surface are proposed by Tsuprem-4 and Medici. The reason of resulting in the two electrical field peaks is also discussed. Two ways of reducing the two field peaks, which are to increase the channel length and to reduce the channel concentration, are also presented. The experimental results show that the methods presented can effectively improve the gate breakdown voltage and greatly improve the reliability of the P-LDMOS.

Key words: peak electrical field; hot-carrier effect; reliability

Since HV-CMOS has well-known intrinsic advantages: high input impedance, short switching time and thermal stability, it has been developed for a variety of applications, such as audio amplifiers, automotive electronics, motor drivers, and flat display panel drivers, etc[1-3]. In the CMOS technology, the most part of the power driver ICs on the die, up to 70%, is taken up by HV-CMOS transistors, so the reliability of HV-CMOS is the most important factor in improving the reliability of the whole power driver ICs. However, high-voltage P-LDMOS is one of the two important devices of HV-CMOS, so improving the reliability of P-LDMOS is very important in improving the reliability of the whole power driver ICs. In most high-voltage IC systems, when high-voltage P-LDMOS is in the on-state, the gate voltage is set to 0 V, but the source voltage is very high, such as PDP driver ICs, VFD driver ICs, etc[4]. So the electrical field along the channel surface of the P-LDMOS is very high, which results in the hot-carrier effect and greatly degrades the reliability of the P-LDMOS. Ref. [5] discussed the microcosmic reasons for the poly-gate breakdown resulting from the hot-carrier effect, but it did not present the reasons for the gate breakdown. Ref. [6] illuminated the macroscopical reasons, but it did not reveal any ways to reduce the hot-carrier effect. In Ref. [7], research on the proposed LDMOS used as a switch focused on the drift region, but the channel region was neglected.

In this paper, the electrical field distribution along the channel surface of the P-LDMOS is discussed in detail. The reasons causing the electrical field peaks is given. The methods for reducing the values of the electrical field peaks and reducing the hot-carrier effect are also presented. The simulation and experimental results show that the methods are very effective in reducing the hot-carrier effect and in improving the reliability of the P-LDMOS.

1 Device Structure and Process

The cross-section and size of the initial high-voltage P-LDMOS are shown in Fig. 1, which has been fabricated based on a 1.2 μm rule epitaxy standard CMOS process. The length of the p-drift is 15 μm, and the junction depth of the p-drift satisfies the RESURF technology[8]. The junction depth of the n-well is 2 μm. The n-well, which is used to avoid punch-through, and the p-drift have been formed by using phosphorus with implanted doses of 10^{14} cm^{-2} and boron with implanted doses of 4×10^{12} cm^{-2}, respectively. The idiographic compatible process flow is shown in Fig. 2. First, an n-epitaxy layer was formed. Secondly, the p-drift diffusion

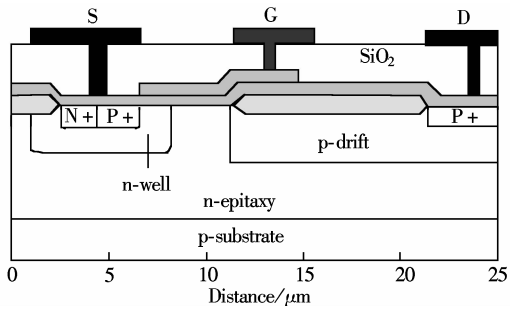

Fig. 1 Schematic cross-section of the initial P-LDMOS

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layer was fabricated. Thirdly, the n-well diffusion layer was formed. Finally, the following process was the same as the LV-CMOS process. In this way, these high-temperature diffusion processes for high-voltage P-LDMOS were fabricated before the standard LV-CMOS process, so the high-voltage P-LDMOS can be compatible with the LV-CMOS and can be used in power ICs.

1. BS p-substrate
2. n-epitaxy formation
3. p-drift formation
4. n-well formation
5. LOCOS formation
6. Channel doping
7. Gate formation
8. S/D formation
9. Contact
10. Metallization

Fig. 2 Compatible process flow of the P-LDMOS

2 Failure Analysis

Fig. 3 shows the electrical field distribution of the P-LDMOS in the silicon side along the Si-SiO_2 interface in the on-state of the initial P-LDMOS. From Fig. 3, one can see that there are two electrical field peaks in the channel region of the P-LDMOS. Peak 1 locates near the P^+N^- junction formed by the P^+ source and the n-well, and peak 2 locates at the PN junction formed by the p-drift and the channel. The hot-carriers in the channel region are strongly generated by the two electrical field peaks. The generated hot-carriers then will bombard the gate oxide and reduce the breakdown voltage of the gate oxide gradually, which can be seen from the experimental results in Fig. 4. The gate oxide breaks down quickly after the drain avalanche breakdown. Fig. 5 shows the cross-section of the SEM photograph of the channel region after the gate oxide breakdown. From Fig. 5, we can see that the gate oxide has ruptured after the breakdown occurs. This kind of breakdown is destructive. So the reliability of the P-LDMOS will be greatly decreased. Ref. [6] showed that the hot-carrier effect was mainly caused by hot-carrier injection near the source region. From the analysis and the experimental results, one can see that it is very important to reduce the two electrical field peaks in the channel region so as to reduce the hot-carrier effect and improve the reliability of the P-LDMOS.

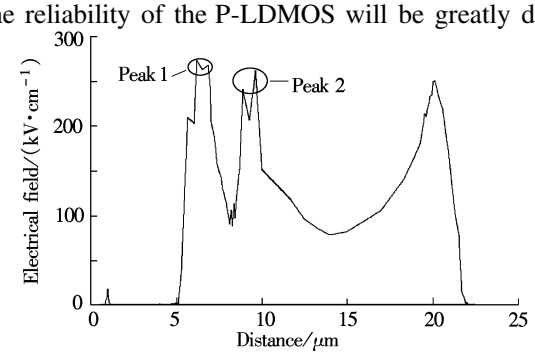

Fig. 3 Electrical field distribution along the Si-SiO_2 interface in the on-state of the initial P-LDMOS

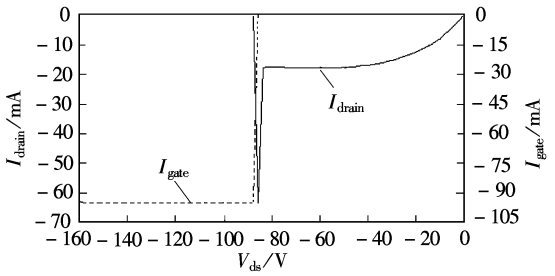

Fig. 4 Metrical currents of drain and gate vs. drain voltage in the on-state of the initial P-LDMOS

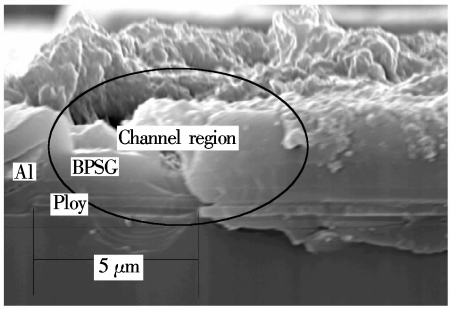

Fig. 5 Cross-section of SEM photograph of the channel region after the gate oxide breakdown

3 Methods

Fig. 6(a) shows the correlation between the two electrical field peaks in the channel region and the length of the channel. With the increase in the length of the channel, peak 2 (see Fig. 3) decreases because of the reduction in the resistance of the overlap region of the n-well and the p-drift, while peak 1 remains constant. Fig. 6(b) shows the correlation between the two electrical field peaks and the implanted doses of the n-well. With the decrease in the implanted doses of the n-well, peak 1 reduces because of the decrease of the n-well concentration at the P^+N^- junction near the source, while peak 2 remains constant.

According to the two methods, we can obtain the optimal high-voltage P-LDMOS, whose reliability is greater. The channel length and the implanted doses of the n-well of the optimized P-LDMOS are 7 μm and 5×10^{12} cm^{-2}, respectively. The electrical field distribution on the silicon side along the Si-SiO_2 interface in the on-state of the optimized P-LDMOS is shown in Fig. 7. Both of the electric field peaks decrease

compared with those of the initial device shown in Fig. 3. The breakdown voltage of the optimized P-LDMOS is higher than that of the initial device because of the lower hot-carrier effects, which can be seen in Fig. 8. Even if the drain breaks down, the gate oxide does not break down because the hot-carrier effect is greatly reduced. So the two electrical field peaks (peak 1 and peak 2 in Fig. 3), which are on the two sides of the channel region, can be reduced by lengthening the channel and lowering the implanted doses of n-well, respectively. From the experimental results, one can see that the proposed methods are very effective in reducing the two electrical field peaks resulting in a reduction of the hot-carrier effect and in improving the reliability of the high-voltage P-LDMOS.

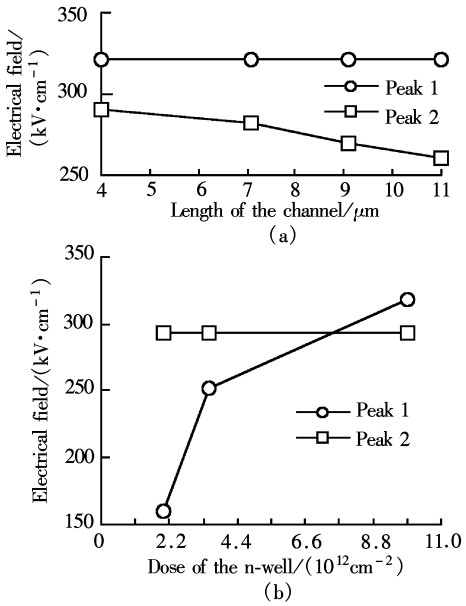

Fig. 6 Two electrical field peaks vs. P-LDMOS parameters. (a) Two electrical field peaks vs. the length of the channel; (b) Two electrical field peaks vs. the implanted doses of n-well

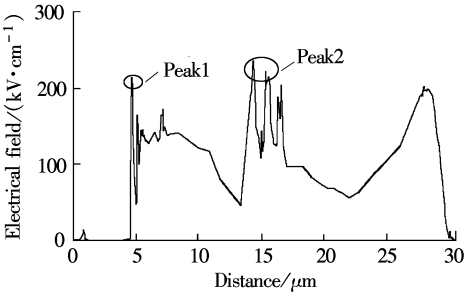

Fig. 7 Electrical field distribution in the silicon side along the Si-SiO_2 interface in the on-state of the optimized P-LDMOS

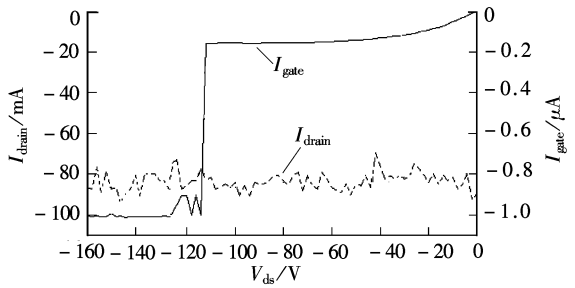

Fig. 8 Metrical currents of drain and gate vs. the drain voltage in the on-state of the optimized P-LDMOS

4 Conclusion

Improving the reliability of the high-voltage P-LDMOS is very important in enhancing the reliability of the HV-CMOS and the whole power ICs. From the research in this paper, one can see that the peak electrical field along the channel surface of the P-LDMOS can lessen the hot-carrier effect, so the reliability will be reduced. Optimizing the length of the channel and the concentration of the n-well were found to be two effective ways of reducing the two electrical field peaks. The values of peak 1 and peak 2 can be reduced by decreasing the concentration of the n-well and increasing the length of the channel, respectively. The simulation and experimental results indicate that the reliability of the P-LDMOS optimized by the proposed methods has been greatly improved.

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高压 P-LDMOS 的栅击穿及其改进方法

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摘要：高压 P-LDMOS 的失效实验分析表明其沟道区的高峰值电场会导致沟道区的热载流子效应，从而将降低高压 P-LDMOS 的可靠性. 借助半导体器件专业软件 Tsuprem-4 和 Medici 的模拟给出了高压 P-LDMOS 沟道区的电场分布情况，模拟结果显示在沟道区存在 2 个峰值电场，讨论了产生这 2 个峰值电场的原因，同时给出了降低这 2 种峰值电场的有效方法——适当增加沟道的长度和降低沟道区的浓度. 实验结果表明采用这 2 种方法优化得到的高压 P-LDMOS 的栅击穿电压得到了很大的提高，同时 P-LDMOS 的可靠性也得以大幅提高.

关键词：峰值电场；热载流子效应；可靠性

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