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Power consumption in a field emission panel

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Abstract: The power consumption and electric field distribution in a field emission display (FED) panel is optimized with a novel pixel structure. A circuit model is proposed to estimate the total power consumption in an FED panel which is composed of anode energy consumption, energy loss due to the leakage current and the energy dissipated in the parasitic capacitances. Moreover, the parasitic capacitances play a vital part in the power consumption and driving performance. In order to lower the parasitic capacitances, multiple dielectric layers are used as the gate electrode. Due to different etching speeds, a novel pixel structure is formed. As a result, the power consumption of an FED panel is reduced by 28% in a full white picture, and the electron beam performance is also better than that of the conventional structure.

Key words: field emission display; power consumption; circuit model

The field emission display (FED) panel has a high luminance efficiency, brightness and resolution. It has become a candidate for flat display panels in the future[1]. Much research, such as fabrication of the field emitters, improvement of the emission characteristics and focus of the electron beam has been done widely[2].

In this paper, the power consumption of an FED device has been studied. The power dissipation of an FED device is the electric power consumed in the capacitances and resistances, and will not transfer to the luminance energy. Normally in the design of an FED device, the emission characteristics and the performance of the electron beam are optimized. However, the power consumption is also very important in the design of an FED device. Furthermore, some parasitic capacitance effects play a vital part in the performance of an FED panel, such as leakage current, cross talk and line coupling effect. In this paper, the energy dissipation in an FED device is analyzed. A circuit model is proposed to estimate the power consumption. With this model, the triode structure is optimized to decrease the power consumption with a good electron beam performance.

1 Luminance Efficiency of an FED Panel

Luminance efficiency is an important parameter in the design of a display device. It can be expressed as[3]

$$\eta = \pi AL / P_{\text{total}} \tag{1}$$

where η is the luminance efficiency, A is the faceplate area of the display device, and L is the luminance in cd/m^2. In a field emission display device, the total power consumption P_{total} can be estimated as

$$P_{\text{total}} = P_{\text{anode}} + P_{\text{leak}} + P_{\text{diss}} \tag{2}$$

where P_{anode} is the energy consumption in the anode, P_{leak} is the energy loss due to the leakage current, and P_{diss} is the energy dissipated in the capacitances between different electrodes.

As shown in Fig. 1, the electrons are emitted from the cold cathode, accelerated by the electric field and bombarded on the phosphor screen. The energy of the electron beam is transmitted from the electrons to the phosphor. Therefore, P_{anode} can be estimated as[4]

$$P_{\text{anode}} = I_{\text{anode}} V_{\text{anode}} \tag{3}$$

where I_{anode} is the current landing on the anode, and V_{anode} is the voltage of the anode. As shown in Fig. 1, a dielectric layer has been fabricated between the cathode plate and the gate electrode. Because the resistance of the dielectric layer is not infinite, leakage current may be generated along the dielectric layer. The power dissipation generated by the leakage current can be expressed as

$$P_{\text{leak}} = I_{\text{leak}} V_{\text{gc}} \tag{4}$$

where I_{leak} represents the current leakage to the gate

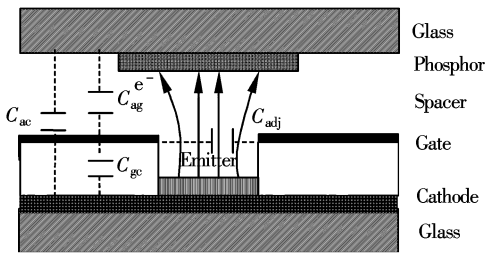

Fig. 1 A triode structure of FED

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through the dielectric layer, and V_{gc} is the gate voltage over the cathode.

In Fig. 1, C_{ac}, C_{ag} and C_{cg} represent capacitances between the cathode, the gate electrode and the anode, respectively . When the video image is displayed on an FED panel, normally the scanning voltage signal is applied on the gate electrode while the data voltage signal is applied on the cathode electrode. During the scanning process, the capacitances C_{ac}, C_{ag} and C_{cg} are charging and discharging periodically.

As shown in Eq. (2), a part of energy is stored and wasted in these capacitances, only the energy P_{anode} can be transferred to the phosphor layer. Thus, the power dissipation P_{leak} and P_{diss} should be controlled in the design of an FED device.

2 Power Dissipation in a Triode Structure

The basic triode structure has been given in Fig. 1. A driving voltage is applied on the gate electrode. Due to the high electric field over the cathode, the electrons are emitted from the field emitter. A high voltage has been applied on the anode, so that the electrons are accelerated and bombarded on the anode with high energy. To decrease the driving voltage, the distance between the cathode and the gate is often very small in design.

To evaluate the power consumption in a triode structure of an FED device, a circuit model shown in Fig. 2 has been proposed. Where C_{adj} is the capacitance between the adjacent gates; I_{ag}, I_{gc} and I_{leak} are the leakage currents corresponding to C_{ag}, C_{gc} and C_{ac}. P_{leak} is largely influenced by the resistance of the emitter and electrodes (R_e), and should be carefully kept low. Because the value of resistance determines how much electric power is transferred to the thermal energy in columns, a high value of resistance causes excessive voltage drop along the same column of the emitter. It will do harm to uniformity of the entire panel.

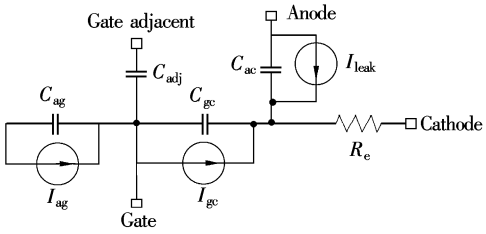

Fig. 2 Circuit model of a triode structure

In the case of the pulse width modulation (PWM) driving method[5], the parasitic capacitances continually charge and discharge. When a certain pixel is selected by the driving circuit, the electric energy is temporarily stored in the capacitances in the charging process. But the capacitances will immediately discharge when this pixel is off. A part of electric energy is lost during the charging and discharging processes when the currents pass through the resistances, which are shown in Fig. 2. In the charging process, when the leakage current goes through the resistance R_e also shown in Fig. 2, some electric energy will be lost in those resistances. And some part will be stored in the capacitances. Then in the discharging process, the electrons which are stored in the capacitances will decrease from Q to 0. At the same time, the voltage decreases from V to 0. So the energy dissipated in the resistance in the charging process can be calculated as

$$W_{charge} = I^2 R \tag{5}$$

And for the discharging process,

$$|W_{discharge}| = \left|\int_Q^0 v\mathrm{d}q\right| = \left|\int_Q^0 \frac{1}{C} q\mathrm{d}q\right| = \frac{1}{2}\frac{Q^2}{C} = \frac{1}{2}V^2 C \tag{6}$$

Assuming the frequency is f, the power dissipated in a whole charging and discharging process is

$$P = f\left(I^2 R + \frac{1}{2}V^2 C\right) \tag{7}$$

According to the circuit model shown in Fig. 2, the capacitive dissipation in a normal gate FED is given as

$$P_{diss} = P_{gc} + P_{ga} + P_{adj} \tag{8}$$

These three parts of power dissipation are donated by three kinds of capacitances. In the first place there are capacitances between the gate electrodes and the cathode plate (C_{gc}). Every gate electrode will be selected once per frame, so the total dissipations due to C_{gc} in the discharging process are

$$P_{gc} = \frac{1}{2} f N_{pix} V_{swing}^2 C_{gc} \tag{9}$$

where V_{swing} is the voltage difference between the pull on voltage and the pull off voltage, and N_{pix} is the number of pixels. The next important capacitance is between adjacent columns on the gate plate, which is represented by C_{adj}. These two capacitances are subjected to the voltage V_{swing}. These capacitances will also be charged and discharged once for each row during every display period, so the capacitive power dissipations in the discharging process become

$$P_{adj} = \frac{1}{2} f N_{pix} V_{swing}^2 C_{adj} \tag{10}$$

There are also capacitances C_{ga} (between the gate and the anode) and the C_{ca} (between the cathode and the anode). In approximation, the power dissipated in these two capacitances (P_{AC}) in the discharging process can be estimated as

$$P_{AC} = P_{ga} + P_{ca} = \frac{1}{2} f N_{pix} V_{anode}^2 (C_{ga} + C_{ca}) \quad (11)$$

Summing all the contributions yields the capacitance dissipations in the normal gate FED,

$$P_{diss} = P_{gc} + P_{adj} + P_{AC} = \frac{1}{2} f N_{pix} [V_{swing}^2 (C_{gc} + C_{adj}) + V_{anode}^2 (C_{ga} + C_{ca})] + (I_{ag}^2 + I_{gc}^2 + I_{leak}^2) R_e \quad (12)$$

Furthermore, the total power consumption can be estimated as

$$P_{total} = I_{anode} V_{anode} + I_{leak} V_{gc} + \frac{1}{2} f N_{pix} [V_{swing}^2 (C_{gc} + C_{adj}) + V_{anode}^2 (C_{ga} + C_{ca})] + (I_{ag}^2 + I_{gc}^2 + I_{leak}^2) R_e \quad (13)$$

The capacitances C_{ga} and C_{ca} are very small compared with the other two capacitances, so they can be ignored when we explore the power dissipation due to them[6]. P_{total} can be roughly given as

$$P_{total} \cong I_{anode} V_{anode} + I_{leak} V_{gc} + (I_{ag}^2 + I_{gc}^2 + I_{leak}^2) R_e + \frac{1}{2} f N_{pix} [V_{swing}^2 (C_{gc} + C_{adj})] \quad (14)$$

From Eq. (14), it can be concluded that reducing the parasitic capacitance is one of the ways of decreasing the power dissipation.

3 Triode Structure with Low C_{gc}

According to Eq. (14), the capacitance C_{gc} has to be decreased to reduce the power dissipation. Normally, the holes in the dielectric layer are etched. The modified triode structure with low C_{gc} is shown in Fig. 3.

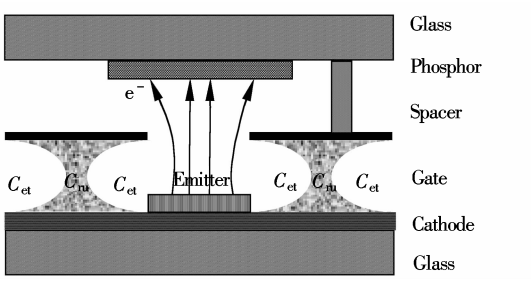

Fig. 3 Section view of the modified triode structure with low C_{gc}

If a set of sub-layers with different dielectric materials are fabricated between the cathode and the gate electrode, the etching speeds for different sub-layers are not the same. The structure shown in Fig. 4 can be obtained.

The capacitance of the etching part is C_{et}, and that of the rudimental part is C_{ru}. These two parts are connected in parallel with each other, so it can be easily concluded that $C_{gc} = C_{et} + C_{ru}$. For this modified structure, C_{et} becomes 0. As a result, C_{gc} reduces and so does the power dissipation of the parasitic capacitance. The capacitances in Fig. 1 and Fig. 3 are numerically calculated respectively. Fig. 4 and Fig. 5 give the distributions of the electric field. Tab. 1 indicates the comparative results of the capacitances between the cathode and the gate with different structures.

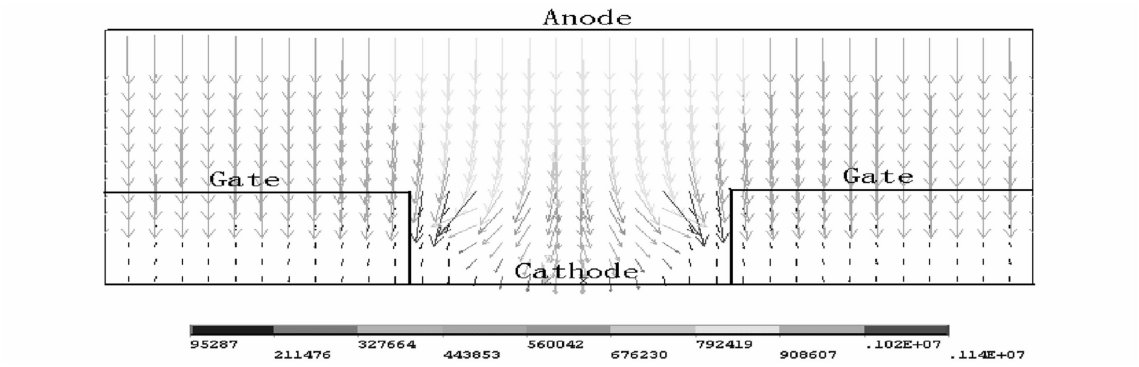

Fig. 4 Electric field distribution of the former structure

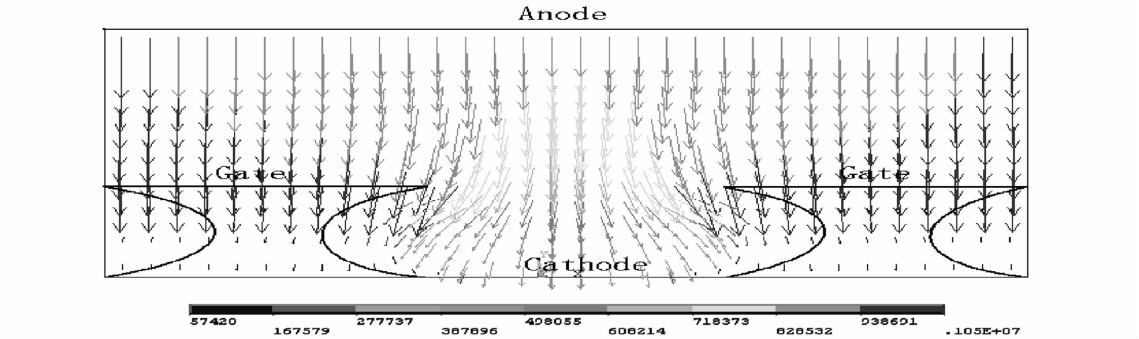

Fig. 5 Electric field distribution of the modified structure

Tab. 1 Capacitances between the electrodes in a pixel

Relative permittivity ε	C_{gc} (former structure)/pF	C'_{gc} (modified structure)/pF
10	0.843 39	0.692 80
7	0.593 16	0.492 63
4	0.342 85	0.249 45

As shown in Tab. 1, the capacitance C_{gc} in Fig. 3 is smaller than that in Fig. 1. Take the XGA FED panel as an example. 28% power dissipation can be saved by the modified structure in a full white picture ($\varepsilon = 10$).

4 Conclusion

We studied the power consumption in a triode structure FED by a circuit model. Especially, the power dissipation in the parasitic capacitance which distorts the image display was carefully examined. We found the relationship between C_{gc} and power dissipation. In order to get lower power dissipation, a modified structure with low C_{gc} was proposed. As a result, this modified structure does not only decrease 28% power dissipation ($\varepsilon = 10$) as compared with the former structure, but it also has a good electron beam performance. The FED panel with low power dissipation increases the luminance efficiency. The lifetime of the FED panel is also prolonged.

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场发射显示器能量消耗研究

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摘要:为了降低场发射显示器的能量消耗,提出一种新型的像素点结构,并优化了其内部电场分布.基于此结构建立了一个电路模型,得到显示屏功耗的3个主要组成部分:阳极功耗、漏电流损耗和寄生电容能量损耗.其中寄生电容的存在不但会影响驱动电路性能,而且会增加显示屏的功耗.另外,利用多种绝缘层不同的腐蚀速度,得到了新型像素点结构,减小了显示屏的寄生电容,使得其功耗比传统结构减小了28%,并且发射电场分布也优于传统像素点结构.

关键词:场发射显示;能量消耗;电路模型

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