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2.488 Gbit/s clock and data recovery circuit in 0.35 μm CMOS

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Abstract: The design of a 2.488 Gbit/s clock and data recovery (CDR) IC for synchronous digital hierarchy (SDH) STM-16 receiver is described. Based on the injected phase-locked loop (IPLL) and D-flip flop architectures, the CDR IC was implemented in a standard 0.35 μm complementary metal-oxide-semiconductor (CMOS) technology. With $2^{31}-1$ pseudorandom bit sequences (PRBS) input, the sensitivity of data recovery circuit is less than 20 mV with 10^{-12} bit error rate (BER). The recovered clock shows a root mean square (rms) jitter of 2.8 ps and a phase noise of −110 dBc/Hz at 100 kHz offset. The capture range of the circuit is larger than 40 MHz. With a 5 V supply, the circuit consumes 680 mW and the chip area is 1.49 mm × 1 mm.

Key words: clock recovery; data recovery; phase-locked loop (PLL); preprocessor

The clock and data recovery (CDR) circuit is one of the core cells in a receiver. Its main functions are to extract the clock from the data stream, to reshape and retime it. As reported, 2.488 Gbit/s CDR ICs have been realized in different Si-bipolar processes[1-4], 0.25 μm CMOS[5] and 0.4 μm CMOS[6], respectively. Adopting the Si-bipolar technology, the CDR ICs have small root mean square (rms) jitters when an external reference clock is used[1,3]. Otherwise the rms jitter is large[2,4]. Moreover, the CDR ICs in Si-bipolar have large die sizes[3-4]. Despite the small chip areas, the CDR ICs in CMOS have large rms jitters[5-6]. In this paper, a 2.488 Gbit/s CDR in 0.35 μm CMOS is presented. It does not use a reference clock but shows an rms jitter of only 2.8 ps and the chip area is only 1.49 mm^2.

1 Circuit Design

The block diagram of the CDR IC is shown in Fig. 1. As shown in the dashed regions, it is composed of a preprocessor, an injected phase-locked loop (IPLL) and a data decision.

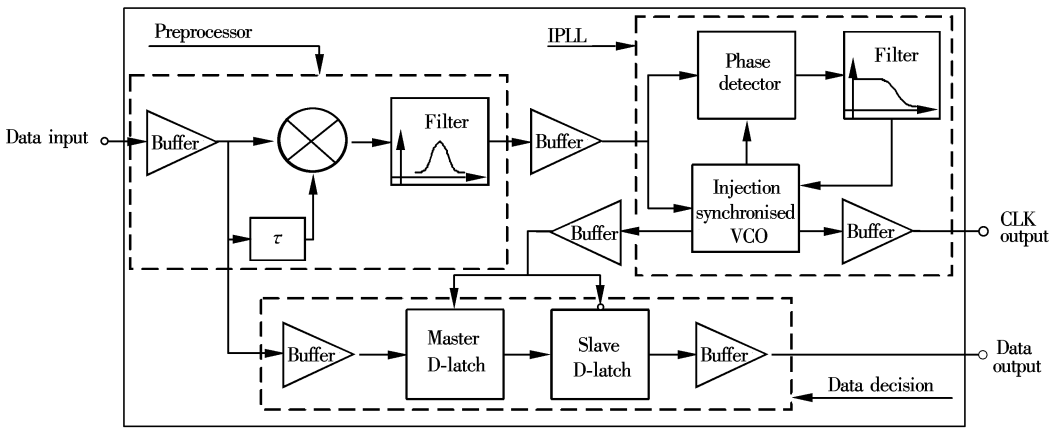

Fig. 1 Block diagram of CDR

The preprocessor includes an input buffer, a delay cell, a multiplicator and a narrow-band filter. The delay cell constructed with a few of wide-band buffers can give an approximately $T/2$ delay with T representing the data period. Under optimal conditions, the multiplicator's differential outputs have no direct current (DC) point difference. With the variation in the temperature, the process and the supply voltage, the delay time will not equal $T/2$ absolutely and the DC point difference may occur. In order to avoid this problem, the traditional multiplicator with a tank circuit as load used in the preprocessor is separated into a multiplicator with resistor load and a narrow-band filter with block capacitors at input terminals. The schematics of the filter is shown in Fig. 2. For lack of

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inductor modeling, the active inductor proposed in Ref. [7] is adopted to construct the LC tank circuit with acceptable noise contribution.

The dashed regions in Fig. 2 indicate the two symmetrical active inductors. Utilizing the small signal model of the metal oxide semiconductor field effect transistor (MOSFET) shown in Fig. 3(a), the small signal equivalent circuit of the active inductor can be drawn as in Fig. 3(b).

Ignoring the effect of R_{ds}, the input impedance of the circuit in Fig. 3(b) can be simplified into a parallel RLC circuit, whose values are calculated as

$$R_{eq}=\frac{(C_1+C_2)(g_{m1}+g_{m3})^2}{g_{m2}(g_{m1}+g_{m3})^2C_2+g_{m1}^2g_{m2}C_4-g_{m1}g_{m2}g_{m3}C_{gs1}-g_{m1}g_{m3}(g_{m1}+g_{m3})C_2}$$

$$C_{eq}=\left(\frac{C_1C_2}{C_1+C_2}+C_3\right)+\frac{g_{m1}}{g_{m1}+g_{m3}}C_4+\frac{C_2}{C_1+C_2}\frac{C_4g_{m1}^2-g_{m1}g_{m3}C_{gs1}}{(g_{m1}+g_{m3})^2},\quad L_{eq}=\frac{C_1+C_2}{g_{m1}g_{m2}}\frac{g_{m1}+g_{m3}}{g_{m3}}$$

with

$$C_1=C_{gs2}+C_{gd1},\quad C_2=C_{gd2}+C_{db1},\quad C_3=C_{sb2}+C_{gd3}+C_{db3},\quad C_4=C_{sb1}+C_{sb3}+C_{gs3}$$

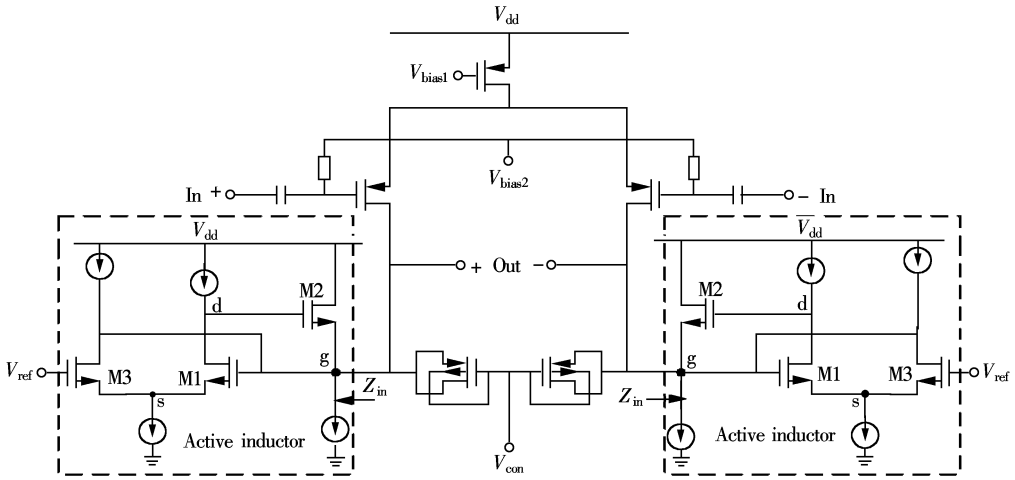


Fig. 2 Schematic of the narrow-band filter

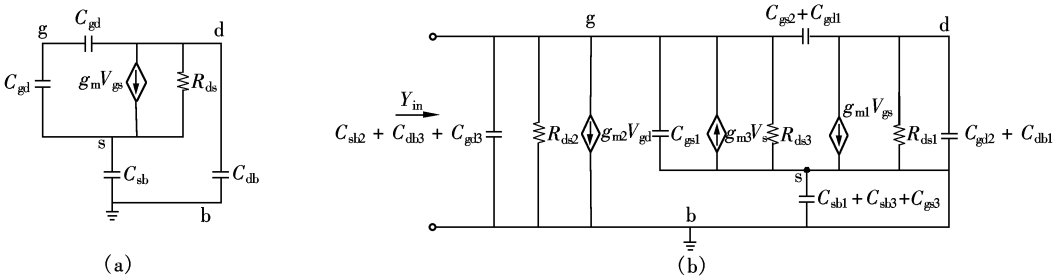


Fig. 3 MOSFET and active inductor equivalent circuit. (a) Small signal model of a MOSFET; (b) Small signal equivalent circuit of the active inductor

Although a tradeoff has to be made between the Q factor of the inductor and the bandwidth of the filter, a properly high Q factor of the active inductor can be obtained. The narrow-band filter shown in Fig. 2 will have sufficient Q factor on condition that the Q factor of the varactor is not worse than that of the inductor. The varactor shown in Fig. 2 can enhance the equivalent resistor in parallel, consequently enhancing the Q factor of the varactor.

The IPLL is composed of a phase detector (PD), a low-passed filter (LPF) and an injection synchronized voltage-controlled oscillator (SO). Although the loop bandwidth of the IPLL should be smaller than 2 MHz, the injection of the clock from the preprocessor to the SO can guarantee the loop stability with no need of an additional loop, such as a loop including a frequency detector. And this injection can shorten the capture process of the loop.

Fig. 4 shows the diagram of the PD and the LPF. The PD consists of a multiplicator, an amplifier and a 2∶1 converter.

The amplifier following the multiplicator is aimed to enhance the gain of the PD and to compensate the gain loss caused by the 2∶1 conversion. The

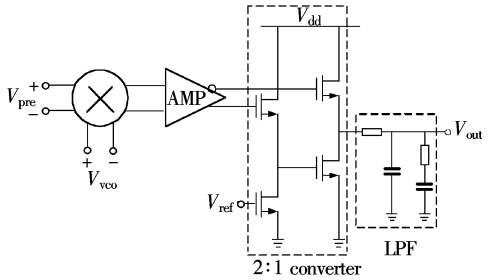


Fig. 4 Phase detector and low-passed filter

2:1 converter consists of a source follower and a push-pull output stage. Compared to the traditional 2:1 converter constructed by a differential amplifier with MOSFET loads, the converter shown in Fig. 4 is very flexible in adjusting the output operating point and the linearity of the PD by optimizing the parameters of the MOSFETs. In comparison to the single-end signal, the gain of the converter is greater than one, and sufficient gain can be achieved together with the foregoing amplifier. In addition, the reference port of the converter is designed as an off-chip terminal so as to adjust the output operating point of the PD. Consequently, the oscillating frequency of the SO can be controlled off-chip. Moreover, this reference port provides an alternative avenue for another loop's control in further application.

The SO is of the ring type and consists of an adder, three narrow-band amplifiers as delay stages and an output buffer. The block diagram is shown in Fig. 5 (a). The SO itself is a loop and the phase of the output signal can be adjusted accommodated to the injected signal automatically. The ring architecture including an adder is necessary to establish this controllable

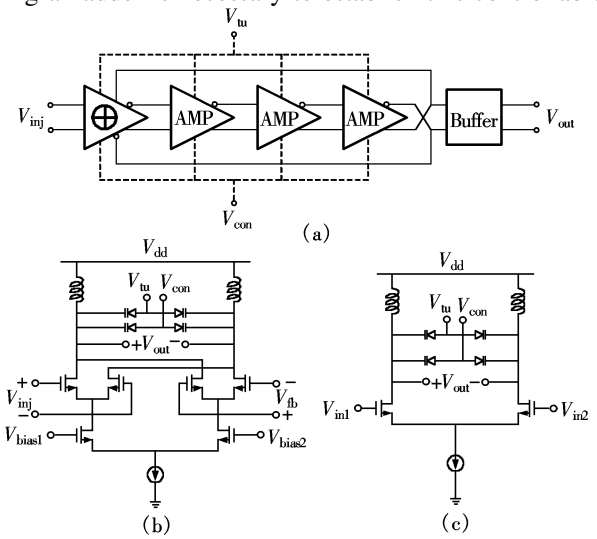


Fig. 5 SO circuit. (a) Block diagram of the SO; (b) Adder; (c) Narrow-band amplifier

phase relationship. The adder and the delay stage are shown in Figs. 5(b) and (c), respectively. In considering the phase noise, a spiral metal inductor is utilized in the SO and the physical simulation is accomplished by the advanced design system (ADS) momentum.

The data decision circuit can form the recovered data through twice alternant sampling by the recovered clock. The circuit consists of classical D-flip flops made of master-slave latches. Fig. 6 is the schematic of one latch. The layout of the latch should be designed carefully to guarantee its symmetry. For the presence of the static phase error in a phase-locked loop (PLL), the phase of the recovered clock may vary according to the environment, resulting in a reduction of the circuit's operating range. To minimize this influence, the delay of the clock or the data signal should be optimized to make the clock sample at the center of the data initially.

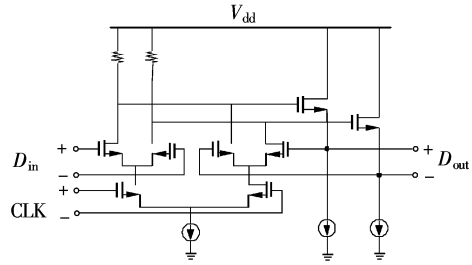


Fig. 6 Latch

2 Measured Results

The CDR IC has been fabricated in a standard 0.35 μm CMOS technology. Fig. 7 is the chip microphotograph and the chip area is 1.49 mm × 1 mm, consuming 680 mW with a 5 V supply.

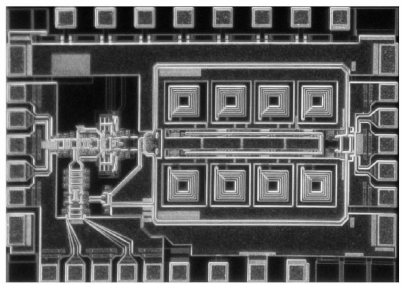


Fig. 7 Chip microphotograph

Fig. 8 displays the measured oscillation frequencies of the SO as a function of the controlling voltage. The tuning range is more than 200 MHz with a satisfactory linearity.

With a 2.488 Gbit/s $2^{31}-1$ pseudorandom bit

sequences (PRBS) input signal, of which the single-ended peak to peak value is 20 mV, the chip achieves a capture range of more than 40 MHz. The spectrum of the recovered clock is presented in Fig. 9 and the phase noise is −110 dBc/Hz at 100 kHz offset.

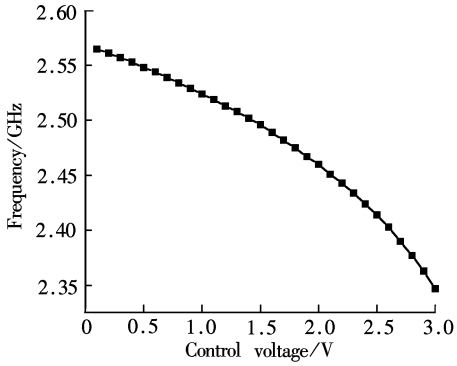
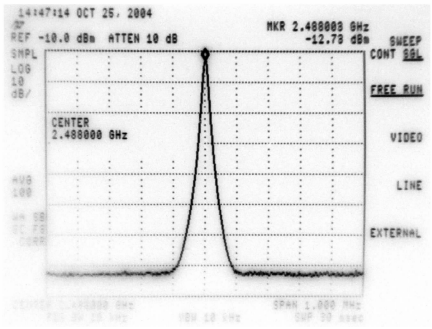


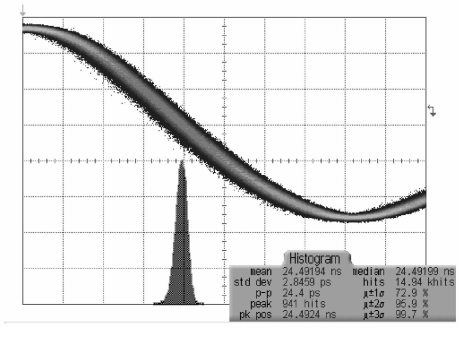
Fig. 8 Measured oscillation frequency vs. control voltage



SPAN = 1 MHz, RES BW = 10 kHz

Fig. 9 Spectrum of the recovered clock

In Fig. 10, the jitter histogram of the clock is shown, indicating the rms and peak-peak values of 2.8 ps and 24 ps, respectively. This jitter performance meets the ITU-T recommendation of 4 ps rms and 40 ps peak-peak.

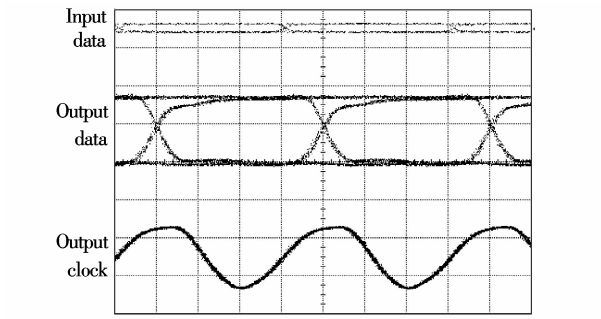


30 mV/div, 20 ps/div

Fig. 10 Jitter histogram of recovered clock

On-chip measurement results show that the sensitivity is less than 20 mV with 10^{-12} BER at the bit rate of 2.488 Gbit/s. The sensitivity value is the peak to peak value of single-ended input signals. The input and output eye diagrams are shown in Fig. 11 together with the recovered clock.

The detailed performance of the chip is summarized in Tab. 1.



100 mV/div, 100 ps/div

Fig. 11 Input/output eye diagrams and recovered clock

Tab. 1 Summarized performance of the CDR

Supply voltage/V	5
Power consumption/mW	680
Sensitivity/mV	<20 (BER $=10^{-12}$)
BER	$<10^{-12}$ (single $V_{p\text{-}p}=20$ mV)
Clock jitter	2.8 ps rms, 24 ps peak-peak
Phase noise	−110 dBc/Hz@100 kHz
Capture range/MHz	40

3 Conclusion

Using a standard 0.35 μm CMOS technology, a monolithically-integrated CDR IC was fabricated for applications at 2.488 Gbit/s. The experimental results summarized in Tab. 1 indicate that the chip is suitable for SDH communication standard STM-16.

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2. 488 Gbit/s 0. 35 μm CMOS 时钟和数据恢复电路

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摘要:描述了用于 SDH 光纤通信 STM-16 速率级的 2. 488 Gbit/s 时钟和数据恢复电路. 该电路采用基于注入式锁相环和 D 触发器的电路结构,在标准的 0. 35 μm CMOS 工艺上实现流片. 经过测试,当输入长度为 $2^{31}-1$ 的伪随机序列,数据速率为 2. 488 Gbit/s 时,在误码率为 10^{-12} 的条件下,电路的灵敏度小于 20 mV. 恢复得到的时钟具有 2. 8 ps 的均方根相位抖动,在 100 kHz 频偏处的相位噪声为 -110 dBc/Hz,并具有大于 40 MHz 的捕获范围. 5 V 电源供电时,电路消耗 680 mW 功率. 芯片面积为 1. 49 mm × 1 mm.

关键词:时钟恢复;数据恢复;锁相环;预处理器

中图分类号:TN402;TN492