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Capacitor self-calibration technique used in time-interleaved successive approximation ADC

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Abstract: A capacitor self-calibration circuit used in a successive approximation analog-to-digital converter (SA-ADC) is presented. This capacitor self-calibration circuit can calibrate erroneous data and work with the ADC by adding an additional clock period. This circuit is used in a 10 bit 32 Msample/s time-interleaved SA-ADC. The chip is implemented with Chart 0.25 μm 2.5 V process and totally occupies an area of 1.4 mm × 1.3 mm. After calibration, the simulated signal-to-noise ratio (SNR) is 59.586 1dB and the spurious-free dynamic range (SFDR) is 70.246 dB at 32 MHz. The measured signal-to-noise and distortion ratio (SINAD) is 44.82 dB and the SFDR is 63.760 4 dB when the ADC samples a 5.8 MHz sinusoid wave.

Key words: capacitor self-calibration; analog-to-digital converter; successive approximation; time-interleaved

The single channel successive approximation analog-to-digital converter (SA-ADC) is a structure providing up to 5 Msample/s sample rate with a resolution of 8 to 16 bits. However, it does not satisfy the need for higher sampling rate applications. The time-interleaved structure is often introduced[1] in such applications. It is found that when M SA-ADCs work in parallel and sample the signal time-interleavedly, the effective overall sampling rate can be multiplied by M. Nonetheless, this type of ADC suffers from offset, gain and sampling timing (jitters and skew) mismatches between the channels[2-3].

The digital-to-analog converter (DAC) is one of the constituent parts used in the SA-ADC, which deposits the numerical quantity conversion within the registers and converges on the analog signal input. It can greatly influence the accuracy of the ADC. For charge scaling DAC, the capacitor matching is important. The mismatches will degrade the performance of time-interleaved SA-ADC greatly including spurious-free dynamic range (SFDR) and signal-to-noise ratio (SNR). There are many ways to calibrate the capacitor mismatches. Laser trimming can guarantee the resolution but it is an expensive and time-consuming procedure. Ref. [4] adopted a sub-capacitor array to calibrate the errors in the capacitor array. However, this method is limited by the parasitics and offsets of the sub-capacitor array itself. It also increases the capacitance load of the input signal. Leung et al.[5] merged big capacity from the smaller capacitors in series. The calibration is based on adding or removing the small capacitors to get a good match in the array. But it provides only a resolution of 1/8 of the unit capacitance value C and makes the design of the layout more difficult. Ref. [6] adopted the algorithm presented in Ref. [7], but the test results did not prove 16 bits accuracy. Besides, the calibration occurs on power-up and cannot calibrate the errors arising during the conversion.

A capacitor self-calibration circuit is proposed in this paper. It can run parallel with the ADC by adding an additional calibration clock period, and calibrate the offset mismatches produced during each ADC conversion cycle. A pseudo-differential input is adopted to cancel the switch channel charge injection and clock feed-through.

1 Capacitor Self-Calibration

The common structure of DAC includes voltage scaling, R-2R voltage scaling, and charge scaling DAC etc. Because of the resistance of the MOS switch in the first two kinds of DACs, the resistor network cannot have correct values thus introduce conversion errors. As for charge scaling DAC, the total capacitor value will become hard to accept since it will rise exponentially with the bit number of resolution. A structure of voltage-charge scaling is used in this circuit and avoids large values of resistors or capacitors. The DAC used in each channel is realized in an economically feasible size, which ensures a great die size saving in a time-interleaved structure as shown in Fig. 1. DA1(R) and DA2(R) are controlled by bit1 to bit4 and bit5 to bit9 of the ADC, respectively. The lower bit10 and bit11 control DA3(R) and DA4(R).

Taking no account of the capacitor calibration module in the dash frame, the analog signals A_{in} and

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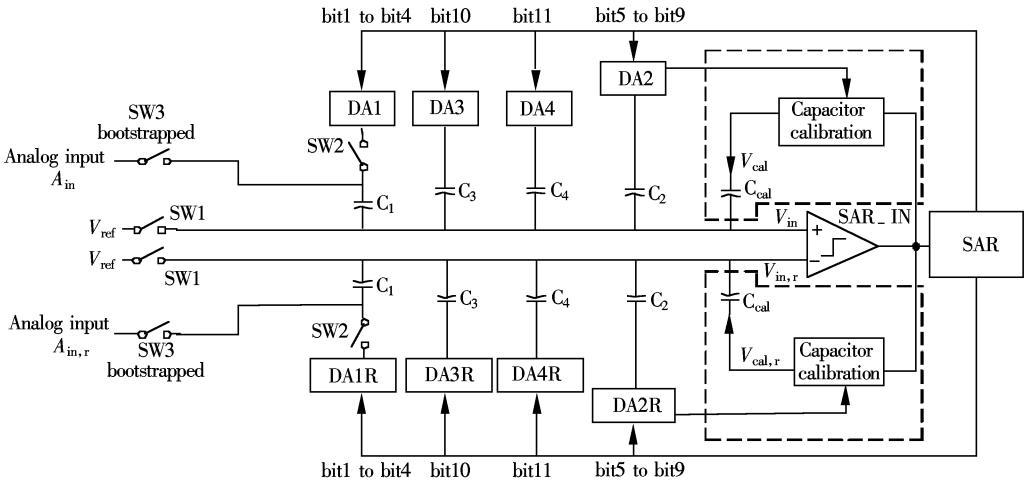

Fig. 1 Architecture of one SA-ADC cell

$A_{in,r}$ first pass through the bootstrapped switches SW3 and SW1, and charge the sampling capacitor C_1. Then the transmission gates SW3 and SW1 are disconnected from C_1, and transmission gate SW2 is turned on at the same time. After a period of settling time, the voltages at V_{in} and $V_{in,r}$ are

$$V_{in} = V_{ref} + (V_{DA1} - A_{in})\frac{C_1}{C_{sum}} + V_{DA2}\frac{C_2}{C_{sum}} + V_{DA3}\frac{C_3}{C_{sum}} + V_{DA4}\frac{C_4}{C_{sum}} \quad (1)$$

$$V_{in,r} = V_{ref} + (V_{DA1R} - A_{in,r})\frac{C_1}{C_{sum}} + V_{DA2R}\frac{C_2}{C_{sum}} + V_{DA3R}\frac{C_3}{C_{sum}} + V_{DA4R}\frac{C_4}{C_{sum}} \quad (2)$$

where $C_{sum} = C_1 + C_2 + C_3 + C_4$.

And the voltage between V_{in} and $V_{in,r}$ is

$$V_{in} - V_{in,r} = [(V_{DA1} - V_{DA1R}) - (A_{in} - A_{in,r})]\frac{C_1}{C_{sum}} + (V_{DA2} - V_{DA2R})\frac{C_2}{C_{sum}} + (V_{DA3} - V_{DA3R})\cdot\frac{C_3}{C_{sum}} + (V_{DA4} - V_{DA4R})\frac{C_4}{C_{sum}} \quad (3)$$

The ADC implements the successive approximation binary search algorithm according to Eq. (3). So the accuracy of the ADCs is mainly determined by the matching of capacitors in the array. However, the accuracy of the capacitors is limited by the process variations and layout geometry errors which make calibration necessary.

Except for the mismatches of comparators, the deviation in the capacitor array will degrade the ADC resolution greatly. The capacitors C_1 and C_2 of the most weight are the main factors in ADC resolution. The ADC which uses the capacitor calibration has 11 digital outputs. Bit1 is the most significant bit (MSB) and the weight is $\frac{1}{2}V_{FS}$. The weights of the other bits are decreased by a factor of two except for bit6 and bit7 which are both $\frac{1}{64}V_{FS}$. Bit11 is the least significant bit (LSB) which equals $\frac{1}{1\,024}V_{FS}$. $V_{FS}$is the full-scale voltage of the ADC input.

If there is neither mismatch nor offset between the weighted capacitors, the weight of bit4 is $\frac{1}{16}V_{FS}$, and the sum of bit5 to bit7 equals $\frac{1}{32}V_{FS} + \frac{1}{64}V_{FS} + \frac{1}{64}V_{FS} = \frac{1}{16}V_{FS}$. During the calibration, bit4 of DA1 switches from 1 to 0 while bit5 to bit7 of DA2 switches from 0 to 1. The net change on V_{in} and $V_{in,r}$ should be zero after these changes. The output of the auto-zeroed comparator can be 1 or 0 of all rate equalities. But when there is any mismatch among the capacitors, the voltages $V_{in}$and $V_{in,r}$ cannot be equal, and the output of the comparator would be stable at 1 or 0. At this time, the calibration module in the dash frame in Fig. 1 will calibrate the mismatch between C_1 and C_2 through the calibration capacitor C_{cal}, and this adjustment will continue through several calibration cycles until the net change value of bit4 and bit5 to bit7 at V_{in} and $V_{in,r}$ comes to zero. And a linear differential attenuator shown in Fig. 2 is proposed to compensate for the slight capacitor mismatches between the arbitrary output of DA1 and DA2.

The voltage weights of DA1-4(R) are $\frac{1}{16}V_{FS}$, $\frac{1}{64}V_{FS}$, $\frac{1}{32}V_{FS}$, $\frac{1}{64}V_{FS}$, respectively. The capacitors C_1, C_2, C_3, C_4, C_{cal} have values of $16C$, $4C$, C, C and C. Considering the calibration module, rewrite Eq. (3) as

$$V_{in} - V_{in,r} = \left[\sum_{1}^{4} D_i 2^{4-i}\frac{1}{16}V_{FS} - (A_{in} - A_{in,r})\right]\frac{C_1}{C_{sum}} +$$

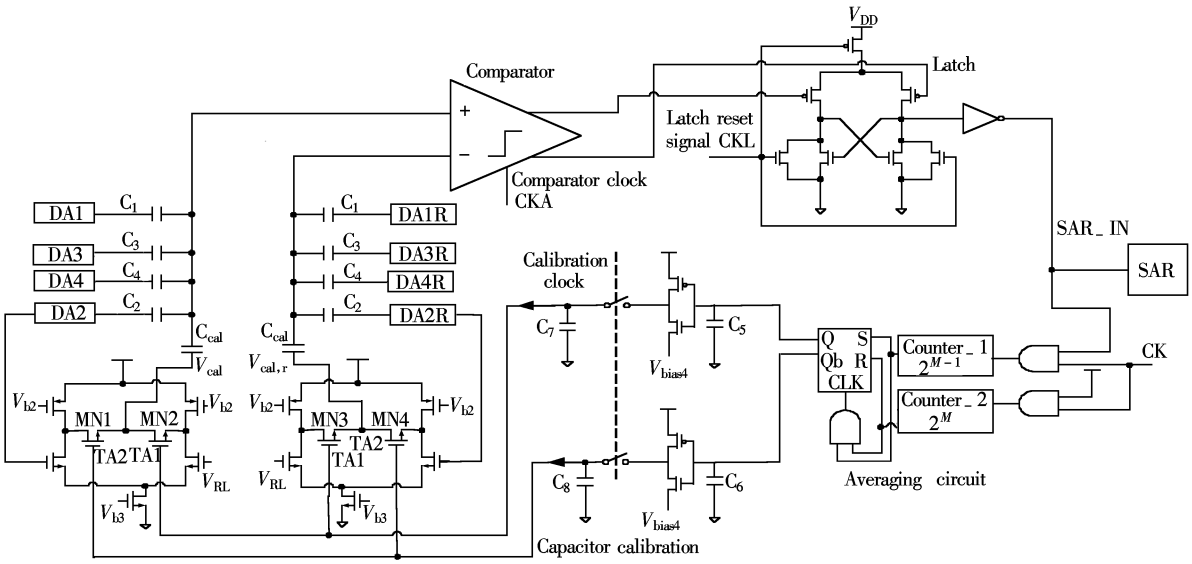

Fig. 2 Circuit of capacitor calibration

$$\left(\sum_{1}^{5} D_{i+4}2^{4-i}\frac{1}{64}V_{FS}\right)\frac{C_2}{C_{sum}} + \left(D_{10}\frac{1}{32}V_{FS}\right)\frac{C_3}{C_{sum}} + \left(D_{11}\frac{1}{64}V_{FS}\right)\frac{C_4}{C_{sum}} + (V_{cal} - V_{cal,r})\frac{C_{cal}}{C_{sum}} = \left[\left(\sum_{1}^{4} D_i 2^{4-i}\frac{1}{16}V_{FS} + \sum_{1}^{5} D_{i+4}2^{4-i}\frac{1}{256}V_{FS} + D_{10}\frac{1}{512}V_{FS} + D_{11}\frac{1}{1\,024}V_{FS}\right) - (A_{in} - A_{in,r})\right]\frac{16}{23} + (V_{cal} - V_{cal,r})\frac{1}{23} \quad (4)$$

where D_i is the digital output of bit i; D_7, D_8, D_9 represent 2^2, 2^1, 2^0, respectively and $C_{sum} = C_1 + C_2 + C_3 + C_4 + C_{cal} = 23C$.

When the ADC works, the digital outputs approximate the analog input of $(A_{in} - A_{in,r})$ by setting the bit1 to bit11 to one or zero. These are controlled by a successive approximation register (SAR). The term $(V_{cal} - V_{cal,r})\frac{1}{23}$ is used to calibrate the mismatches between C_1 and C_2. The architecture is shown in Fig. 2.

The capacitor C_7 and C_8 will be charged or discharged according to the result of the voltage at the node SAR_IN so as to control the potential at TA1 and TA2. An averaging circuit is included. Counter_2 has a period of 2^M ($M = 4$ in this case) clocks. Counter_1, which counts only when the comparator output SAR_IN is high, has a period of 2^{M-1} cycles. Both of the counters average the number of highs and lows, store the results in an RS flip-flop, and pass it on to the C_5 and C_6. MN1 to MN4 controlled by TA1 and TA2 work at the deep triode region just like controlled resistors and thus the gain of differential amplifier A_v will be low. The calibration signal V_{cal} and $V_{cal,r}$ is a linear of the summation of the potentials at TA1 and TA2 which depends on the resistance ratio among MN1 to MN4:

$$V_{cal} = V_{DA2}A_V\frac{R_{MN1}}{R_{MN1} + R_{MN2}} \quad (5)$$

$$V_{cal,r} = V_{DA2R}A_V\frac{R_{MN3}}{R_{MN3} + R_{MN4}} \quad (6)$$

So we can calibrate the mismatches between C_1 and C_2 by generating the controlled potential of the calibration capacitor C_{cal}. To guarantee the calibrated voltage beyond the threshold voltage of MN1 to MN4, the signal V_{bias4} is 1 V, instead of ground potential.

If there is no mismatch, the end voltage of TA1 and TA2 is about 1.75 V. The voltage step between each calibration process is 70 μV, which equals a 14 bit resolution. Therefore, the voltage adjustment each time is small and it takes a long time for the accurate adjustment of C_1 and C_2.

2 Structure of Time-Interleaved ADC

The calibration module is used in a 10 bit 32 Msample/s SA-ADC (see Fig. 3). The design consists of 16 identical SA-ADC sections, all operating time-interleavedly, a 16-phase clock generator, a 16∶1 digital output multiplexer (MUX), and a voltage reference generator that provides common reference levels for each ADC section. The single SA-ADC section consists of an auto-zero comparator, DAC, SAR and a calibration module.

3 Simulation and Experimental Results

To simulate the function of this calibration module, we assume that the capacitor C_1 of each SA-ADC cell has a normal distribution with a standard deviation of 5%. The static simulation is shown in Fig. 4 with the

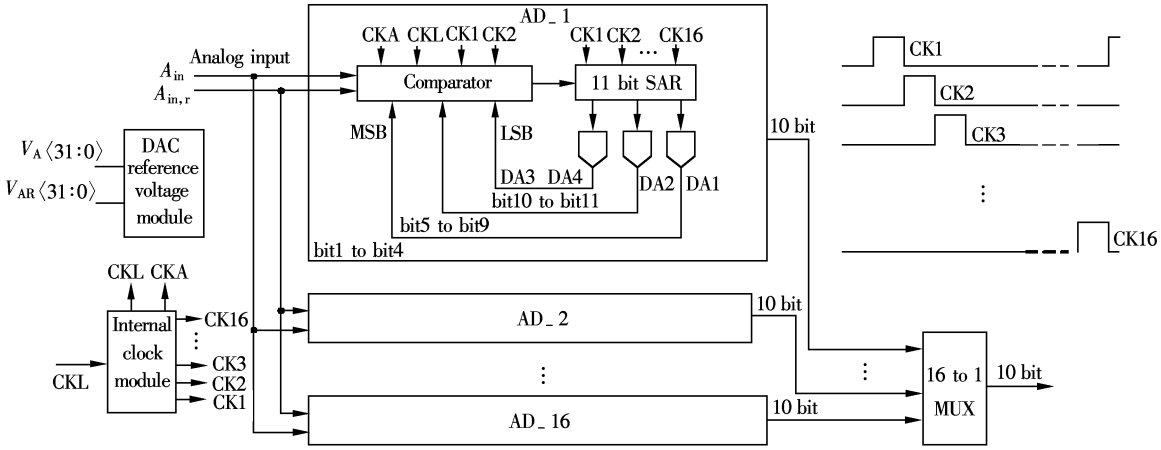

Fig. 3 Structure of 16 time-interleaved ADCs

calibration clock. We can see from the diagram that the calibration potential of TA1 and TA2 press in the grid alternately high and low, to adjust the resistance ratio among R_{MN1} to R_{MN4}. After a period of time, the potential stays relatively stable and the calibration goes into a balance.

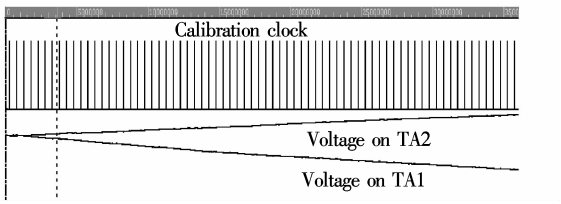

Fig. 4 Waveform of capacitor calibration

NanoSim-VCS co-simulation is adopted to simulate the dynamic parameters of the ADC. A coherent sampling is performed with a 1 MHz input signal and a 32 MHz sampling clock. 2 048 points are taken and Matlab is used to compute the SNR, SINAD and SFDR. The output spectrum without calibration is shown in Fig. 5. It is clear that the capacitor mismatches result in harmonic distortion of the time-interleaved ADCs[2-3]. Fig. 6 shows the calibrated output spectrum after the calibration module is adjusted for a period of time. The harmonic is removed. The simulated SINAD is 58. 787 8 dB, SNR is 59. 586 1 dB, SFDR is 70. 246 dB. The average power consumption is about 32. 78 mW (without PAD), the highest is 157. 12 mW, with a 2. 5 V supply. The third harmonic is the most adverse factor affecting the SFDR, which is mainly caused by pseudo-differential input.

The ADC has been fabricated in a Chart 0. 25 μm double-poly five-metal CMOS process as a front-end of a cable set-top box, which is packaged in plastic quad flat package (PQFP) with 64-lead. The test board is shown in Fig. 7. The input-signal is generated from the function generator Hewlett-Packard HP8648B and the clock-signal is driven by a 32 MHz crystal. The output of the ADC is buffered by SN74ALVCH16244, and

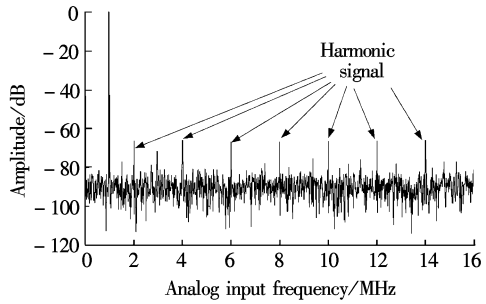

Fig. 5 Output spectrum with capacitor offset

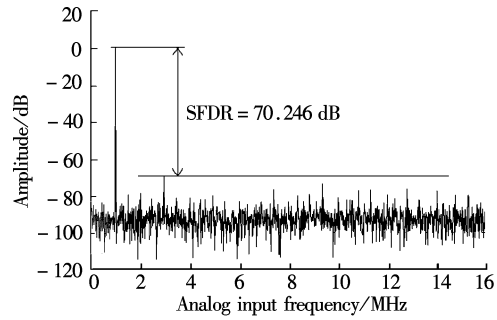

Fig. 6 Output spectrum with capacitor calibrated

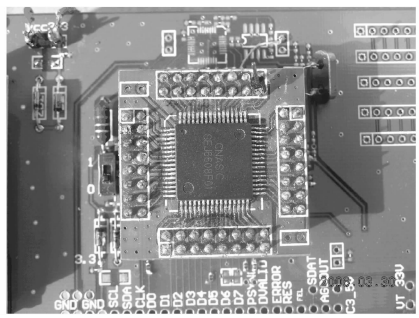

Fig. 7 Test board of the ADC

then goes into Logic Analyzer Agilent 16702B. Fig. 8 shows the fast Fourier transform (FFT) results with a 5. 8 MHz input at −1dBFS and a 32 MHz sampling clock, which achieves 44. 9 dB SNR, 44. 82 dB SINAD, and 63. 76 dB SFDR. All measurements are performed with a 2. 5 V supply at room temperature (25 ℃).

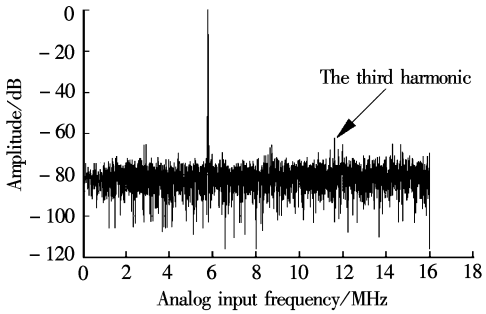

Fig. 8 Spectrum obtained with 5.8 MHz input

Fig. 8 shows that the calibration module effectively restrains the harmonic of the signal, except for the third, effectively. It is almost the same as the simulation results and guarantees the required SFDR of the ADC. The measured SNR differs from the theoretical 10 bit 60 dB. As is known to all, the FFT noise floor is $10\lg(N/2)$ dB below the actual noise floor. Compared with Fig. 6 and Fig. 8, deduct the 6 dB noise floor differences due to the 2048 FFT and 8192 FFT. Then we can see that the noise floor is lifted in the test. This is mainly because of the random jitter of clock signals[8].

4 Conclusion

A linear analog calibration technique to reduce the capacitor mismatches in a time-interleaved SA-ADC is proposed in this paper. The calibration module can work parallel with the ADC conversion and calibrate the capacitor mismatches effectively. It avoids the requirements of precision matching and trimming of components as normally expected with the ADC signal conversion. The ADC is implemented in a double-poly five-metal CMOS process. It is demonstrated that the calibration module can reduce the harmonic distortion effectively.

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时间交叉存取逐次逼近型 ADC 中的电容自校准技术

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摘要:设计了一种用于逐次逼近型 ADC 中的电容自校准电路. 通过增加一个校准周期,该电容自校准结构即可与原电路并行工作,并可校准电路工作时产生的误差. 采用该电路设计了一个用于多通道逐次逼近型结构的 10 bit 32 Msample/s 模数转换器单元,该芯片在 Chart 0.25 μm 2.5 V 工艺上实现,总的芯片面积为 1.4 mm × 1.3 mm. 在 32 MHz 工作时,通过校准后的信噪比仿真结果为 59.586 1 dB,无杂散动态范围为 70.246 dB. 芯片实测,输入频率 5.8 MHz 时,信噪失真比为 44.82 dB,无杂散动态范围为 63.760 4 dB.

关键词:电容自校准;模数转换器;逐次逼近;时间交叉存取

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