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Design of 0.18 μm CMOS programmable frequency divider based on standard cells

He Xiaohu Hu Qingsheng

(Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

Abstract: The design of a programmable frequency divider, which is one of the components of the phase-locked loop (PLL) frequency synthesizer for transmitter and receiver in IEEE 802.11a standard, is investigated. The main steps in very large-scale integration (VLSI) design flow such as logic synthesis, floorplan and placement & routing (P & R) are introduced. By back-annotating the back-end information to the front-end design, the custom wire-load model is created and used for optimizing the design flow under deep submicron technology. The programmable frequency divider is implemented based on Artisan TSMC (Taiwan Semicoductor Manufacturing Co. Ltd.) 0.18 μm CMOS (complementary metal-oxide-semiconductor) standard cells and fabricated. The chip area is 1 360.5 μm^2 and can work in the range of 100 to 200 MHz. The measurement results indicate that the design conforms to the frequency division precision.

Key words: programmable frequency divider; frequency synthesizer; standard cells; CMOS

In modern communication systems, the phase-locked loop (PLL) frequency synthesizer is one of the basic components. The operating frequency of the frequency synthesizer is limited by both the frequency divider and the voltage controlled oscillator (VCO)[1-3]. Many researches have focused on the frequency synthesizer with high operating frequency. However, there is an increasing demand for its multi-system application. For example, in the 5 to 6 GHz band, there are HIPERLAN Ⅰ/Ⅱ and IEEE 802.11a standards, they work within a similar band but at different center frequencies and channel spaces[4-5].

In this paper, a new programmable frequency divider for the frequency synthesizer is implemented in TSMC 0.18 μm CMOS technology. The programmable frequency divider is designed based on standard cells and the remaining parts of the frequency synthesizer are designed using the full custom method. Measurement results indicate that our programmable frequency divider works well in the frequency synthesizer. With the programmable frequency divider, the frequency synthesizer can perform multi-modulus division and can be used in multi-standard applications.

1 Frequency Synthesizer Architecture

In the PLL frequency synthesizer, the high-speed digital frequency divider is usually formed by cascading divided-by-2 stages for high operation frequency of the system[6]. However, this method can only obtain the division ratios equal to the n power of 2, where n is the number of divided-by-2 stages. So, an integer-N frequency synthesizer structure is adopted in our design. It is because the integer-N frequency synthesizer is more practical, less costly and has low spurious sideband performance as compared to the fractional N frequency synthesizer[7-8]. In order to obtain various division ratios, the dual modulus prescaler (DMP) and the programmable frequency divider are integrated in our PLL frequency synthesizer. In this way, the dividers can obtain any division ratio under the control logic.

Fig. 1 is the block diagram of the frequency synthesizer, in which the output f_{VCO} of VCO is a 4 GHz oscillating signal, and the input signal f_{ref}, generated by the crystal oscillator, is the reference signal for detecting frequency and phase. In the PLL frequency synthesizer, the whole divider is composed of divider DIV/4, DMP and the programmable frequency divider. The divider divided-by-4 outputs a 1 GHz oscillating signal for the up-converter mixer. The output signal of the divided-by-8/9 DMP is also determined by the output of the DIV/4 module. With the control of CtrlLogic, the input signal of DMP is divided-by-259-266. Finally, the output signal of the programmable frequency divider LowOut is sent to the PFD to detect frequency and

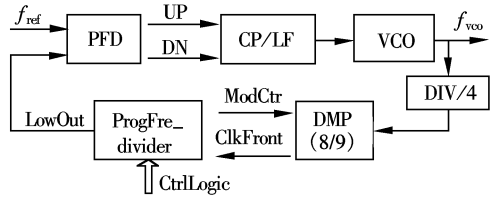

Fig. 1 Block diagram of PLL frequency synthesizer

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Biographies: He Xiaohu (1981—), male, graduate; Hu Qingsheng (corresponding author), female, doctor, professor, qshu@seu.edu.cn.

phase.

2 Design of Programmable Frequency Divider

The programmable frequency divider is shown in Fig. 2. It consists of two counters. One is the program counter, the other is the swallow counter, where the program counter is modulus N_1 while the swallow counter is modulus N_2 ($N_1 > N_2$). The two control parameters N_1 and N_2 can be configured according to the practical applications. Both the counters count up until the values are equal to N_1 and N_2 separately. A period of LowOut is completed when the program counter up-counts to N_1. At the same time, the counters of the programmable frequency divider are cleared when the program counter up-counts to N_1. The most important output of the programmable frequency divider is ModCtr which is used to control the DMP divided-by-8/9. If ModCtr is high, the DMP is divided-by-9; otherwise, it is divided-by-8. In this case, as shown in Fig. 3, the swallow counter keeps the output ModCtr high while its value is less than N_2. Otherwise, ModCtr maintains a low level.

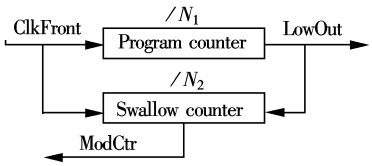

Fig. 2 Block diagram of programmable frequency divider

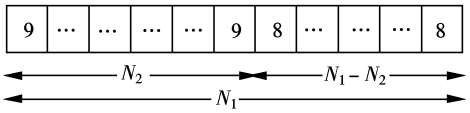

Fig. 3 Principle of frequency division

By using the programmable frequency divider and DMP, divided-by-M can be realized based on the following formula:

$$M = N_2 \times 9 + (N_1 - N_2) \times 8 = N_1 \times 8 + N_2 \quad (1)$$

In our design, $N_1 = 32$. When N_2 varies from 3 to 10, the frequency divider can be divided by 259 to 266 separately. As a result, the VCO can work at eight central frequencies distributing from 4.144 to 4.256 GHz with a 16 MHz interval.

The specific design of the programmable frequency divider is based on the Artisan TSMC 0.18 μm standard cell library. Different from full custom design, standard-cell-based design mainly depends on EDA tools. First, the function is realized in Verilog HDL. Then we use a synthesis tool Design Compiler (DC) to synthesize the design, in which the wire-load model is required for DC to predict the signal delay. It is known that the more precise the wire-load model is, the more perfect the design that can be obtained in submicron technology especially in deep submicron (DSM). In most cases, however, the linear wire-load models are provided by synthesis tools, in which the path delay, wire-load and wire length have linear relationships with the fanout of the circuits[9]. Therefore, it is better to generate a precise wire-load model to improve the synthesis results for a specific design[10]. Fig. 4 is the DSM design flow. In order to create the custom wire-load model before detail synthesis, initial synthesis and initial place and routing (P & R) are required. In these two steps, the "initial" means not much attention is paid to the timing since they are just for creating a practical wire-load model.

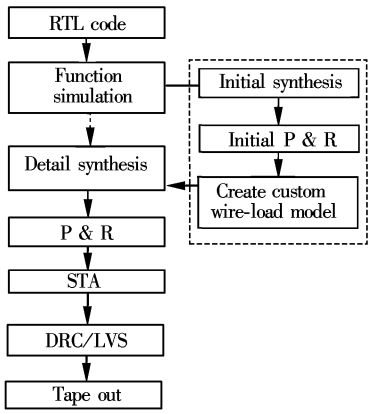

Fig. 4 DSM design flow

After obtaining RC parameters, wire-load delay and the results of initial P & R, we back-annotate them to DC. Then we use the command create_wire_load in DC to create the custom wire-load model. Fig. 5 shows the generated custom wire-load model. From the figure, we know that the wire-length, resistance, capacitance and area do not have the linear relationships with the fanout.

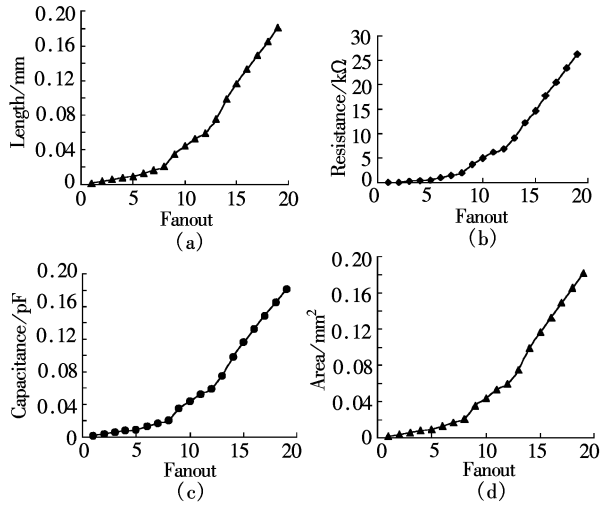

Fig. 5 Generated custom wire-load model. (a) Wire-length vs. fanout; (b) Resistance vs. fanout; (c) Capacitance vs. fanout; (d) Area vs. fanout

After obtaining the custom wire-load model, the design can go to the detail synthesis. Tab. 1 shows the main synthesis constraints set in DC. In this design, the clock period should not be more than 8 ns. Considering the margin for the back-end design flow, the clock period is constrained to 4 ns practically. As for the clock network, the clock latency and uncertainty are both set as 1 ns. The clock signal ClkFront and the clear signal Clr are set as "do not touch network". Of course, the maximum area is constrained to zero to minimize the chip area. With these constraints and the custom wire-load model, better results can be achieved after detail synthesis compared to the default wire-load model.

Tab. 1 Synthesis constraints

Properties in DC	Value
Clock period/ns	4
Clock latency/ns	1
Clock uncertainty/ns	1
Do not touch network	ClkFront, Clr
Net drive	ClkFront, Clr
Maximum area	0

The next steps are P & R, which are back-end design and can be completed in Apollo Ⅱ[11]. Normally, many steps are required to complete P & R. The chip area, power and ground (P/G) pad numbers, and core aspect ratios are considered according to the synthesis results and the I/O numbers of the design. The chip area should include the core area and P/G network area. Typically, the core aspect ratio is set as 1∶1. Experimentally, 6 to 8 I/O pads need a pair of P/G pads. The P/G pad numbers can also be figured out based on the electro-migration and IR drop as follows. From the power consumption report of DC, we know that the core power consumption P_{core} is 12.25 mW. Thus the core power consumption will be up to 20 mW if a 50% margin is set. In TSMC 0.18 μm CMOS technology, the core voltage V_{core} = 1.8 V and the maximum current that an I/O pad can afford is 26 mA, so the core current is P_{core}/V_{core} = 11.1 mA and a pair of P/G pins are enough for the design.

To determine the width of the power strap, the electro-migration and IR drop should be considered. From the technology document we know that the square resistance of metal 1 is 0.101 Ω/sq and its current density is 1 mA/μm. Based on the electro-migration, the minimal width of the power strap should be 11.1 μm. Then we check the power strap width to see if the IR drop is less then 5% of VDD_{core}. Since the IR drop equals 5 mV (< 5% of VDD_{core}), the floor plan of the design meets the requirements of both the electro-migration and the IR drop. Otherwise, if the IR drop is larger than 5% of VDD_{core}, the minimal width of power strap should be recalculated according to the IR drop.

The static timing analysis (STA) can be performed after P & R. Some back-end design results, such as set_load, standard delay format (SDF) and detailed standard parasitic format (DSPF) files, can be back-annotated to the timing analyzer Prime Time (PT) to analyze the static timing. The analysis results show that both hold time and setup time satisfy the design requirements.

The last step of the design flow is the verification. By importing the layout information from Apollo into Cadence Virtuoso, we use Mentor Calibre to perform design rule check (DRC) and layout-vs-schematic (LVS) and to verify the correction of the design. Additionally, we use extracted RC parameters to do the transient analysis in HSPICE. The transient analysis results are shown in Fig. 6. Here, $N_2 = 6$, in order to obtain a complete period waveform, the period of both Clr and ClkFront are configured as 320 ns and 8 ns, respectively. The waveform shows that the division precision is identical to its functional simulation result when $N_2 = 6$. And when N_2 equals other values varying from 3 to 10, the division precision also conforms to our design requirements.

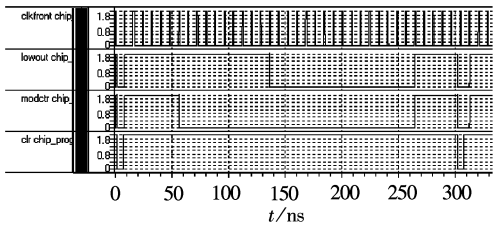

Fig. 6 Transient simulation result ($N_2 = 6$)

3 Measurement Results

The programmable frequency divider has been implemented in TSMC 0.18 μm CMOS technology and taped out. Fig. 7 shows the die photo of the programmable frequency divider, where the core area is 1 360.5 μm^2 and the total area is 0.66 mm^2.

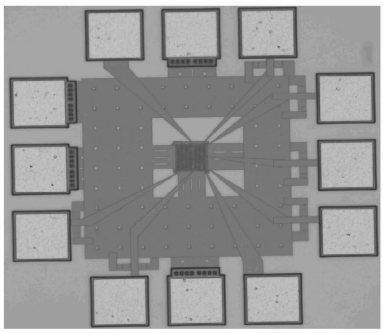

Fig. 7 The die photo of the chip

Measurements are carried out on-wafer with an RF probe station. The outputs of the chip are connected to the 50 Ω ports of a high impedance oscilloscope. The measurement results of power consumption indicate that the current is about 7.5 mA which is very close to the post simulation result, as shown in Tab. 2. The voltage is supplied with 1.8 V. Fig. 8 shows the measurement results of the chip. From Fig. 8 we can see that the duty circle of ModCtr is 25.13%, and LowOut is 50.96% when $N_2 = 8$. Consequently, the function of frequency division is realized precisely.

Tab. 2 Test result of power consumption

Item	Current/mA	Power consumption/mW
Simulation	6.8	12.25
Test	7.5	13.4

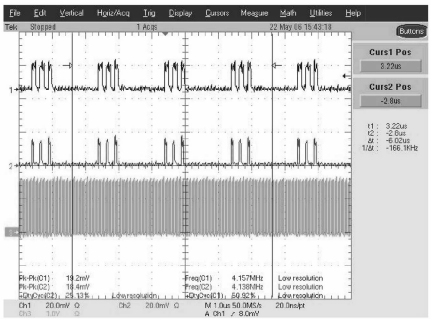

Fig. 8 Measurement results of the chip ($N_2 = 8$)

4 Conclusion

A programmable frequency divider is implemented using TSMC 0.18 μm CMOS technology based on Artisan standard cells. By back-annotating the useful messages of back-end design to synthesis tools and creating the custom wire-load model, we obtain a more precise process for DSM technology. Measurement results indicate that the frequency divider achieves the expected precision.

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基于 0.18 μm CMOS 标准单元的可编程分频器设计

何小虎　　胡庆生

(东南大学射频与光电集成电路研究所,南京 210096)

摘要:设计实现了一种应用于 IEEE 802.11a 收发信机的 PLL 频率综合器中的可编程分频器. 介绍了逻辑综合、版图规划、布局布线等 VLSI 设计流程的关键步骤,通过将后端信息返标到前端设计工具,生成自定义线负载模型,优化了深亚微米工艺下的设计流程. 可编程分频器采用 Artisan TSMC 0.18 μm CMOS 标准单元库设计并流片. 芯片内核面积为 1 360.5 μm^2,可工作在 100 ~ 200 MHz 的频率范围. 测试结果表明芯片能够完成精确的分频比.

关键词:可编程分频器;频率综合器;标准单元;CMOS

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