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11.6-GHz 0.18-μm monolithic CMOS phase-locked loop

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Abstract: A design of a 11.6-GHz phase-locked loop (PLL) fabricated in 49-GHz 0.18-μm CMOS (complementary metal-oxide-semiconductor transistor) technology is described. An analog multiplier phase detector (PD), a one-pole passive low pass filter and a three-stage ring oscillator with variable negative-resistance loads build up the monolithic phase-locked loop. The measured rms jitter of output signal via on-wafer testing is 2.2 ps under the stimulation of $2^{31}-1$ bit-long pseudo random bit sequence (PRBS) at the bit rate of 11.6 GHz. And the tracking range is 250 MHz. The phase noise in the locked condition is measured to be −107 dBc/Hz at 10 MHz offset, and that of the ring VCO at the central frequency is −99 dBc/Hz at 10 MHz offset. The circuit area of the proposed PLL is only 0.47 mm × 0.72 mm and the direct current (DC) power dissipation is 164 mW under a 1.8-V supply.

Key words: phase-locked loop; CMOS technology; high speed

High-speed low-power phase-locked loops (PLLs) are an indispensable part of clock recovery circuits and frequency synthesizers, and have wide application in optical data links, synchronous digital hierarchy (SDH) systems and wireless communication. In the multigigahertz range, most of the analog circuits have been implemented in BiCMOS or GaAs in the past. From the view of system integration, it is desirable to design these kinds of circuits in CMOS technologies for the realization of system on chip (SOC)[1].

This paper describes the design of an 11.6-GHz PLL with a tracking range from 11.39 to 11.64 GHz.

1 PLL Architecture

Fig. 1 shows the block diagram of our PLL, a fairly standard topology consisting of six parts, an input buffer, a phase detector (PD), a low-pass filter(LPF), a voltage-controlled oscillator (VCO), a shifter and an output buffer[1].

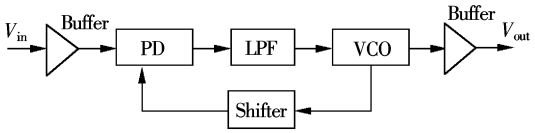

Fig. 1 Phase-locked loop architecture

The PLL incorporates fully differential circuits in both the high-frequency signal path and the frequency control path to improve the common-mode rejection.

2 Building Blocks

2.1 VCO

The design of the VCO directly affects several critical parameters of the PLL, such as speed, timing jitter, spectral purity, and power dissipation. Although LC topologies can achieve a lower phase noise, their limited tuning range may lead to narrow tracking range of the PLL. So we chose a wide range ring oscillator in our first design in 0.18-μm technology.

There are three stages in this ring oscillator[2]. As shown in Fig. 2, each stage is a differential amplifier with variable negative-resistance load[3-4]. The load of the differential pair consists of two resistors R_1 and R_2 ($R_1 = R_2 = R_p$) and the cross-coupled pair M3-M4. As the current of M3 and M4 increases, the small-signal resistance $-1/g_{m_{3,4}}$ becomes less negative, and the equivalent resistance $R_p//(-1/g_{m_{3,4}})$ increases, which

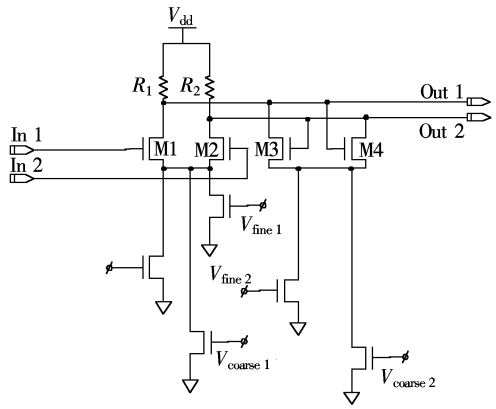

Fig. 2 Implementation of each stage

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may lower the operating frequency of the oscillator[5].

2.2 Phase detector

The phase detector realizes the conversion from phase to voltage. Although there are many design techniques of CMOS PDs, a simple Gilbert cell which behaves as an analog multiplier is employed[6]. The advantage of the analog multiplier PD is its high operation speed as compared with other implementations such as XOR PD, DFF PFD, bang-bang PD etc[7]. As shown in Fig. 3, it compares the phase of input and output of the oscillator after shifting, then converts the phase error to the voltage.

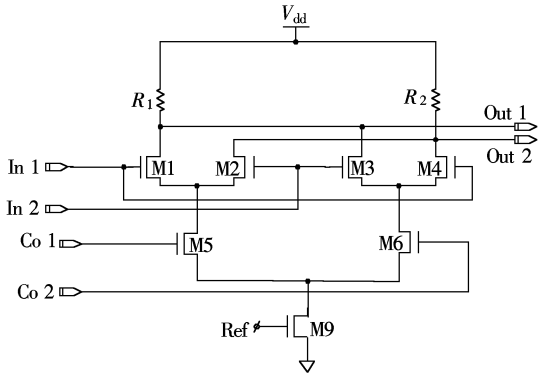


Fig. 3 Phase detector

2.3 Low-pass filter

The general phase-locked loop is considered as the second order. In principle, the low-pass filter can include more poles to achieve sharper cut-off characteristics, a desirable property in many applications. However, it is difficult to make such systems stable, especially when process and temperature variations are taken into account. Therefore, in this design we employ a one-pole passive low-pass filter, which just consists of a capacitor and a resistor[8].

3 Experimental Result

Our PLL has been fabricated in a 49-GHz 0.18-μm CMOS technology. Fig. 4 is a photograph of the die, in which active area is about 470 μm × 720 μm.

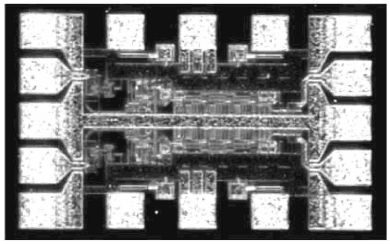
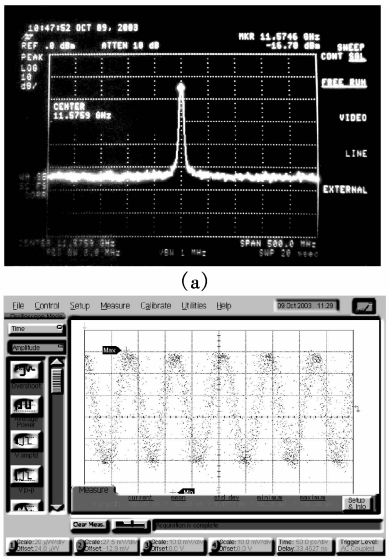


Fig. 4 PLL die photograph

Via on-wafer testing, the total supply current is 91 mA under a 1.8-V supply. Of this value, approximate 42 mA is drawn by the VCO, 16 mA by the output buffer, and 33 mA by the phase detector and shifter.

The measured output of the oscillator in the frequency domain is depicted in Fig. 5(a). The operating frequency is 11.57 GHz, and the phase noise is −99 dBc/Hz at 10 MHz offset. Fig. 5(b) is the corresponding output in time domain.

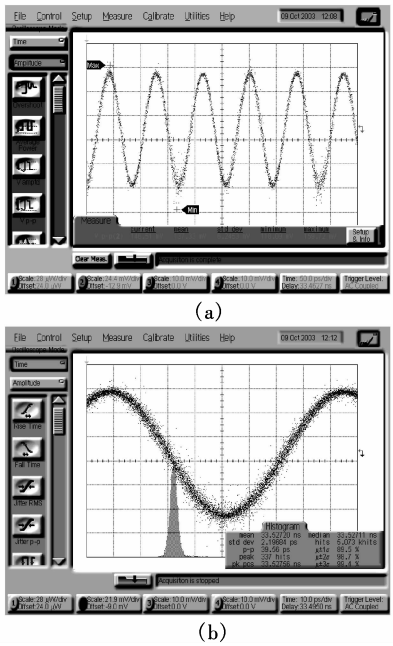


(a)

(b)

Fig. 5 Measured VCO output. (a) Spectrum of the VCO; (b) Output of the VCO in time domain

Fig. 6 shows the measured output in the time domain when the circuit is locked to a 11.57 GHz input whose amplitude is 100 mV. The bottom window dis-



(a)

(b)

Fig. 6 Measured PLL output in time domain. (a) Waveforms of PLL output; (b) Jitter histogram of PLL output

plays one of the edges on a horizontal scale of 50 ps/div, revealing an rms jitter of 2.2 ps and a peak-to-peak jitter of 39 ps. The PLL achieves a tracking range of 250 MHz.

The performance of PLL has also been examined in the frequency domain. As shown in Fig. 7, when the loop is locked, the phase noise is −107 dBc/Hz at 10 MHz offset.

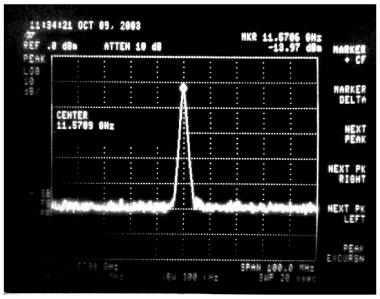


Fig. 7 PLL output spectrum

All the performance of our PLL is summarized in Tab. 1.

Tab. 1 The performance of our PLL

Parameters	Value
Center frequency/GHz	11.57
Amplitude of V_{in}/mV	100
Power dissipation/mW	163.8
Tracking range/GHz	11.39 to 11.64
Rms jitter/ps	2.2
Amplitude of V_{out}/mV	73
Phase noise/dBc@10 MHz	−106.6
Chip size/mm^2	0.47×0.72

The pretty good results are attributed to the following considerations.

First of all, the post-simulation is especially necessary in the design of high-speed circuits. In high-speed circuits, large differences can be found between the experimental results and the results of pre-simulation, but the results of post-simulation are close to the experimental results, as shown in Tab. 2.

Tab. 2 Comparison between simulations and result

Process	Center frequency/GHz	Amplitude/mV
Pre-simulation	13.67	160
Post-simulation	11.36	180
Experimental result	11.57	186

Secondly, the proper model should be chosen. There are two models in TSMC 0.18-μm CMOS technology. One is the mixed signal model, and the other is the radio frequency (RF) signal model. They are designed for different situations. The mixed signal model is suitable for the design of high-speed, large-scale and high-power circuits. While, the RF signal model is suitable for the design of small-scale, low-power and low-noise circuits[9]. Therefore, we should choose the mixed signal model. In addition, it can be proved that the mixed signal model is not bad in noise.

In addition, it is also very important to optimize the layout in the design of high-speed circuits. Especially, to optimize the key transistors, we employ folded structure in differential transistors of VCO, and from the result of the post-simulation, the center frequency of VCO increases beyond 1 GHz[2].

Also, the antenna effect, latch-up, reference distribution, resistors and capacitors of metal layers are taken into account[10].

Finally, simple structure should be employed in the design of high-speed circuits. Fewer devices can reduce parasitical effects in the layout for achieving high speed.

4 Conclusion

The high-speed circuit techniques mentioned above make it possible to design high-performance phase-locked loops and clock recovery circuits in very large scale integrated circuit technologies. Based on these techniques we designed a monolithic CMOS PLL with the center frequency of 11.6 GHz. The oscillator jitter in the locked condition is reduced to an rms value of 2.2 ps.

The circuit can not only be used for demodulation and frequency synthesis applications, but also be used in clock recovery with the addition of a preprocessor.

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11.6-GHz 0.18-μm CMOS 锁相环电路

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摘要：利用截止频率为 49 GHz 的 0.18-μm CMOS 工艺，设计实现了 11.6-GHz 锁相环电路. 该电路由模拟乘法鉴相器、单极点低通滤波器及采用可变负电阻负载的三级环形振荡器构成. 在片晶圆测试表明，该芯片在输入速率为 11.6 GHz、长度为 $2^{31}-1$ 伪随机序列的情况下，恢复时钟的均方根抖动为 2.2 ps. 锁相环的跟踪范围为 250 MHz. 环形振荡器在偏离中心频率为 10 MHz 处的单边带相位噪声为 –107 dBc/Hz. 在锁定条件下，锁相环在偏离中心频率为 10 MHz 处的单边带相位噪声为 –99dBc/Hz. 芯片面积为 0.47 mm × 0.72 mm，在 1.8-V 电源供电下，功耗为 164 mW.

关键词：锁相环；CMOS 技术；高速

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