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20 Gbit/s 1∶2 demultiplexer of low-power using 0.18 μm CMOS

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Abstract: A 1∶2 demultiplexer (DEMUX) that is fabricated using 0.18 μm CMOS (complementary metal-oxide-semiconductor transistor) technology is presented. The DEMUX consists of a master-slave-slave, master-slave D flip-flops and output buffers. The D flip-flop employs a dynamic-loading structure and common-gate topology with single clock phase for the bias transistors. The dynamic-loading structure can make the circuit work faster because it decreases the charge/discharge time of the output node, and it consumes lower power because its working current is in a switch mode. In addition, the positive feedback loop, which is made up of a cross-coupled transistor pair in the latch, speeds up the circuit. Measurement results at 20 Gbit/s $2^{23}-1$ pseudo random bit sequence (PRBS) via on-wafer testing show that the 1∶2 DEMUX can operate well. The power dissipation is 108 mW with the area of 475 μm × 578 μm.

Key words: demultiplexer; dynamic-loading; low power; high speed

Due to the demand for the realization of an optical communication growth, larger transmission capacity is required. The demultiplexer (DEMUX) is one of the key circuits used in constructing communication systems and plays an important role in converting a high-speed data stream into several low-speed parallel data ones. DEMUXs operating at speeds higher than 10 Gbit/s have been realized with GaAs HBTs, SiGe bipolar transistors, and BiCMOS[1-3]. The power consumption of these ICs, however, is relatively large. CMOS technology has the advantages of low power and low cost. So it is gradually used in the high speed IC designs with its steady improvement. Although the f_T of the 0.18 μm CMOS is 49 GHz, there have been few papers on 20 Gbit/s class DEMUX circuits using 0.18 μm CMOS technology. This paper illustrates the detailed realization of a 20 Gbit/s 1∶2 low-power DEMUX with TSMC 0.18 μm CMOS technology, in which a latch structure with single clock phase and dynamic-loading[4] are adopted. Compared with the traditional SCFL[5] (source coupled FET logic) structure, its speed is faster and the power consumption is lower.

1 Structure of DEMUX

Fig. 1 shows the block diagram of the 1∶2 DEMUX. It consists of a DEMUX core and two 10 Gbit/s output buffers. In this architecture, the input signal, which consists of a high-speed 20 Gbit/s data D and a 10 GHz clock, goes through the DEMUX, and in the output we get two 10 Gbit/s data q_1, q_2. Then q_1, q_2 are amplified by two outbuffers separately. The DEMUX core consists of a master-slave-slave (MSS) and master-slave (MS) D flip-flops as shown in Fig. 2. It captures the lead bit on the positive-edge of the clock and the following bit on the negative-edge. Therefore, the clock frequency is half of the input data rate, which degrades the design difficulty.

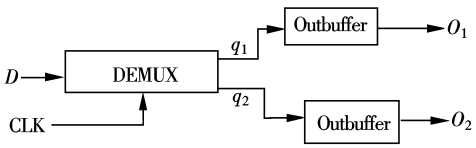

Fig. 1 Block diagram of 1∶2 DEMUX

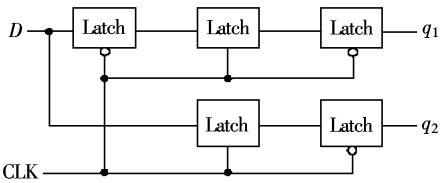

Fig. 2 Block diagram of the DEMUX

Both the MSS and MS D flip-flops are composed of latches, so the circuit topology of the latch is very important to the whole circuit. It affects not only the circuit speed but also the power dissipation.

2 Latch Design Analysis

Both SCFL and dynamic-loading structures can be used to implement latch design. Analysis for them is presented in the following.

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2.1 SCFL

SCFL structure is shown in Fig. 3. The latch structure consists of a pair of loads (R_1-R_2), a sampling pair (MN_1-MN_2), a latching pair (MN_3-MN_4) and two nMOS switches (MN_5-MN_6), which are controlled to turn on or off by CLK and CLK_n signals. When CLK = H, MN_5 is on while MN_6 is off and MN_1-MN_2 is used to sense the input in the sampling mode. When CLK = L, MN_6 is on while MN_5 is off and the cross-coupled pair MN_3-MN_4 is configured as a positive feedback to latch the output in the latching mode.

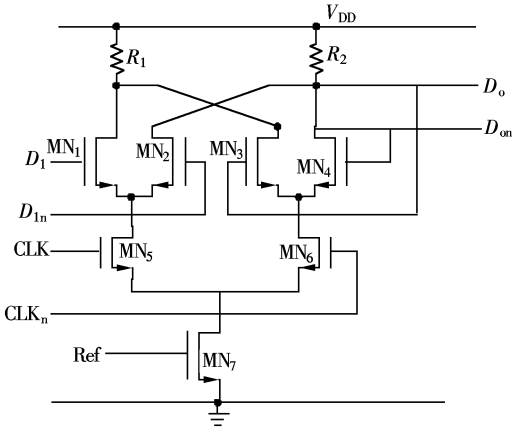


Fig. 3 Schematic of SCFL structure

The difficulty of the latch design is to choose the loads. We know that the charge/discharge time of the output node is in proportion to the total capacitor C and resistor R of the output.

On the one hand, it needs a small R to reduce the time, which makes for high speed; on the other hand, it needs a large R to attain a big output voltage swing V_{om}. As $V_{om} = RI$, the larger the R is, the smaller the circuit current is assuming the same $V_{om.}$ So a large R also leads to a low power consumption. But SCFL structure cannot meet the requirement due to its constant load.

2.2 Dynamic-loading

Fig. 4 shows the schematic of a dynamic-loading latch. It consists of a pair of pMOS(MP_1-MP_2), a sampling pair(MN_1-MN_2), a latching pair(MN_3-MN_4) and a clock switch (MN_5). The structure of SCFL and dynamic-loading correspond, so their functions are the same. The places where the second structure differs from the first are MP_1-MP_2, which is used as dynamic load, and MN_5, which is controlled by one single clock signal.

The resistance of MP_1-MP_2 is varied dynamically by clock signals. When CLK = L, the pMOS transistors work in the linear region and the turn-on resistances are very small, so a small RC time constant is

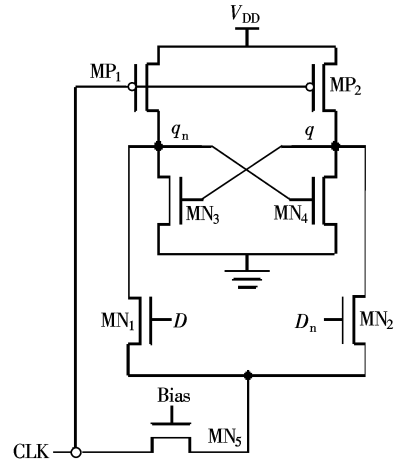


Fig. 4 Schematic of dynamic-loading structure

achieved, which accelerates the sampling speed. Such a small RC time enables the nMOS MN_1-MN_2 pair to sense the input data and charge up the output node at a maximum speed. When CLK = H, the pMOS transistors are turned off, which leads to a large RC time constant. The nMOS pair MN_3-MN_4 hold the output state. In this mode, the current of the latch approximates zero. As a result, the power consumption is greatly reduced compared to that of the SCFL, in which the working current is always being.

Unlike the SCFL design shown in Fig. 3 where MN_5-MN_6 is controlled by two complementary clock signals, NM_5 in Fig. 4 only requires one single clock signal. In order to operate at high speed, a common-gate configuration is used for the clock transistor (MN_5) rather than the common-source configuration. By using the common-gate configuration, the dc biasing of the input clocks can be optimized simultaneously for both the pMOS loadings and the nMOS.

The analysis of SCFL and dynamic-loading structure indicates that the maximum operation frequency of the former cannot be reached as fast as the latter due to its constant load. Besides, dynamic-loading structure consumes nearly half of the power of the SCFL, since its working current is provided in a switch mode. That is why the dynamic-loading is adopted in this DEMUX design.

3 Measurement Results

A micrograph of the DEMUX chip is shown in Fig. 5 and its area is 475 μm × 578 μm. The measurement of the chip was performed on-wafer using high-speed microwave probes of Cascade Microtech Inc. The supply voltage was 1.8 V. The input clock was 10 GHz, and the input pattern was a 20 Gbit/s $2^{23} - 1$ pseudo random bit sequence (PRBS). The output eye

diagrams are presented in Fig. 6.

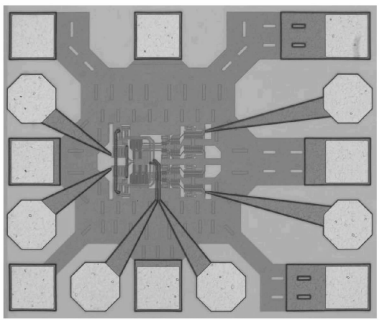
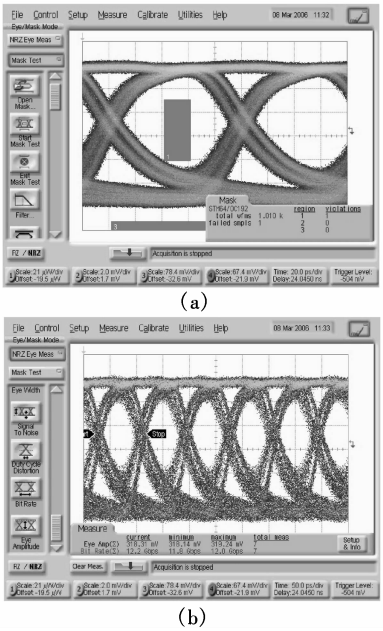


Fig. 5 Chip micrograph of the EDMUX



(a)

(b)

Fig. 6 Output eye diagrams. (a) 20 Gbit/s input; (b) 24 Gbit/s input

Fig. 7 shows the measured input and output waveforms of the 1∶2 DEMUX when the input pattern is 0000 1111 1111 0000 1111 0000 0011 1111. The total power dissipation is 108 mW. The measured eye opening performed well with more than 300 mV on the external 50 Ω load. During the measurement, the function of the 1∶2 DEMUX was verified. It can work well under the input data of 20 Gbit/s and even work at up to 24 Gbit/s.

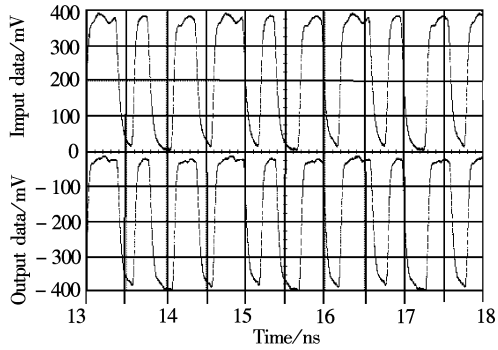


Fig. 7 Measured waveforms of the DEMUX

Tab. 1 shows measured performance of the proposed DEMUX together with that of reported DEMUX designs. The ratio of the speed (v) of DEMUX to f_T in the table is used to weigh the difficulty of the design, and our work is the most difficult among these, which proves that the dynamic-loading structure is relatively superior to others in increasing operating speed. Furthermore, the power consumption of this chip is only 15% of Ref. [6] with the same 20 Gbit/s data rate.

Tab. 1 Comparison of published DEMUX with the proposed DEMUX

	Feature size	f_T/GHz	Speed v/(Gbit·s^{-1})	v/f_T	Structure	Power/mW
Ref. [5]	0.18 μm CMOS	49	10	0.20	SCFL	240(1∶4)
Ref. [6]	0.2 μm PHEMT	60 to 63	20	0.32 to 0.33	SCFL	720
Ref. [7]	0.13 μm InP HEMT	220	50	0.23	SCFL	490(1∶4)
This paper	0.18 μm CMOS	49	20	0.41	Dynamic-loading	108

4 Conclusion

A 20 Gbit/s 1∶2 demultiplexer has been designed and fabricated in TSMC 0.18 μm CMOS technology. A latch structure of dynamic-loading with a common-gate topology and a single clock phase is used to increase its speed and decrease its power dissipation. Under the 1.8 V supply, this DEMUX can work at 20 Gbit/s and the whole power is 108 mW. These results prove that this design is a viable solution to realize DEMUX at ultra high speed with low power by using a deep submicron CMOS process.

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20 Gbit/s 低功耗 0.18 μm CMOS 1∶2 分接器

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摘要：采用 TSMC 0.18 μm CMOS 工艺实现了一个 20 Gbit/s 1∶2 分接器，分接器由主-从-从、主-从 D 触发器和数据输出缓冲组成. D 触发器单元采用动态负载结构，其偏置晶体管采用单时钟输入的共栅结构. 动态负载结构的触发器工作速度更快因为它减小了输出点的冲放电时间，而且由于工作时电流处于开关模式，其功耗更低. 另外，触发器中采用交叉耦合的正反馈三极管对，加快了整个电路的速度. 通过在片晶圆测试，该芯片在输入 20 Gbit/s、长度为 $2^{23}-1$ 的伪随机码时工作良好. 功耗仅为 108 mW，芯片面积为 475 μm × 578 μm.

关键词：分接器；动态负载；低功耗；高速度

中图分类号：TN722