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Performance analysis of a novel chip tracking loop used for regenerative pseudo-noise ranging clock recovery

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Abstract: To improve the performance of composite pseudo-noise (PN) code clock recovery in a regenerative PN ranging system at a low symbol signal-to-noise ratio (SNR), a novel chip tracking loop (CTL) used for regenerative PN ranging clock recovery is adopted. The CTL is a modified data transition tracking loop (DTTL). The difference between them is that the Q channel output of the CTL is directly multiplied by a clock component, while that of the DTTL is multiplied by the I channel transition detector output. Under the condition of a quasi-squareware PN ranging code, the tracking (mean square timing jitter) performance of the CTL is analyzed. The tracking performances of the CTL and the DTTL are compared over a wide range of symbol SNRs. The result shows that the CTL and the DTTL have the same performance at a large symbol SNR, while at a low symbol SNR, the former offers a noticeable enhancement.

Key words: clock recovery; tracking loops; pseudo-noise codes ranging; data transition tracking loop; chip tracking loop

A ranging system determines the distance to an object by measuring the delay of a signal between transmission and reception. Fundamentally, there are several types of ranging signals such as tones[1], sequential[2–4] codes and PN codes[5–8]. With the progress of digital design techniques and the improvement of the very large scale integration (VLSI) technologies, PN codes and regenerative ranging have become important techniques of spacecraft ranging systems. The principle of PN and regenerative ranging is described in Refs. [5 – 6]. Until recently, the turnaround PN code ranging has been implemented by the Euro Space Agency (ESA)[9–11]. While the PN code regenerative ranging is under development both by the National Aeronautics and Space Administration (NASA) and the ESA[12–15]. Compared to the turnaround PN codes ranging, the PN regenerative ranging can effectively increase the ranging signal power, which is useful for ranging precision promotion and can be applied in the low signal-to-noise ratio (SNR) environment to improve SNR.

In a PN regenerative ranging system, a high performance clock synchronizer is needed, which is used for accurate PN code detection to reduce the following correlation time and to obtain small timing jitter in order to improve the ranging accuracy. This paper presents a novel chip tracking loop (CTL) used for quasi-squarewave PN ranging code clock recovery. The CTL is a modified data transition tracking loop (DTTL)[16–19], which has been used over the past few decades as a common clock synchronizer in digital systems to track non-return-to-zero (NRZ) received data with additive white Gaussian noise (AWGN). In particular, this paper analyzes the CTL and the DTTL tracking performances under the condition of a quasi-square-wave PN ranging code. As will be shown herein, the mean-square timing jitter of the CTL is always better than that of the DTTL, especially at a low symbol SNR.

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1 CTL vs. DTTL Structure

The JPL1999 PN code[5–6] is used in most modern transponders, which is a composite code and built from six component codes. The length of each component code is 2, 7, 11, 15, 19 and 23, respectively. The component sequences are as follows:

C_1: +1, −1

C_2: +1, +1, +1, −1, −1, +1, −1

C_3: +1, +1, +1, −1, −1, −1, +1, −1, +1, +1, −1

C_4: +1, +1, +1, +1, −1, −1, −1, +1, −1, −1, +1, +1, −1, +1, −1

C_5: +1, +1, +1, +1, −1, +1, −1, +1, −1, −1, −1, −1, +1, +1, −1, +1, +1, −1, −1

C_6: +1, +1, +1, +1, +1, −1, +1, −1, +1, +1, −1, −1, +1, +1, −1, −1, +1, −1, +1, −1, −1, −1, −1

The first component C_1 is identified as a clock component. The ranging sequence is built by logic "and" operations from components C_2 to C_6 and "or" operations with the clock component C_1 (assuming that − 1 maps to logic "0" and + 1 maps to logic

"1"), shown as follows:

$$\text{seq}(i) = C_1(i) \cup (C_2(i) \cap C_3(i) \cap C_4(i) \cap C_5(i) \cap C_6(i)) \quad (1)$$

The resulting sequence length is the product of the six sequence lengths, i. e. 1 009 470 chips. It is easy to show the distribution of " +1" and " −1":

$$\sum_{i \text{ is even}} \text{seq}(i) = 504\,735, \quad \sum_{i \text{ is odd}} \text{seq}(i) = -458\,655 \quad (2)$$

Since half of the sequence length is 504 735, this means that, for i even, the sequence is always +1, and, for i odd, there are 481 695" −1" and 23 040" +1". It is impossible to have the continual −1 sequence and this feature will be utilized in the CTL. The sequence resembles an alternating +1/−1 sequence, also called as quasi-squarewave.

For the above composite PN code sequence in ranging, the DTTL is usually adopted as the clock synchronizer[16–19] (see Fig. 1). The NRZ baseband input signal is first passed through two parallel channels: the in-phase channel (the upper part) monitors the polarity of the actual transitions, and the quadrature channel (the lower part) measures the timing error. Specifically, the in-phase channel accumulates over a symbol followed by a hard decision on the signal polarity. By subtracting two successive decisions, a transition detector is used to determine whether a no transition (0), a +1 to −1 transition, or a −1 to +1 transition has occurred. The quadrature channel, on the other hand, accumulates over the estimated symbol transition and, after an appropriate delay, is multiplied by the in-phase channel output I_k. The multiplication results in an error signal e_k, which is proportional to the estimation of the phase (or timing) error. Subsequently, e_k is filtered and the resulting output is used to control the timing logic.

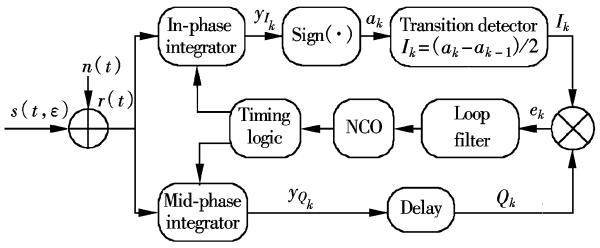

Fig. 1 Data transition tracking loop structure

The CTL differs from the DTTL in the way that the Q channel output of the CTL is directly multiplied by +1/−1, while that of the DTTL is multiplied by the I channel transition detector output. The functional block diagram of the CTL is illustrated in Fig. 2. A mid-phase integration of one chip duration is multiplied by the interlacing of −1 and +1. If the period of a chip is T and the phase error is accumulated by L times, the loop update rate is LT. For multiple +1 chip sequences, the phase error pair of negative-going transition (potential) and positive-going transition (potential) results in a complete cancellation within one accumulation. The in-phase integrator is controlled by the CTL timing logic and delivers data out to the following correlation process.

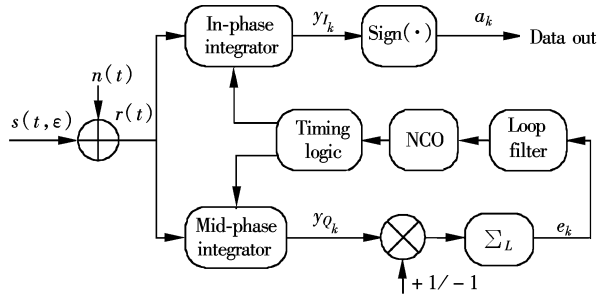

Fig. 2 Chip tracking loop structure

2 Tracking Performance Analysis of CTL and DTTL

Under the condition of a quasi-squarewave PN code with an NRZ signaling format, the received data waveform is given by

$$r(t) = s(t, \varepsilon) + n(t) \quad (3)$$

and

$$s(t, \varepsilon) = A \sum_{n=-\infty}^{\infty} a_n p(t - nT - \varepsilon) \quad (4)$$

where A is the amplitude of the signal; T is the period of the chip; $n(t)$ is AWGN with one-side power spectral density N_0 (W/Hz); ε is the random epoch to be estimated, which is assumed to be uniformly distributed in the interval $-T/2 \leqslant \varepsilon \leqslant T/2$; $p(t)$ is a unit amplitude rectangular pulse of T duration; and a_n represents the k-th symbol polarity, taking on values +1 and −1. Let the timing error λ be defined as

$$\lambda = \frac{\varepsilon - \hat{\varepsilon}}{T} \qquad -\frac{1}{2} \leqslant \lambda \leqslant \frac{1}{2} \quad (5)$$

where $\hat{\varepsilon}$ is the estimated symbol timing. The Q channel output of the CTL is given by

$$y_{Q_k} = \int_{(k-\frac{1}{2})T+\hat{\varepsilon}}^{(k+\frac{1}{2})T+\hat{\varepsilon}} r(t)\,\mathrm{d}t = \int_{(k-\frac{1}{2})T+\hat{\varepsilon}}^{(k+\frac{1}{2})T+\hat{\varepsilon}} s(t, \varepsilon)\,\mathrm{d}t + \int_{(k-\frac{1}{2})T+\hat{\varepsilon}}^{(k+\frac{1}{2})T+\hat{\varepsilon}} n(t)\,\mathrm{d}t = c_k + N_k \quad (6)$$

where N_k is a zero mean Gaussian random variable with variance $\sigma^2 = N_0 T/2$ and c_k is given by

$$c_k = AT\left[a_{k-1}\left(\frac{1}{2} + \lambda\right) + a_k\left(\frac{1}{2} - \lambda\right)\right] \qquad -\frac{1}{2} \leqslant \lambda \leqslant \frac{1}{2} \quad (7)$$

The error signal is given by

$$e(t) = e_k = y_{Q_k} D \qquad D = \pm 1 \quad (8)$$

One of the key performances of the CTL is the

steady-state timing jitter of λ, which is defined as σ_λ^2. Using the linear theory, σ_λ^2 can be derived once the following two quantities are determined:

① The loop S-curve $g(\lambda)$ as a function of the normalized timing error λ;

② The two-sided spectral density S_N of the equivalent additive noise $n_\lambda(t)$.

The S-curve is, by definition, the statistical average of the error signal over the signal and noise probability distributions, which is defined by

$$g(\lambda) = E_{n,s}[e(t)] = E_{n,s}[(c_k + N_k)D] \tag{9}$$

Substituting c_k into Eq. (9) and performing the necessary averaging over the noise and the data symbols, the S-curve of the CTL can be obtained.

$$g_{CTL}(\lambda) = E_{n,s}[e(t)] = E_{n,s}[(c_k + N_k)D] = 2AT\lambda \quad -\frac{1}{2} \leqslant \lambda \leqslant \frac{1}{2} \tag{10}$$

Using the same method, the S-curve of the DTTL under quasi-squarewave conditions can be obtained.

$$g_{DTTL}(\lambda) = \begin{cases} 2AT\lambda \operatorname{erf}(\sqrt{SNR}(1-2\lambda)) & 0 \leqslant \lambda \leqslant \frac{1}{2} \\ 2AT\lambda \operatorname{erf}(\sqrt{SNR}(1+2\lambda)) & -\frac{1}{2} \leqslant \lambda \leqslant 0 \end{cases} \tag{11}$$

where SNR $= A^2T/N_0$ denotes the symbol SNR. It is also straightforward to show that the S-curve of the DTTL is an odd function of the normalized timing error.

The slope of the S-curve at the origin represents the loop detector gain

$$K_{g_{CTL}} = 2AT \tag{12}$$

and

$$K_{g_{DTTL}} = 2AT\operatorname{erf}(\sqrt{SNR}) \tag{13}$$

The normalized S-curves of the CTL and the DTTL are shown in Fig. 3. The loop detector gain is an important index, which indicates the loop ability of acquisition and tracking. It is shown that the acquisition and tracking ability of the CTL is better than that of the DTTL. Moreover, the acquisition and tracking ability of the CTL is independent of symbol SNRs while that of the DTTL deteriorates at low symbol SNRs.

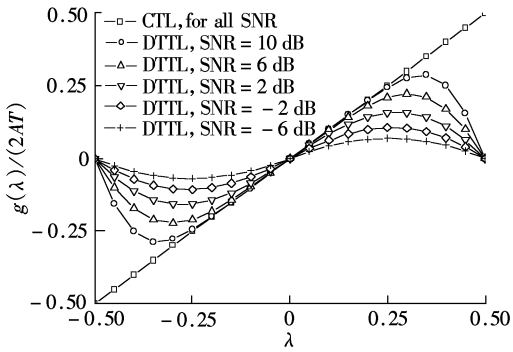

Fig. 3 Normalized S-curves of the CTL and the DTTL

3 Mean-Square Timing Jitter Analysis of CTL and DTTL

For large loop SNR, the linearized loop model is reported in Ref. [20], which is shown in Fig. 4, and the stochastic differential equation that characterizes the operation of the CTL and the DTTL[20] is

$$\frac{\hat{\varepsilon}}{T} = \frac{KF(p)}{p}[g(\lambda) + n_\lambda(t)] \tag{14}$$

where K is the total loop gain, $F(p)$ is the transfer function of the loop filter with p denoting the heaviside operator, and $n_\lambda(t)$ is the equivalent additive noise which characterizes the variation of the loop error signal around its mean.

$$n_\lambda(t) = e(t) - E_{n,s}[e(t)] = e_k - g(\lambda) \tag{15}$$

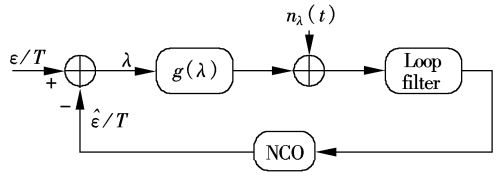

Fig. 4 Linearized loop model for CTL and DTTL

A covariance function that is piecewise linear between the sample values is

$$\begin{aligned} R_n(\tau)\,|_{\tau=mT} &= E_{n,s}[n_\lambda(t)n_\lambda(t+\tau)]\,|_{\tau=mT} = \\ & E_{n,s}[(e_k - g(\lambda))(e_{k+m} - g(\lambda))] = \\ & E_{n,s}(e_k e_{k+m}) - g^2(\lambda) = R(m,\lambda) \\ & m = 0, \pm 1, \pm 2, \ldots \end{aligned} \tag{16}$$

For the loop bandwidth which is small compared to the reciprocal of the chip time interval, $n_\lambda(t)$ can be approximated by a delta-correlated process with equivalent flat power spectral density

$$S_N = \int_{-\infty}^{\infty} R_n(\tau)\,\mathrm{d}\tau = T\left[R(0,\lambda) + 2\sum_{m=1}^{\infty} R(m,\lambda)\right] \tag{17}$$

For the CTL, it can be obtained that

$$e_k^2 = [(c_k + N_k)D]^2 = (c_k + N_k)^2 = c_k^2 + 2c_kN_k + N_k^2 \tag{18}$$

and

$$\begin{aligned} R(0,\lambda) &= E_{n,s}[e_k^2] - g^2(\lambda) = \\ & E_{n,s}[c_k^2] + E_{n,s}[N_k^2] - g^2(\lambda) = \\ & 4A^2T^2\lambda^2 + \sigma^2 - 4A^2T^2\lambda^2 = \sigma^2 = \frac{N_0T}{2} \end{aligned} \tag{19}$$

$$R(m,\lambda) = 0 \qquad m = \pm 1, \pm 2, \ldots \tag{20}$$

Thus, the power spectrum of the loop error signal of the CTL is

$$S_{N\,CTL} = TR(0,0) = \frac{N_0T^2}{2} \tag{21}$$

Using the same method, the following results of the DTTL under quasi-squarewave conditions can be obtained.

$$S_{N\mathrm{DTTL}} = TR(0,0) = \frac{N_0 T^2}{4}[1 + \mathrm{erf}^2(\sqrt{\mathrm{SNR}})] \tag{22}$$

With the power spectrum of the loop error signal, the mean square timing jitter σ_λ^2 of the CTL and the DTTL can be obtained. For conditions of a first-order loop ($F(p) = 1$), a large loop SNR and a one-sided loop bandwidth B_L, from the general theory of PLL[5], we can obtain

$$\sigma_\lambda^2 = \frac{S_N 2B_\mathrm{L}}{K_g^2} \tag{23}$$

Making the appropriate substitutions in Eq. (23), the mean square timing jitters of the CTL and the DTTL are

$$\sigma_{\lambda\,\mathrm{CTL}}^2 = \frac{N_0 B_\mathrm{L}}{4A^2} = \frac{B_\mathrm{L} T}{4\mathrm{SNR}} \tag{24}$$

$$\sigma_{\lambda\,\mathrm{DTTL}}^2 = \frac{N_0 B_\mathrm{L}[1 + \mathrm{erf}^2(\sqrt{\mathrm{SNR}})]}{8A^2\mathrm{erf}^2(\sqrt{\mathrm{SNR}})} = \frac{B_\mathrm{L} T[1 + \mathrm{erf}^2(\sqrt{\mathrm{SNR}})]}{8\mathrm{SNR}\,\mathrm{erf}^2(\sqrt{\mathrm{SNR}})} \tag{25}$$

The normalized mean-square timing jitter performances of the CTL and the DTTL are shown in Fig. 5. The numerical results clearly illustrate the superior performance of the CTL at a low symbol SNR.

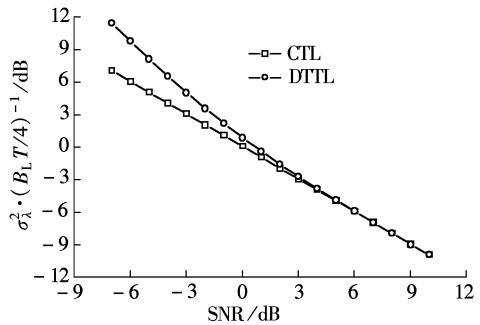

Fig. 5 Normalized mean-square timing jitter performances of the CTL and the DTTL

4 Conclusion

This paper presents a novel chip tracking loop used for regenerative PN ranging clock recovery. For the first-order loop, under the condition of quasi-squarewave PN ranging code, the mean square timing jitter performance of the CTL is analyzed. The tracking performances of the CTL and the DTTL are compared over a wide range of symbol SNRs. It is shown that the CTL and the DTTL have the same performance at a large symbol SNR, while at a low symbol SNR, the former offers a noticeable enhancement.

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用于再生伪码测距时钟恢复的新型码片跟踪环性能分析

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摘要:为了提高低信噪比条件下再生伪码测距系统中的复合伪码时钟恢复性能,采用了一种新型的码片跟踪环.此码片跟踪环是一种改进型的数据转换跟踪环,两者之间的区别在于,码片跟踪环的Q路输出直接乘上了时钟分量,而数据转换跟踪环乘上了I路的转换检测器输出.在准方波伪码测距信号的情况下,详细分析了码片跟踪环的跟踪(均方定时抖动)性能.分析对比了不同码片信噪比条件下的码片跟踪环和数据转换跟踪环跟踪性能.分析表明,码片跟踪环和数据转换跟踪环在大信噪比条件下性能一致;而在小信噪比条件下,码片跟踪环性能明显好于数据转换跟踪环.

关键词:时钟恢复;跟踪环路;伪码测距;数据转换跟踪环;码片跟踪环

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