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Function electrical stimulation circuit for neural signal regeneration system

Wang Jue[1,2] Li Wenyuan[1] Wang Zhigong[1]

([1]Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

([2]College of Integrated Circuits, Southeast University, Nanjing 210096, China)

Abstract: A low-power, high-gain circuit for function electrical stimulation (FES) is designed for the microelectronic neural signal regeneration system based on CSMC (CSMC Technologies Corporation) 0.6 μm CMOS (complementary metal-oxide-semiconductor transistor) technology. It can be used to stimulate microelectrodes connected with the nerve bundles to regenerate neural signals. This circuit consists of two stages: a full differential folded-cascode amplifier input stage and a complementary class-AB output stage with an overload protection circuit. The rail-to-rail input and output stages are used to ensure a wide range of input and output voltages. The simulation results show that the gain of the circuit is 81 dB; the 3 dB-bandwidth is 295 kHz. The chip occupies a die area of 1.06 mm × 0.52 mm. The on-wafer measurement results show that under a single supply voltage of +5 V, the DC power consumption is about 7.5 mW and the output voltage amplitude is 4.8 V. The chip can also run well under single supply voltage of +3.3 V.

Key words: low-power; rail-to-rail; neural signal; voltage drive

After nerve bundles are injured, the upper or lower neurons of damaged surfaces are still subsistent. However, the organism has lost related motorial and sensory functions, since neural signal channels are interrupted[1–3]. In theory, if implant compatible integrated circuit chips are used to replace necrotic or seriously damaged nerves as well as to realize functions of the organism based on the electrical properties of neurons, an artificial channel will be built which may reach the goal of reconstructing neural functions. In the neural signal regeneration system, the microelectrode functions as neural signal detectors and actuators. It exchanges signal with nerve bundles through coupling with bioelectricity[4]. The microelectrode is an interface of the circuit to the organism, so it is a very important component[1]. In this paper, an output voltage circuit is designed to generate a high swing voltage signal that can stimulate the microelectrode to regenerate neural signals. According to the characteristics of neural signals[5], the gain should be above 80 dB, and the frequency response bandwidth should be much wider than the highest frequency of the neural signals. The application is considered to be an in-body embedded electronic system. This design is focused on effective driving and is monolithic without any off-chip pieces.

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Biographies: Wang Jue(1983—), female, graduate; Li Wenyuan(corresponding author), male, doctor, associate professor, lwy555@seu.edu.cn.

1 Circuit Design

1.1 Full differential folded-cascode amplifier

The schematic of the full differential folded-cascode amplifier is shown in Fig. 1. M_{1a} together with M_{1b} compose complementary NMOS differential pairs, and M_{2a} together with M_{2b} compose complementary PMOS differential pairs. $M_{5a(b)}$-$M_{6a(b)}$ and $M_{7a(b)}$-$M_{8a(b)}$ compose cascode current sinks. $M_{12a(b)}$-$M_{15a(b)}$ with complementary differential pairs compose a full differential folded-cascode amplifier circuit.

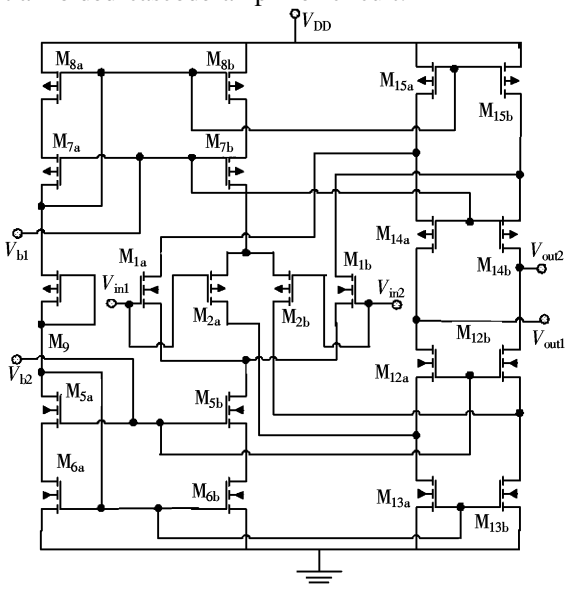


Fig. 1 Schematic of the full differential folded-cascode amplifier

1.1.1 Complementary differential input pair

The input stage is made up of two complementary NMOS and PMOS differential pairs to achieve the full swing of V_{cm}, which is the common mode input voltage. The schematic is shown in Fig. 2. M_{1a} and M_{1b} compose an NMOS differential pair, and $I_{N\text{-bias}}$ is their current source. Similarly, M_{2a} and M_{2b} compose a PMOS differential pair, and $I_{P\text{-bias}}$ is their current source. For the N-channel CMOS differential pair, the common-mode input can approach V_{DD}, but its negative end is far from V_{SS}. On the contrary, for the P-channel CMOS circuit, the common-mode input can approach V_{SS}, but its positive end is far from V_{DD}. So if one complements the N-channel different pairs with the P-channel different pairs, the common mode input range can reach from V_{SS} to V_{DD}[6-7].

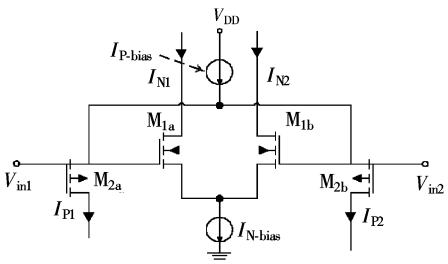


Fig. 2 Complementary differential input pair

1.1.2 Current sink circuit

The schematic picture of the current sink circuit is shown in Fig. 3. $M_{5a(b)}$ and $M_{6a(b)}$ have the same ratios. Hence, the current through M_{5a} and M_{6a} must be equal to the current through M_{5b} and M_{6b}, which means $I_O = I_{bias}$.

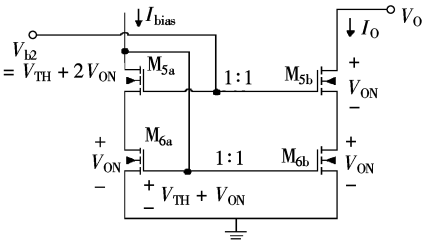


Fig. 3 High-swing cascode current sink

Assume that the gate voltage of M_{6a} equals $V_{TH} + V_{ON}$. Apparently, $V_{b2} = V_{TH} + 2V_{ON}$[8]. So the current sink will reduce the common mode input range to

$$V_{cm} \geqslant V_O + V_{TH} = 2V_{ON} + V_{TH} = V_{b2} \qquad (1)$$

The PMOS current sink has the same structure, so the currents through $M_{7a(b)}$ and $M_{8a(b)}$ are equal to I_{bias}, and will reduce the common mode input range to $V_{cm} \leqslant V_{b1}$.

V_{ON} can be made comparatively small, which guarantees a large common-mode input range and creates a reduction in the current circuit.

1.1.3 Full differential folded-cascode amplifier

When all transistors are active, because of the effect of the current sink, $M_{1a(b)}$ and $M_{2a(b)}$ have the same current which equals $I_{bias}/2$. From Fig. 1, the current through $M_{15a(b)}$ should be $I_{bias}/2$ more than $M_{14a(b)}$ and the current through $M_{12a(b)}$ should also be $I_{bias}/2$ more than $M_{13a(b)}$.

Connect the grid of $M_{15a(b)}$ with M_{8a}, $M_{14a(b)}$ with M_{7a}, $M_{13a(b)}$ with M_{5a} and $M_{12a(b)}$ with M_{6a}. $M_{15a(b)}$, M_{8a} and M_{7a} have the same ratios which are twice $M_{14a(b)}$. Similarly $M_{12a(b)}$, M_{6a} and M_{5a} have the same ratios which are twice $M_{13a(b)}$. Apparently, the currents through $M_{15a(b)}$ and $M_{12a(b)}$ equal I_{bias}, which are $I_{bias}/2$ more than $M_{13a(b)}$ and $M_{12a(b)}$, so the amplifier can work normally.

1.2 Rail-to-rail output stage

The output stage is made up of two error amplifiers (AMP1 and AMP2), M1 and M2, as shown in Fig. 4. AMP1 and AMP2 are used to detect as well as to reduce the voltage difference between input and output. M1 and M2 are connected as a common source form to achieve full swing output. The output resistance will be far less than the r_o of M1 in parallel with the r_o of M2, because of negative feedback through AMP1 and AMP2. And increasing the gain of error amplifiers will reduce the output resistance[9].

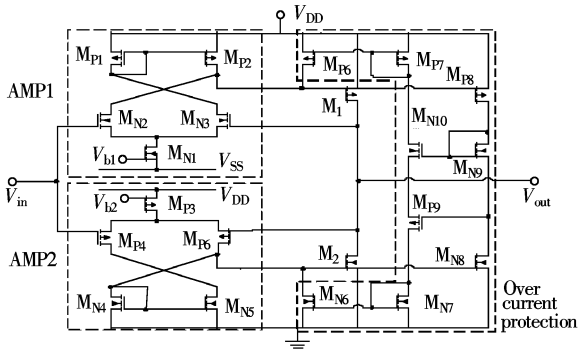


Fig. 4 Complementary class-AB output stage with over current protection

In order to prevent the device being destroyed due to large output signals, the complementary Class-AB output stage is optimized by a protective circuit which is composed of $M_{N(P)6}$-$M_{N(P)10}$. M1 and M2 are mirrored by M_{P8} and M_{N8}, and currents through M_{P8}, M_{N8}, and M_{N9} are equal since these transistors are connected in series. When working normally, the current through M_{N9} is less. However, when the output signal becomes larger, the drain source voltage of M_{N9} will exceed the sum of the threshold voltages of M_{N10} and M_{P9}. The ratio of M_{N9} is much smaller than those of M_{N10} and M_{P9}, so M_{N10} and M_{P9} are sensitive to the drain source voltage change of M_{N9}. Moreover, the current flowing through M_{N10} and M_{P9} is mirrored in M_{N7}, M_{N6}, M_{P7}

and M_{N8}, which reduces the gate-to-source voltage of M1 and M2. Hence, the current through the output transistors becomes smaller to protect the circuit[10].

1.3 Bias circuit

The bias circuit supports bias voltage (V_{b1}, V_{b2}) for the input stage. The schematic picture is shown in Fig. 5.

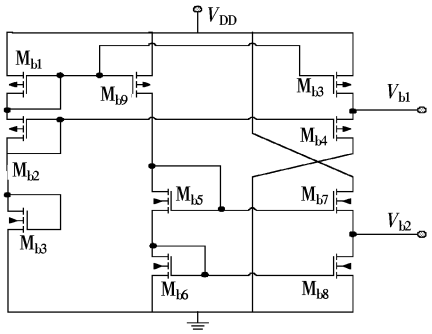


Fig. 5 Bias circuit

All of the P-channel and N-channel transistors have the same ratios, except that the ratio of M_{b2} is only 1/4 of the other P-channel transistors and the ratio of M_{b5} is only 1/4 of the other N-channel transistors.

Since M_{b6} is working in the saturation region, assume that its gate voltage is equal to $V_{TH} + V_{ON}$. So the gate voltage of M_{b5} should be $2V_{ON}$ more than M_{b6}. Because M_{b6} and M_{b8} compose a current mirror, $I_{b7} = I_{b5}$. The bias voltage of V_{b2} can be calculated as

$$V_{b2} = V_{G,Mb7} - V_{ON} = V_{G,Mb5} - V_{ON} = (V_{TH} + V_{ON} + 2V_{ON}) - V_{ON} = V_{TH} + 2V_{ON} \quad (2)$$

Similarly, V_{b1} is equal to $V_{DD} - (V_{TH} + 2V_{ON})$.

2 Simulation Result

The key performances of the circuit under a single supply voltage of +5 V are shown in Tab. 1. The results are based on CSMC 0.6 μm CMOS technology and stimulated by Hspice.

Tab. 1 Circuit key performances

Parameters	Measured results
Open-loop gain/dB	81.42
3 dB-bandwidth/kHz	295
Power dissipation/mW	8.9
Output resistance/Ω	12.7
PSRR +/dB	82.7
PSRR −/dB	85
CMRR/dB	99

AC analysis results under a supply voltage of +5 V are shown in Fig. 6.

3 Test Result

The chip micrograph is shown in Fig. 7, and its die area is 1.06 mm × 0.52 mm. The equipment used in this test include: Agilent 33220A function/arbitrary waveform generator, Agilent E4438C ESG vector signal generators and Tektronix TDS5104 oscillograph.

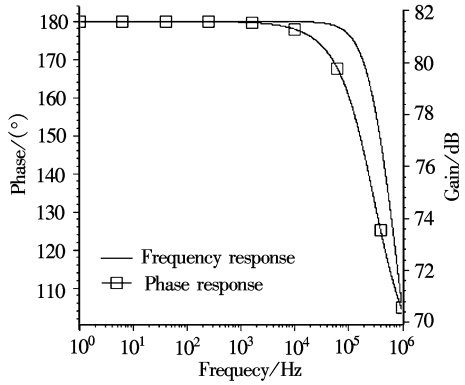


Fig. 6 Frequency response of open-loop transfer function

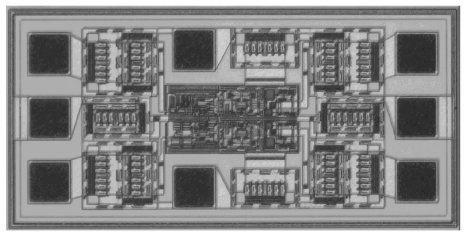
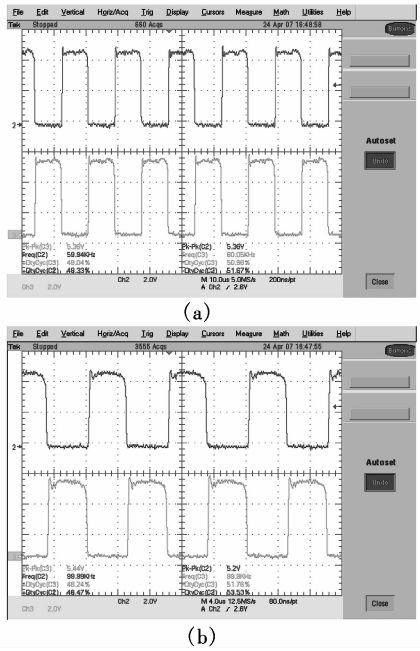


Fig. 7 Micrograph of the chip

Under a single supply voltage of +5 V, the whole circuit provides a low-power consumption of 7.5 mW and the output amplitude can achieve 4.8 V. Moreover, the circuit can work when the common-mode input varies from 1 to 4 V. The chip can also run well when supply voltage falls to +3.3 V, with a power consumption of 2.64 mW and a 3.2 V output amplitude.

Fig. 8 shows the output waveforms at different frequencies where input signals are a square-wave of 2.5 V DC level and a 50 mV amplitude.



(a) (b)

Fig. 8 Output signal waveforms at different frequencies of input signal. (a) 60 kHz; (b) 100 kHz

4 Conclusion

A voltage driving monolithic circuit with low power, high gain and wide common-mode input range advantages is realized based on CSMC 0.6 μm CMOS technology. The structure and the principle of this circuit are described. Finally, the simulation and test results are displayed. The circuit is expected to be applied in the neural signal regeneration system in an in-body mode to stimulate electrodes.

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用于神经信号再生的神经功能电压驱动电路

王 珏[1,2] 李文渊[1] 王志功[1]

([1] 东南大学射频与光电集成电路研究所,南京 210096)

([2] 东南大学集成电路学院,南京 210096)

摘要:采用华润上华 0.6 μm CMOS 工艺,设计实现了一种用于神经信号再生微电子系统的低功耗、高增益功能电激励电压驱动电路. 它可以用于驱动激励电极和与之相连的神经来再生神经信号. 电路由 2 部分组成:全差分折叠式共源共栅放大器及带过载保护的互补型甲乙类输出级. 电路采用了满摆幅的输入输出结构,保证了大输入电压范围和大输出电压范围. 仿真结果表明,电路增益可以达到 81 dB,具有 295 kHz 的 3 dB 带宽. 芯片面积为 1.06 mm × 0.52 mm. 经流片实现后在片测试,在单电源 +5 V下工作,直流功耗约为 7.5 mW,输出电压幅度达到 4.8 V;同时在单电源 +3.3 V 下也可正常工作.

关键词:低功耗;满摆幅;神经信号;电压驱动

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