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10 Gbit/s PRBS tester implemented in FPGA

Miao Peng Wang Zhigong

(Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

Abstract: The design of an FPGA(field programmable gate array) based programmable SONET (synchronous optical network) OC-192 10 Gbit/s PRBS (pseudo-random binary sequence) generator and a bit interleaved polarity 8 (BIP-8) error detector is presented. Implemented in a parallel feedback configuration, this tester features PRBS generation of sequences with bit lengths of $2^7-1, 2^{10}-1, 2^{15}-1, 2^{23}-1$ and $2^{31}-1$ for up to 10 Gbit/s applications with a 10 Gbit/s optical transceiver, via the SFI-4 (OC-192 serdes-framer interface). In the OC-192 frame alignment circuit, a dichotomy search algorithm logic which performs the functions of word alignment and STM-64/OC192 de-frame speeds up the frame sync logic and reduces circuit complexity greatly. The system can be used as a low cost tester to evaluate the performance of OC-192 devices and components, taking the replacement of precious commercial PRBS testers.

Key words: bit interleaved polarity 8 (BIP-8); synchronous digital hierarchy (SDH); framer; field programmable gate array (FPGA); pseudo-random binary sequence (PRBS)

Reliable testing at 10 Gbit/s has become a major issue in the development of high speed optical fiber communication systems (e. g., SONET OC-192) and related high-speed components. PRBS (pseudo random binary sequence) standardized by ITU O. 151 is used for this application[1]. However, the commercially available PRBS test equipment is often an impediment to application due to high costs.

BIP-8 is a method used for error monitoring where each bit of the BIP-8 code word or byte corresponds to even parity as calculated across matching bit positions for the distinct bytes in a SONET frame[2]. A low cost FPGA-based PRBS generator and a BIP-8 error block detector are set up. The PRBS test system is integrated with a commercial FPGA (Stratix GX EP1S25-FF1020C6)[3] and a 10 Gbit/s optical transceiver (Intel TXN13303 2103A01)[4].

Fig. 1 shows the architecture of the test system. The SFI-4 is transferred duplex with 16 low voltage differential signaling (LVDS) 622.08 Mbit/s signals and a 622.08 MHz LVDS clock[5]. Therefore, an aggregate of 9 953.28 Mbit/s is transferred in each direction. In the TX direction, the PRBS generator and the OC-192 framer generate OC-192 frame structure with frame delimiter 192 A1 and A2, BIP-8 words, and PRBS payloads. Then, the structured frame is transmitted by 4∶1 Mux in FPGA to form SFI-4 signals. In the RX direction, after the 1∶4 demuxed SFI-4 signals are aligned to the OC-192 frame structure, the BIP-8 calculation unit counts bit polarity errors.

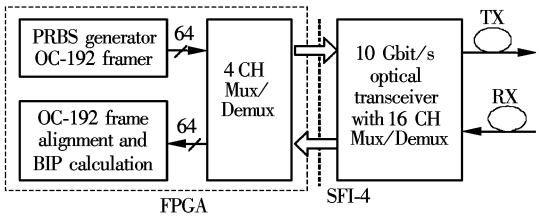

Fig. 1 PRBS test system architecture

1 Test System Architecture

1.1 PRBS generator

Conventionally, a PRBS generator consists of a liner feedback shift register (LFSR) chain. With the bit rate increasing, the clock frequency should be speeded up to trigger out the high speed sequence. However, to achieve operation speeds as high as 10 Gbit/s, the propagation delay of traditional DFF LFSR becomes extremely stringent. Furthermore, boosting up the clock frequency causes drastic power consumption.

As a solution to the problem, a parallel PRBS generator structure is put forward. As shown in Fig. 1, the parallel PRBS generator consists of two-stage Mux (namely 64∶1) and 64 DFF cells running at a 1/64 speed of OC-192 (155.520 MHz). According to the *m*-sequence sampling theorem, a necessary and efficient condition for $\{a_{sk}\}$ sequence shift and equal to an *m*-sequence $\{a_k\}$ of length $L=2^n-1$ is the existence of an integer $r, 0 \leqslant r \leqslant n-1$, which produces $s=2^r \pmod L$[6].

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Biography: Miao Peng(1972—), male, doctor, lecturer, miaopeng123@hotmail.com.

So, based on the *m*-sequence sampling theorem, the proposed structure of the parallel PRBS generator core is shown in Fig. 2. The 64 DFF cells are connected in parallel feedback configuration, with each Q output $2\pi/64$ phase difference.

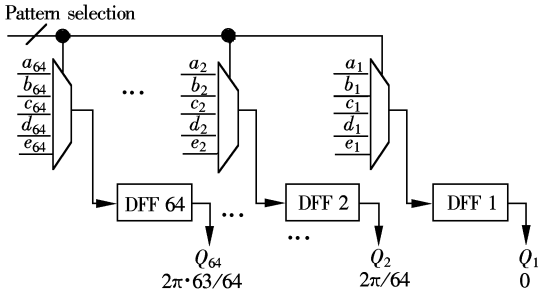

Fig. 2 Parallel PRBS generator core

According to ITU O. 151 recommendations, PRBS of lengths, 2^7-1, $2^{10}-1$, $2^{15}-1$, $2^{23}-1$, and $2^{31}-1$ polynomials are listed as follows:

$$f_7(x) = x^7 + x + 1$$
$$f_{10}(x) = x^{10} + x^3 + 1$$
$$f_{15}(x) = x^{15} + x + 1$$
$$f_{23}(x) = x^{23} + x^5 + 1$$
$$f_{31}(x) = x^{31} + x^3 + 1$$

In Fig. 2, $i + x$ stands for $i + x$ mod 64. So, they can be listed as

If $n = 7$, let $a_i = Q_{i+57}$ XOR Q_{i+58}, $i = [1 \ldots 64]$;

If $n = 10$, let $b_i = Q_{i+54}$ XOR Q_{i+57}, $i = [1 \ldots 64]$;

If $n = 15$, let $c_i = Q_{i+49}$ XOR Q_{i+50}, $i = [1 \ldots 64]$;

If $n = 23$, let $d_i = Q_{i+41}$ XOR Q_{i+46}, $i = [1 \ldots 64]$;

If $n = 31$, let $e_i = Q_{i+33}$ XOR Q_{i+36}, $i = [1 \ldots 64]$.

The pattern selecting signal is used to select different PRBS patterns.

1.2 Mark density generator

The output of the core Q along with the mark density selecting signals are fed to the mark density generator. The variable mark density generator is built on the simple idea that "and"ing a PRBS stream with a delayed version of itself would produce a stream with an average mark ratio of 1/4. In a regular PRBS stream, Prob(0) = Prob(1) = 1/2. When two adjacent bits are "and"ed, a "1" appears at the output only if both bits are 1s. So, Prob(1) = (1/2) × (1/2) = 1/4. (This probability calculation assumes that the sequence is uncorrelated with a delayed version of itself, which is true in the case of PRB sequences.) This idea can be used to generate sequences with mark ratios of 1/8, 1/16, and so on. In this way, mark ratios of 1/4 and 1/8 can be generated. The actual circuit used is shown in Fig. 3. Tab. 1 shows the function of mark density control logic.

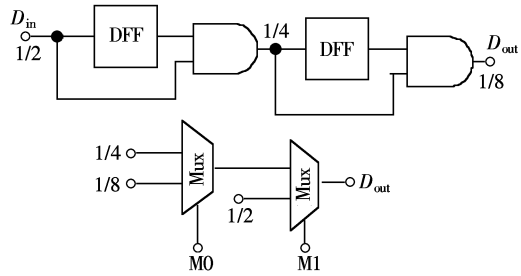

Fig. 3 Mark density control logic

Tab. 1 Function of mark density control logic

M0	M1	Mark density
X	1	1/2
0	0	1/4
1	0	1/8

1.3 OC-192 framer

The transmitter contains a PRBS generator which is capable of generating various PRBS patterns as required for system and chip level testing. In the TX direction, Q_1 to Q_{64} PRBS output succeeding OC-192 delimiter 192 A1(F6H), 192 A2(28H) and 4-BIP word are mapped onto four parallel channels. The BIP is calculated (XOR) on each bit of previous channel frame data.

1.4 OC-192 frame alignment logic

In the RX direction, the FPGA receives a 16-bit 622 Mbit/s LVDS electrical signal from the OC-192 framer chip as defined in OIF99. 102. The RX block diagram is illustrated in Fig. 4.

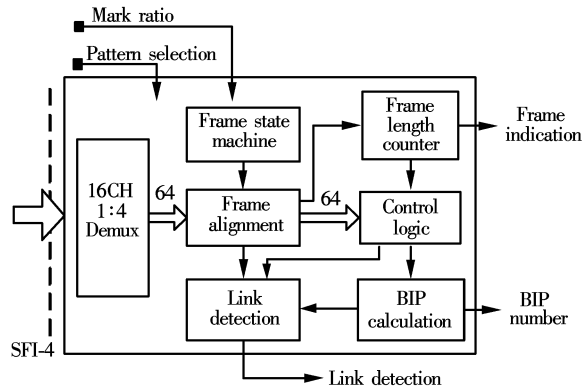

Fig. 4 RX block diagram

In Fig. 4, the SFI-4 OC-192 data is 1∶4 demuxed to frame alignment logic, which plays an important role in the Mux/Demux system to detect the A1A2 transition in the incoming data frame. Conventional framing approaches operate in serial or parallel manner to search frame synchronous code (FSC) A1A2[7-8]. However, with the increment in data bus width, these strategies impose strict timing constraints on the related circuits which, in turn, leads to the substantial increment in the frame system design complexity.

A dichotomy search algorithm logic to perform word alignment and OC192 de-frame speeds up the alignment circuit working speed and reduces circuit complexity greatly[9]. The block diagram is shown in Fig. 5.

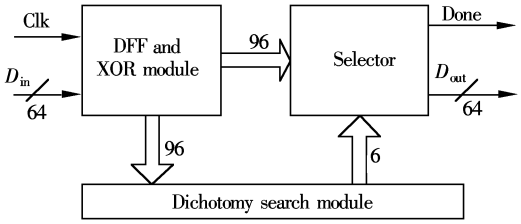

Fig. 5 Dichotomy search logic

If 192 A1 in an OC-192 data stream are divided into data groups by every 64 bit width, there are at least 23 same-data groups. So, the XOR results of current groups and previous groups will be all zeros. Once the first A2 arrives, the XOR results of current groups and previous groups will not be all zeros. The first "1" appears in the XOR results indicating the boundary of A1 and A2. While the first "1" after 23 consecutive non-zero groups appears, the dichotomy search logic can locate the position of the first "1", namely the boundary of A1 and A2. By comparing with ordinary frame alignment logic, the complexity of the dichotomy frame alignment circuit is reduced from N stage to $\log_2 N$ stage, where N is the Demux ratio, which speeds up the circuit working speed and reduces circuit complexity greatly.

The frame state machine (FSM) is used to detect the out-of-frame (OOF) state every 125 μs[10]. Thus, the frame alignment logic can indicate frame signal even if in a low bit error rate (BER), e. g. 10^{-4}.

1.5 Link detection

Fig. 6 shows the state diagram of the link detection logic implemented in the pattern checker. The link detection logic monitors the number of error blocks in the received data at each cycle to report the link status.

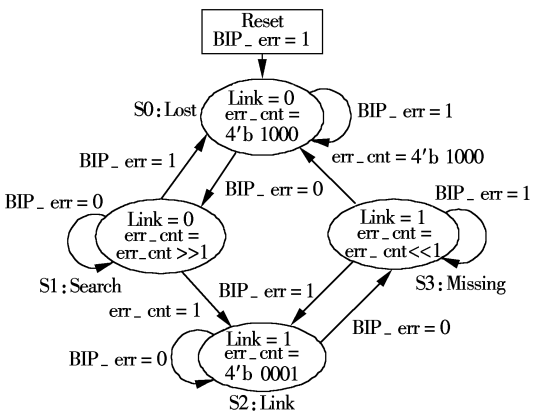

Fig. 6 Link detection FSM

The logic declares a "link up" whenever it finds error-free incoming data for seven or more consecutive clock cycles. It declares a "link down" whenever it finds one or more error blocks at each cycle for seven or more consecutive clock cycles. The link status remains unchanged under all other conditions. The link detection logic filters out any scattered random bit errors occurring at a medium or low BER to keep the link relatively stable during a BER test[11].

1.6 BIP block

The BIP-8 check result is located right after the end of A2 in every OC-192 data frame. In the TX direction, the parity calculation is performed (XOR) over the previously entire SONET/SDH frame including both payload (e. g. PRBS) and overhead (e. g. A1A2) octets. At the end of each frame the running calculation is compared with the received BIP-8 and an error count is generated.

2 Test System

Fig. 7 shows the photograph of the test system. The framer-serdes interface (FSI) between the 10 Gbit/s optical transceiver and the FPGA is OIF99. 102 compliant and the TX and RX ports of the optical transceiver can be connected to OC-192 components or self looped. Eventually, a bit error rate test at 10 Gbit/s is performed using the sequence of 2^7-1, $2^{10}-1$, $2^{15}-1$, $2^{23}-1$ and $2^{31}-1$ bits. After a sequence of error has been intentionally generated in several frame data, the BIP-8 error checker counters total error blocks.

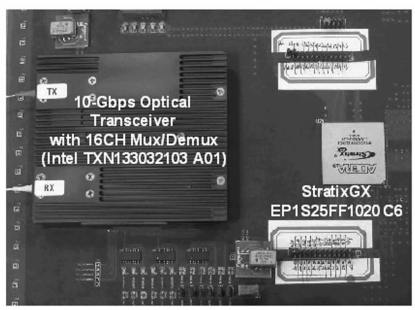

Fig. 7 Test system photograph

3 Conclusion

An FPGA based 10 Gbit/s PRBS test system has been implemented which is suitable for the performance evaluation of OC-192 devices and systems. Compared with the commercial 10 Gbit/s test system ADVANTEST D3186, test results show that BIP error blocks are at the same grade as in the FPGA PRBS test. The programmable parallel PRBS generator per-

forms as an LFSR function with a total 1∶64 demultiplexer, which reduces the clock rate by 64 times, and is more feasible for realization in FPGA. The dichotomy search logic greatly improves the frame alignment performance and the BIP-8 facilitates the built-in self test of OC-192-level devices with very high error detection probability. In conclusion, the test system exhibits a very high practical value in PRBS tests.

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基于 FPGA 的 10 Gbit/s 伪随机序列测试装置

苗 澎　　王志功

(东南大学射频与光电集成电路研究所,南京 210096)

摘要:介绍了一种基于 FPGA 的可编程 SONET OC-192 10 Gbit/s 伪随机序列发生器和比特间插入奇偶校验码 BIP-8 的误码测试仪. 该误码测试仪为并行反馈结构,可生成 PRBS 序列长度为 2^7-1, $2^{10}-1$, $2^{15}-1$, $2^{23}-1$ 和 $2^{31}-1$,通过 SFI-4 接口,采用 10 Gbit/s 收发一体光模块,其工作速率可达 10 Gbit/s. 在 OC-192 帧同步调整电路中,采用 STM-64/OC192 二分查找法的帧同步法,显著提高了帧同步速度并减少了帧同步逻辑的复杂度. 该系统可作为一种低成本的测试仪评估 OC-192 设备与器件,以取代昂贵的商用 PRBS 测试仪.

关键词:比特间插误码;同步数字体系;成帧器;现场可编程逻辑阵列;伪随机序列

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