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Robust CMOS phase frequency detector for high speed and low jitter charge pump PLL

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Abstract: In order to improve the performance of the existing phase frequency detectors (PFDs), a systematical analysis of the existing PFDs is presented. Based on the circuit architecture, both classifications and comparisons are made. A new robust CMOS phase frequency detector for a high speed and low jitter charge pump phrase-locked loop (PLL) is designed. The proposed PFD consists of two rising-edge triggered dynamic D flip-flops, two positive-edge detectors and delaying units and two OR gates. It adopts two reset mechanisms to avoid the UP and DN signals to be logic-1 simultaneously. Thus, any current mismatch of the charge pump circuit will not worsen the performance of the PLL. Furthermore, it has hardly any dead-zone phenomenon in phase characteristic. Simulations with ADS are performed based on a TSMC 0.18-μm CMOS process with a 1.8-V supply voltage. According to the theoretical analyses and simulation results, the proposed PFD shows a satisfactory performance with a high operation frequency ($\approx$1 GHz), a wide phase-detection range [$\pm 2\pi$], a near zero dead-zone ($<$0.1 ps), high reliability, low phase jitter, low power consumption ($\approx$100 μW) and small circuit complexity.

Key words: phase frequency detectors; dead-zone; blind-zone; phase characteristic; frequency characteristic

Charge-pump phase-locked loops (CPPLLs) are widely used for the applications of frequency synthesizers, clock synchronization and clock recovery, etc. The development of these applications brings an increased demand for low-jitter, low-power and high-speed PLLs. One of the key elements in a CPPLL is the phase frequency detector (PFD).

As shown in Fig. 1, the main function of the PFD is to detect and amplify the phase/frequency differences between the reference signal f_{REF} and the divided VCO output signal f_{DIV} at the input ends. UP and DN pulses are produced as the outputs of the PFD according to the phase/frequency differences. The outputs of the PFD will then modify the control voltage for VCO (V_C). So the performance of any PLL circuit is critically dependant on the PFD design.

There are several important design issues concerning the PFD. Among them, the output phase characteristic has the largest impact on the PLL. It is mainly dominated by two issues: dead-zone and blind-zone. The undetectable phase error range near zero phase error is called the dead-zone. It is responsible for increasing phase noise and spurious tones. It is due to the finite transition times of a logic gates, and needs to be avoided. During a reset operation, the PFD is insensitive to any transitions in the input signals. This frequency insensitivity during the reset operation is known as a blind-zone. The blind-zone degrades the maximum phase-detection range of the PFD[1]. However, it is impossible to eliminate the blind-zone completely.

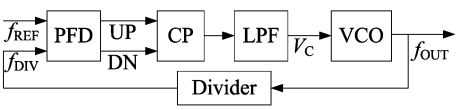

Fig. 1 Typical CPPLL architecture

If both PFD outputs UP and DN have an overlap time of a logic-1 state, this transient state not only increases the power dissipation of PLL, but also makes the PLL be easily affected by an external noise, and, consequently, deteriorate the phrase noise of the PLL, which is called the four-state problem.

The maximum operating frequency is another important characteristic. It influences the performance of PFDs.

1 Theoretical Analysis of Different PFD Architectures

Recently, a significant effort has been made on designing high-speed low-power CMOS PFDs for communications and digital systems. Many novel configurations and design techniques have emerged. An in-depth examination of these techniques, however, is not available. Here, an in-depth examination of the advantages and limitations of these emerging techniques are presented. Critical design issues, such as dead-zone, blind-zone, sensitivity to input data pattern and linear phase error detecting range are investigated in detail.

PFDs are often designed with tri-state techniques based on the concept model depicted in Fig. 2. Usually, a PFD is built with two parts: memory elements such as flip-flops, and the reset generator. The performance of PFDs is critically dependent on the reset generator instead of the memory elements. Different PFDs may have totally different phase/fre-

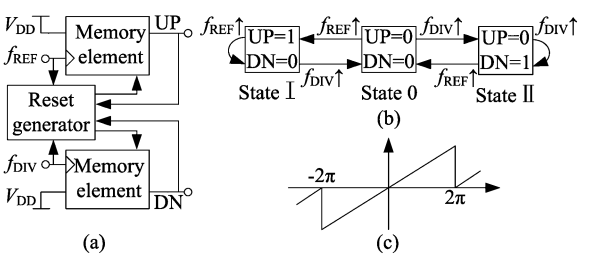

Fig. 2 Concept model of PFDs. (a) Architecture; (b) Finite state-machine; (c) Ideal phase-detecting characteristic

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quency characteristics, only due to the different reset mechanisms used in the PFDs. Here, PFDs are classified into six kinds according to the adopted reset mechanisms.

In order to obtain a correct phase/frequency characteristic which is independent of the duty-cycle of the inputs, a PFD must be positive-edge triggered, instead of negative-edge triggered or level-triggered. Thus, all the PFDs discussed in the following sections are, by default, rising-edge triggered.

For convenience of discussion, we assume that T is the period of the input signals; ρ_R and ρ_V are the duty-cycles of the input signals f_{REF} and f_{DIV}, respectively. Δ is the setting time for charge-pump (CP) switches to turn on (in order to minimize the dead-zone of the PFD, the value of Δ must be minimized; moreover, once the CP is designed, Δ is not a design parameter any more.); τ is the phase error between the two input signals; Δ_{in} is the delay time from the rising-edge of the input signal of one D-flipflop (DFF) to the output of this DFF to be desirably set; $\Delta_{RST,in}$ is the delay time from the rising-edge of the input signal of one DFF to the output of the other DFF which is desirably reset; $\Delta_{RST,out}$ is the delay time from the rising-edge of the output signal of one DFF to the output of the other DFF which is desirably reset.

Obviously, when the dead-zone characteristic of the FPD is under analysis, $\tau \to 0$; however, when the blind-zone characteristic of the FPD is under consideration, $\tau \to T$, and $\Delta_{RST,out}, \Delta_{RST,in}, \Delta_{in} \ll \tau$.

1.1 Class-A PFDs using input-level crosswise reset style

In the PFDs shown in Fig. 3, the delayed f_{REF} and f_{DIV} are used to crosswise reset the other DFF asynchronously.

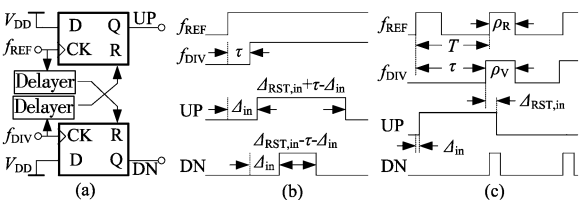

Fig. 3 PFDs using input-level crosswise reset style. (a) PFD architecture; (b) Dead-zone; (c) Blind-zone

For these PFDs, if $\Delta \leqslant \Delta_{RST,in} - \tau - \Delta_{in}$, there is no dead-zone but the four-state problem; and if $\Delta_{RST,in} - \tau - \Delta_{in} < \Delta \leqslant \tau + \Delta_{RST,in} - \Delta_{in}$, there is no dead-zone and no four-state problem; or else, the PFDs have a non-zone dead-zone.

Suppose that f_{REF} leads f_{DIV}, the PFD enters its blind-zone, when $\tau + \rho_V + \Delta_{RST,in} \geqslant T + \Delta_{in}$. Vice versa, when f_{DIV} leads f_{REF} and $\tau + \rho_R + \Delta_{RST,in} \geqslant T + \Delta_{in}$, the PFD enters the blind-zone.

The disadvantages of this kind of PFD include large blind-zone, relative small linear phase-detecting range, which, moreover, depends on the duty-cycle of the inputs. For instance, in the case of $\rho_R = \rho_V = T/2$, the blind-zone is as large as $\tau \geqslant T/2 + \Delta_{in} - \Delta_{RST,in} > T/2$, because of $\Delta_{in} < \Delta_{RST,in}$, in order to avoid the dead-zone. The linear phase-detecting range is obviously smaller than $[\pm\pi]$.

1.2 Class-B PFDs using output-level feedback reset style

In the PFDs shown in Fig. 4, the output of UP AND with DN is delayed to reset the DFFs synchronously.

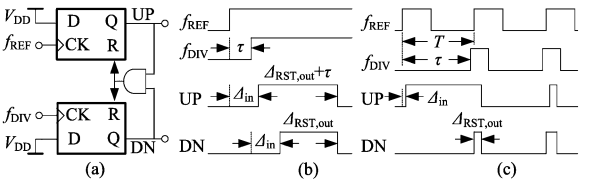

Fig. 4 PFDs using output-level feedback reset style. (a) PFD architecture; (b) Dead-zone; (c) Blind-zone

For these PFDs, if $\Delta \leqslant \Delta_{RST,out}$, there is no dead-zone but the four-state problem; and if $\Delta_{RST,out} < \Delta \leqslant \tau + \Delta_{RST,out}$, there is no dead-zone and no four-state problem; or else, PFDs have a non-zone dead-zone. When $\tau + \Delta_{RST,out} > T$, the PFD enters its blind-zone.

This kind of PFD has a linear phase-detecting range as large as $[\pm(2\pi - \Delta_{RST,out})]$, which, moreover, is independent of the duty-cycle of the inputs. However, these PFDs cannot avoid the dead-zone and the four-state problem simultaneously.

1.3 Class-C PFDs using output-level crosswise feedback reset style

In the PFDs shown in Fig. 5, the outputs UP and DN are delayed and crosswise fed back to reset the DFFs asynchronously.

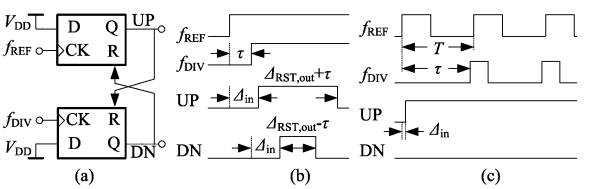

Fig. 5 PFDs using output-level crosswise feedback reset style. (a) PFD architecture; (b) Dead-zone; (c) Blind-zone

For these PFDs, there is no dead-zone but the four-state problem, if $\Delta \leqslant \Delta_{RST,out} - \tau$; and there is no dead-zone and no four-state problem, if $\Delta_{RST,out} - \tau < \Delta \leqslant \tau + \Delta_{RST,out}$; or else, PFDs have a non-zone dead-zone. However, they are not tri-state PFDs and cannot correctly detect the phase error between two inputs.

1.4 Class-D PFDs using input rising-edge crosswise forward reset style

In the PFDs shown in Fig. 6, the inputs f_{REF} and f_{DIV} are rising-edge detected and delayed to crosswise reset the DFFs asynchronously.

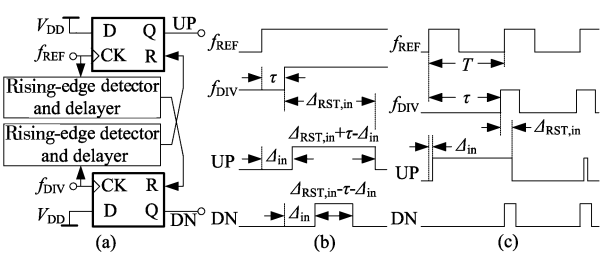

Fig. 6 PFDs using input rising-edge crosswise forward reset style. (a) PFD architecture; (b) Dead-zone; (c) Blind-zone

For these PFDs, there is no dead-zone but the four-state problem, if $\Delta \leqslant \Delta_{RST,in} - \tau - \Delta_{in}$; and there is no dead-zone

and no four-state problem, if $\Delta_{RST,in} - \tau - \Delta_{in} < \Delta \leqslant \Delta_{RST,in} + \tau - \Delta_{in}$; or else, these PFDs have a non-zone dead-zone. But they are also not tri-state but two-state PFDs and cannot correctly detect the phase error between two inputs.

1.5 Class-E PFDs using both A and C reset styles

In the PFDs shown in Fig. 7, the delayed inputs f_{REF} and f_{DIV} combine with the output of the corresponding DFF using an OR gate, respectively, and then reset the other DFFs in a crosswise mode asynchronously.

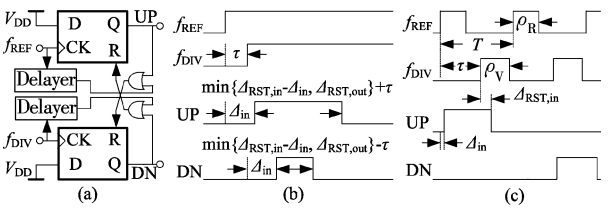

Fig. 7 PFDs using both A and C reset styles. (a) PFD architecture; (b) Dead-zone; (c) Blind-zone

Similar to the class-A PFDs, the disadvantages of this kind of PFD include a large blind-zone, a relative small linear phase-detecting range, which, moreover, depends on the duty-cycle of the inputs.

1.6 Class-F PFDs using both D and C reset styles

In the PFDs shown in Fig. 8, the inputs f_{REF} and f_{DIV} are rising-edge detected and delayed, and then combine with the output of the corresponding DFF using an OR gate, respectively, and then reset the other DFFs in a crosswise mode asynchronously.

For these PFDs, there is no dead-zone but the four-state problem, if $\min\{\Delta_{RST,out} - \tau, \Delta_{RST,in} - \tau - \Delta_{in}\} > \Delta$; and there is no dead-zone and no four-state problem, if $\min\{\Delta_{RST,out} - \tau, \Delta_{RST,in} - \tau - \Delta_{in}\} < \Delta \leqslant \min\{\tau + \Delta_{RST,out}, \tau + \Delta_{RST,in} - \Delta_{in}\}$; or else, PFDs have a non-zone dead-zone. When $\Delta_{RST,in} - \Delta_{in} + \tau > T$, the PFD enters the blind-zone. This kind of PFD has a linear phase-detecting range as large as $[\pm(2\pi - \min\{\Delta_{RST,out}, \Delta_{RST,in} - \Delta_{in})]$, which, moreover, is independent of the duty-cycle of the inputs.

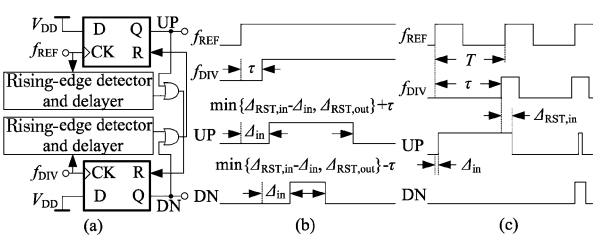

Fig. 8 PFDs using both D and C reset styles. (a) PFD architecture; (b) Dead-zone; (c) Blind-zone

1.7 Comparisons of these six kinds of PFDs

Based on the theoretical analysis above, we can know that the PFDs of class-A and -E have large blind-zones and narrow linear phase-detecting ranges depending on the duty-cycle of the inputs; the PFDs of class-C and -D have poor phase characteristics and cannot correctly detect the phase errors between the two inputs; the PFDs of class-B and -F have good phase characteristics independent of the duty-cycle of the inputs, but the PFDs of class-B cannot avoid the dead-zone and the four-state problem simultaneously. Thus, the class-F PFD is the best one.

2 Conventional PFD Architectures

The DFFs in the PFD proposed in Ref. [2], the difference phase frequency detector (dd-PFD)[3], the Fs-PFD[4] and the double-edge-checking PFD (dec-PFD)[5] are not designed to be operated in the positive-edge triggered mode, so these PFDs have a phase characteristic dependent on the duty-cycle of the inputs.

The conventional PFD (con-PFD), the TSPC PFD[6], the pass-transistor DFF PFD[7] and the PFD with dynamic CMOS logic[8] belong to class-B PFD, and they have good phase characteristics independent of the duty-cycle of the inputs, but cannot avoid dead-zones and the four-state problem simultaneously. The PFD proposed in Ref. [9], the high-speed PFD[10] and the pt-type PFD[11] belong to class-E PFDs, and they have large blind-zones, relatively small linear phase-detecting ranges, which, moreover, dependent on the duty-cycle of the inputs.

A non-clocked phase frequency detector (nc-PFD)[12] belongs to class-A PFD, so it has a phase characteristic dependent on the duty cycle of the inputs and serious four-state problem.

As we know, all the above-mentioned PFDs have such-and-such disadvantages, such as large blind-zone, small phase-detecting range, the four-state problem or dependence on the duty-cycle of the inputs etc.

3 Circuit Structure and Operating Principle of the Proposed PFD

In order to overcome the shortcomings of the above-mentioned PFDs, a new tri-state PFD is proposed based on the concept model of the class-F PFD, shown in Fig. 9.

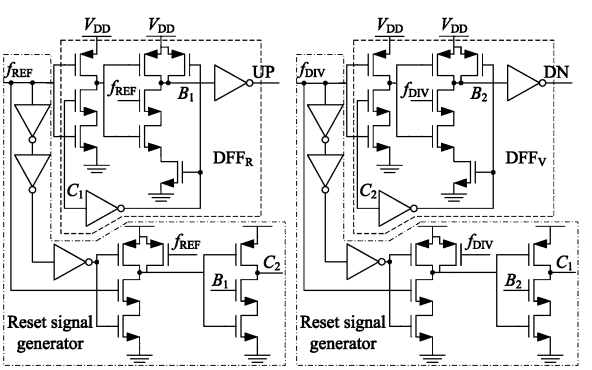

Fig. 9 Schematic of the proposed PFD

In this PFD, dynamic DFFs are used as the memory elements, three inverters and the two-input NAND gate are used to detect the rising-edge of the inputs, and generate a negative narrow pulse. Then this narrow pulse NAND with the signal B_1 or B_2 to generate the reset signal C_2 or C_1, respectively, then C_2 and C_1 crosswise reset the DFFs. For instance, if f_{REF} leads f_{DIV}, the rising-edge of f_{REF} will set DFF_R, that is UP = 1, and at the same time, the rising-edge of f_{REF} will be detected and delayed by the reset signal generator unit to reset the DFF_V; on the other hand, when UP =

1, DFF_V also will be reset, i. e. DN = 0, vice versa, when DN = 1, then UP = 0. Thus there is no four-state problem in this PFD. The right values of $\Delta_{RST,out}$, $\Delta_{RST,in}$, Δ_{in} are achieved by carefully optimizing the dimensions of the logic gates in the reset path and those inside the DFFs.

4 Simulation Results and Comparisons

All simulations are performed with ADS based on a TSMC 0. 18-μm CMOS process with a 1. 8-V supply voltage.

4. 1 Phase characteristic

When the periods of f_{REF} and f_{DIV} are set to be the same such as 0. 02 μs, and the phase error (i. e. τ in Figs. 10 and 11) between the two inputs sweeps from -3π to 3π, transient simulation outputs a linear saw-tooth phase-detecting curve which is independent of the duty-cycle of the inputs, shown in Fig. 10. Its linear phase-detecting range is almost [$\pm 2\pi$]. Moreover, it has an almost zero dead-zone (i. e. smaller than 1 ps), as shown in Fig. 11.

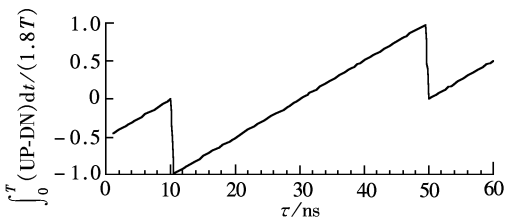

Fig. 10 Phase characteristic of the proposed PFD (f_{REF} = f_{DIV} = 50 MHz)

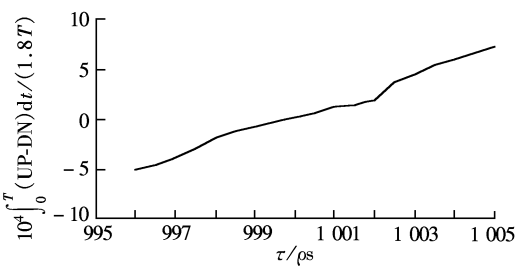

Fig. 11 Dead-zone of the proposed PFD (f_{REF} = f_{DIV} = 50 MHz)

4. 2 Frequency characteristic

When the initial phases of f_{REF} and f_{DIV} are set to be the same such as 10 ns, and the period of f_{REF} is 20 ns, then the period (i. e. P_V in Fig. 12) of f_{DIV} sweeps from 5 to 80 ns. Transient simulation outputs the frequency characteristic of the PFD, as shown in Fig. 12. Obviously, the proposed PFD also has a good frequency characteristic. As long as the frequency of f_{REF} is larger than that of f_{DIV}, the average value of (UP-DN) will be positive, and the control voltage V_C of VCO will be increased, and then the frequency of VCO will also increase. Meanwhile, the frequency difference between the inputs of the PFD will be smaller and smaller, and this frequency difference will be zero in the end. Obviously, the PLL is locked from then on.

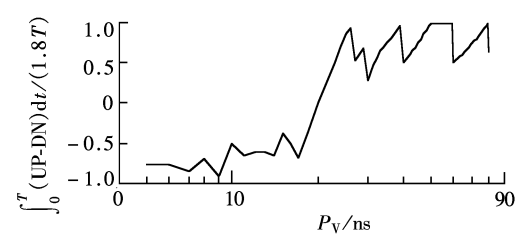

Fig. 12 Frequency characteristic of the proposed PFD

4. 3 Maximum operation frequency

In this design, the maximum operation frequency is up to 1 GHz, which is high enough for usual applications.

5 Conclusion

The proposed PFD adopts two reset functions to avoid the UP and DN signals to be logic-1 simultaneously. Thus, current mismatch of the charge pump will not worsen the performance of the PLL. Moreover, unlike the PFDs proposed in Refs. [6, 11], the performance of the proposed PFD is independent of the initial voltage of the nodes in the PFD, so the proposed PFD is also a robust PFD with high reliability. The power consumption of the proposed PFD is 53. 5 μA × 1. 8V@ 50 MHz. Thus, based on the theoretical analyses and simulation results, the proposed PFD shows satisfactory circuit performance with a high operation frequency ($\approx$ 1 GHz), a near zero dead-zone ($<$ 0. 1 ps), a wide phase-detection range ([$\pm 2\pi$]), high reliability, low phase jitter, low power consumption ($\approx$100 μW) and small circuit complexity.

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一种应用于高速低抖动电荷泵锁相环的高鲁棒性鉴频鉴相器

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摘要: 为改善现有鉴频鉴相器(PFD)中存在的问题,从理论分析的角度对现有的 PFD 进行了研究,并对其进行了基于电路结构的分类与比较. 提出并设计了一种应用于高速低抖动电荷泵锁相环的高鲁棒性新型鉴频鉴相器. 该 PFD 由 2 个上升沿触发的动态 D 触发器、2 个上升沿检测和延时模块及 2 个或门组成. 由于融合了 2 种复位机制,能避免 UP 与 DN 信号同时为高电平,因此,电荷泵的电流失配将不会恶化 PLL 的性能. 而且,该 PFD 的鉴相特性中几乎没有鉴相死区. 设计及仿真是基于 1.8 V 电源电压的 TSMC 0.18 μm CMOS 工艺. 由理论推导和电路仿真可知,该 PFD 具有高工作频率(≈ 1 GHz)、高可靠性、宽鉴相范围([±2π])、零死区(<0.1 ps)、低抖动、低功耗(≈100 μW)、低复杂度等特性.

关键词: 鉴频鉴相器;死区;盲区;鉴相特性;鉴频特性
中图分类号: TN763