Journal of Southeast University (English Edition) Vol. 24, No. 2, pp. 155 – 158 June 2008 ISSN 1003—7985

Integrated circuit for single channel neural signal regeneration

Li Wenyuan Wang Zhigong

(Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

Abstract: Based on the 4-channel neural signal regeneration system which is realized by using discrete devices and successfully used for *in-vivo* experiments on rats and rabbits, a single channel neural signal regeneration integrated circuit (IC) is designed and realized in CSMC's 0.6 μm CMOS (complementary metal-oxide-semiconductor transistor) technology. The IC consists of a neural signal detection circuit with an adjustable gain, a buffer, and a function electrical stimulation (FES) circuit. The neural signal regenerating IC occupies a die area of 1.42 mm × 1.34 mm. Under a dual supply voltage of ±2.5 V, the DC power consumption is less than 10 mW. The on-wafer measurement results are as follows: the output resistor is 118 mΩ, the 3 dB bandwidth is greater than 30 kHz, and the gain can be variable from 50 to 90 dB. The circuit is used for *in-vivo* experiments on the rat's sciatic nerve as well as on the spinal cord with the cuff type electrode array and the twin-needle electrode. The neural signal is successfully regenerated both on a rat's sciatic nerve bundle and on the spinal cord.

Key words: neural signal regeneration; function electrical stimulation; integrated circuit; electrode; CMOS technology

The neural signal regeneration system, which can be used to recover the function of a central neural system as well as other nerve bundles such as the sciatic nerve bundle, includes a neural signal detection microelectrode, a neural signal detection amplifier, a function electrical stimulation (FES) signal generating circuit, and a stimulating microelectrode[1].

In the system, a microelectrode is attached to the upper neural stump near the damage point of the injured nerve, detecting the bioelectrical signal on the neural stump. Because the bioelectrical signal detected by the microelectrode is weak, it must be connected to a neural signal detection amplifier so as to be amplified to a suitable amplitude. Then, the neural signal is sent to the FES signal generating circuit. Finally, the FES signal is sent to the stimulating microelectrode that connects with the lower neural stump near the damage point of the injured nerve, so that a bioelectrical signal similar to the one from a normal neural channel[2] is regenerated therein.

Based on the neural signal regeneration system, a four-channel neural signal regeneration system module is implemented by using discrete devices. Combined with a cuff-type microelectrode or a shaft-type microelectrode, it can successfully regenerate the neural signal in *in-vivo* experiments on rats and rabbits[3].

Because the neural function regeneration system should be implanted into the body, a single channel integrated circuit (IC) for neural signal regeneration is designed and realized in CSMC's 0.6 μm CMOS technology.

1 Circuit Descriptions

The neural signal regeneration system is shown in Fig. 1. The neural signal detecting microelectrode connects with the upper neural stump to obtain the neural signal and sends the signal to the signal detection circuit. The neural signal obtains amplification through the neural signal detection circuit, and it is then sent to the FES circuit through a buffer to stimulate the lower neural stump by the FES microelectrodes.

1.1 Neural signal detection circuit

The neural signal detection circuit consists of a capacitance, a resistance network and an instrument amplifier. The instrument amplifier is composed of three operational amplifiers. In accordance with the characteristics of the neural signals, high common-mode rejection ratio, low noise and low-power design are of the most importance for the detection circuit[4-5].

The detection circuit adopts the RC network structure instead of the conventional DC-coupled or AC-coupled structure (see Fig. 1). The RC network realizes the AC coupling for differential signals, and provides DC bias for the next amplifier at the same time. Theoretically, this structure leads to an unlimitedly large common mode rejection ratio (CMRR). In reality, however, the CMRR of the RC networks is limited since the grounding resistance and microelectrode impedance are unstable.

Three operational amplifiers are the most important parts in neural signal detection circuits. In Fig. 1, let $R_1 = R_2$, $R_3 = R_4$, and $R_5 = R_6$. The difference gain of the entire instrument amplifier is given by

$$A_v = \frac{v_o}{v_{in1} - v_{in2}} = -\frac{R_5}{R_3}\left(1 + 2\frac{R_1}{R_g}\right) \tag{1}$$

R_{A1} and R_{A2} represent the CMRR of operational amplifier A1 and A2, A_{v1} is the difference mode magnification of A1 and A2. The equivalent R_{A12} of the first stage circuit composed by A1 and A2 is given by

$$R_{A12} = \frac{A_{V1}}{A_{C1}} = \frac{1}{1/R_{A1} - 1/R_{A2}} = \frac{R_{A1}R_{A2}}{R_{A2} - R_{A1}} \tag{2}$$

According to Eq. (2), in order to improve the CMRR of the first stage, two operational amplifiers must have the same CMRR.

Received 2008-03-25.

Biography: Li Wenyuan (1964—), male, associate professor, lwy555@seu.edu.cn.

Foundation item: The National Natural Science Foundation of China (No. 90307013, 90707005).

Citation: Li Wenyuan, Wang Zhigong. Integrated circuit for single channel neural signal regeneration[J]. Journal of Southeast University (English Edition), 2008, 24(2): 155 – 158.

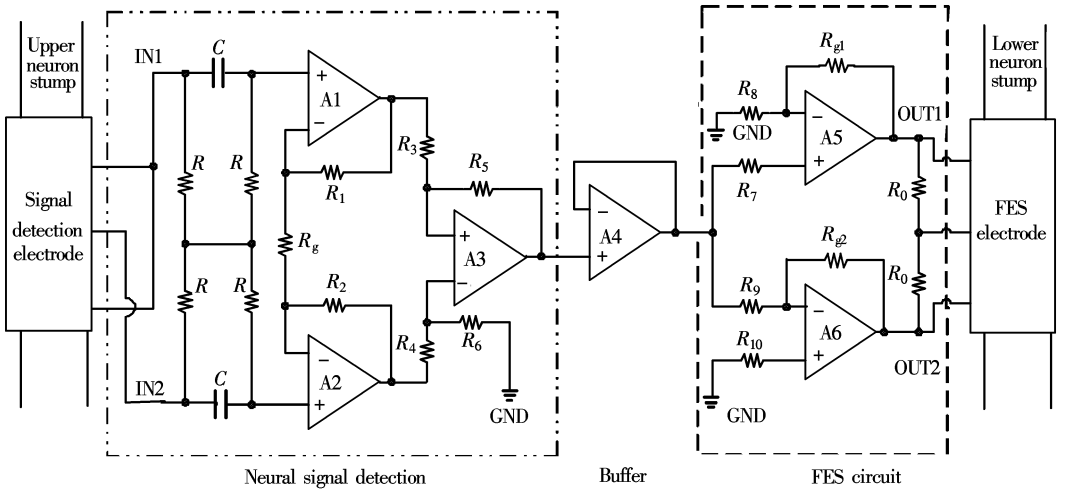


Fig. 1 Neural signal regeneration system

Then the equivalent CMRR of the whole detection circuit is

$$R_{\mathrm{A}} = \frac{A_{\mathrm{V1}} R_{\mathrm{A3}} R_{\mathrm{A12}}}{A_{\mathrm{V1}} R_{\mathrm{A3}} + R_{\mathrm{A12}}} \tag{3}$$

Therefore, to improve the CMRR of the whole detection circuit, the CMRR of a single operational amplifier must be improved. When R_{A1}, R_{A2}, and R_{A3} are fixed, enhancing the first-stage magnification can improve R_{A}. R_{A} is the CMRR of the entire detection circuit.

The operational amplifiers A1 to A3 have the same structure, shown in Fig. 2. It includes a two-stage structure. The Miller capacitor C and transistor M8 operating in the linear region are for frequency compensation. The open-loop gain of the operational amplifier is 78 dB, the unit gain bandwidth is 4.7 MHz, the phase margin is 78°, and the CMRR is 100 dB. The constant transconductance bias is used in the operational amplifier whose bias and power are irrelevant.

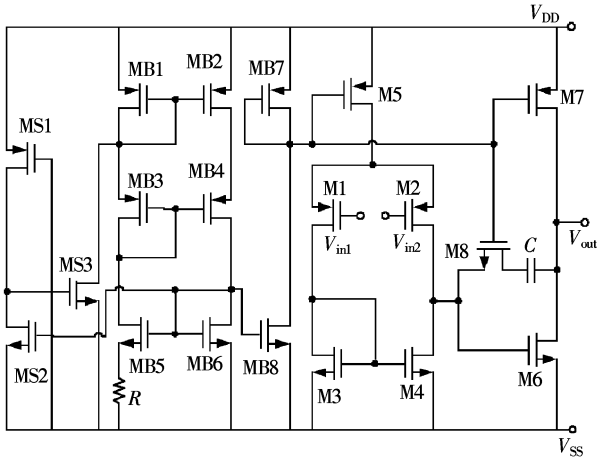


Fig. 2 Schematic of the operational amplifier

In order to reduce the operational amplifier noise, the input transistor is PMOS type because of its lower noise performance. Also, to obtain lower noise performance of the detection circuit, the sizes of the input and output transistors of the operational amplifier must be optimized.

The output transistors M8 and M9 should have a larger W/L in order to enhance the drive ability of the FES circuit.

1.2 Buffer circuit

The buffer circuit is a unit gain operational amplifier A4. The structure of the operational amplifier A4 is just the same as A1, A2 and A3, shown in Fig. 2. The buffer circuit has small output resistance, and transfers the neural signals to the next stage without loss. The simulation results show that the output resistance of the buffer is about 3.7 Ω.

1.3 FES circuit

The FES circuit amplifies the neural signals coming from the detection circuit. To regenerate the neural signals in the lower neural stump, the stimulating signals generated by the FES circuit must have a large voltage swing, and the output impedance of the FES circuit must be small[6-8].

The whole FES circuit consists of an in-phase amplifier and an inversion amplifier, so that the two output signals with 180° phase difference can stimulate the lower neural stump efficiently to regenerate the neural signals. The schematic of operational amplifiers A5 and A6 that constitute the FES circuit is shown in Fig. 3. The output voltage swing can reach an amplitude up to the power voltage.

In the circuit, the output transistors M8 and M9 are connected in the form of common source. This will not decrease the voltage margin, and the output signal will be rail-to-rail. Furthermore, to reduce the output impedance, feedback methods are used in the circuit.

The non-zero offset voltage in the error amplifier will change the quiescent current of the output transistor. The high quiescent current can decrease cross distortion and output signal swing and increase power loss. So, the relevant protection circuits are designed to control over-current of circuits through negative feedback.

The protection circuit consists of MD1 to MD9. It is used to control over-current of the FES circuit through negative feedback. MD9 has a small W/L. Normally, the current flow through MD9 is small, and the voltage between source and drain of MD9 is relatively small, so MD7 and MD8 do not act. When the current of the output circuit becomes large, the current flowing through MD9 increases correspondingly. When the voltage between source and drain of MD9 exceeds the total conduction voltage of MD7 and MD8, the whole

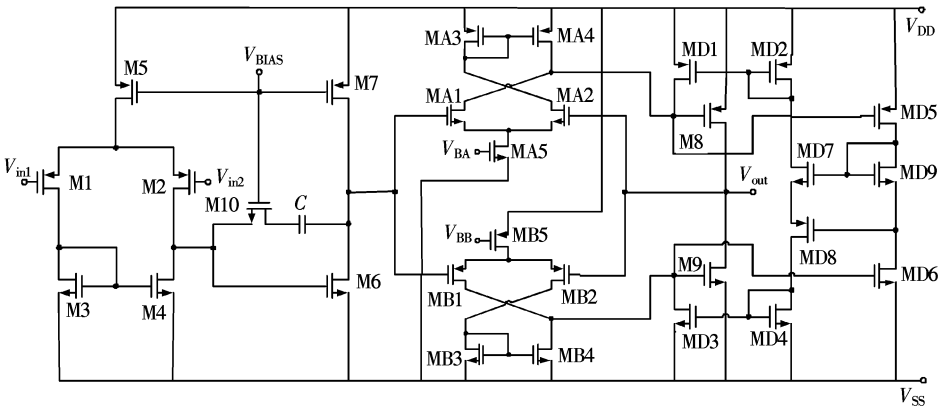


Fig. 3 Schematic of the operational amplifier A5/A6

over-current control circuit begins to run. Because MD9 has a small W/L compared to that of MD7 and MD8, a little change in the voltage between source and drain of MD9 (> $V_{TMD7} + |V_{TMD8}|$) will lead to great change of current in MD7 and MD8. And through MD1, MD2, MD3 and MD4, the current feeds back to the gate of M8 and M9, and the gate-source voltage of M8 and M9 is reduced, so that the over-current is also reduced.

The largest quiescent current I_Q (suppose $V_{TMD7} = V_{TMD9}$) of the output transistor is given by Eq. (4), in which β_{MD9} is the transconductance parameter of MD9.

$$I_Q = \frac{\beta_{MD9}}{2}(V_{TMD7} + |V_{TMD8}| - V_{TMD9})^2 \frac{(W/L)_{M9(M8)}}{(W/L)_{MD6(MD5)}} = \frac{\beta_{MD9}}{2} V_{TMD8}^2 \frac{(W/L)_{M9(M8)}}{(W/L)_{MD6(MD5)}} \quad (4)$$

2 Test Results

The chip is fabricated using the CSMC's 0.6 μm CMOS technology by means of multi-project wafer (MPW) project. Fig. 4 shows the photograph of the realized chip. The die size of the chip is 1.42 mm × 1.34 mm. It is tested on-wafer in our probe station. The static power consumption of the chip is less than 10 mW, the output resistor is 118 mΩ, 3 dB bandwidth is greater than 30 kHz, and the gain can be adjustable from 50 to 90 dB. The output signal measured on-wafer is shown in Fig. 5, where the V_{pp} of the input 1 Hz sine signal is 2 mV.

After the package, the chip is also measured. The output signal is shown in Fig. 6 where both the input 100 Hz and the 10 kHz sine signal have an amplitude of 2 mV.

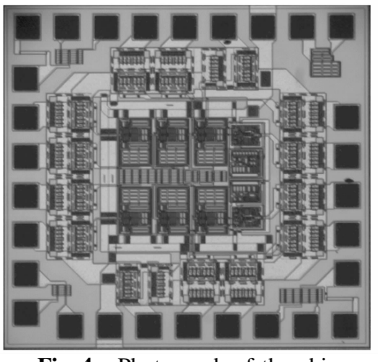


Fig. 4 Photograph of the chip

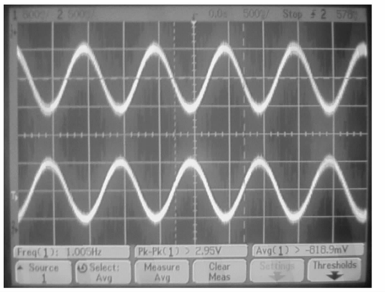
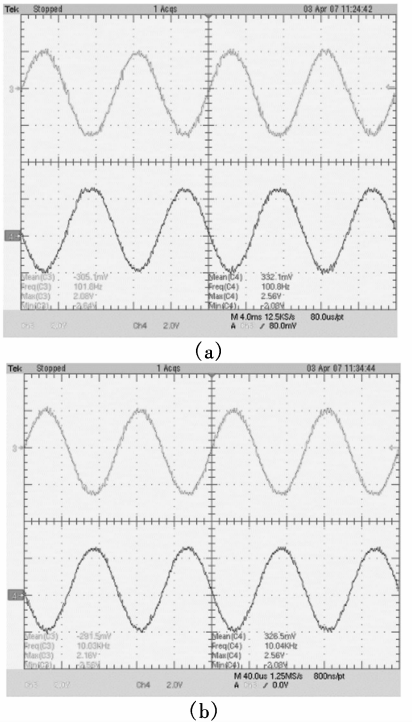


Fig. 5 Output signal measured on-wafer



(a)

(b)

Fig. 6 Output signal measured after the circuit is packaged, the input signal V_{pp} is 2 mV. (a) Input 100 Hz sine signal; (b) Input 10 kHz sine signal

3 Animal Experiment

Two *in-vivo* neural signal regeneration experiments are carried out at the Institute of RF- & OE-ICs of Southeast University. The experimental objects are rats. Their weights are about 350 g. The surgery procedure in a rat is as follows: anaesthesia; rat body fixation; exposure left crus sciatic nerve; right crus sciatic nerve; spinal cord around T12;

electrode location; fixation; and leads connection.

The FES signal has a frequency of 1 Hz, generated by an arbitrary wave generator in Agilent 33220A. The bioelectrical signals are monitored and recorded by an oscillograph of Agilent 54624A.

An experiment is conducted by using two twin-needle electrodes and a cuff microelectrode connected with the IC chip. One twin-needle electrode inserted into the spinal cord located at the rat' s left crus motor nerve area is used for applying FES signal. Another twin-needle electrode inserted into the lower end of the rat' s right crus sciatic nerve is used as a stimulating electrode. The cuff microelectrode enwraps the rat' s left crus sciatic nerve, which is used as a neural signal detection electrode. When the FES signal is applied and the IC is turned on, the rat moves its left crus as well as its right crus. Turn off the IC, and the rat only moves its left crus. Cut off the rat' s right crus sciatic nerve at the upper end, and turn on the IC. When the FES signal is applied, the rat moves its left crus and right crus again. Turn off the IC and the rat only moves its left crus.

The cuff electrode has 12 dots; several dots are used to monitor the neural signals by the oscillograph of Agilent 54624A. So, during the experiment, the neural signals can be observed. Fig. 7 is one photo of the experiment.

Fig. 7 Photo of the *in-vivo* neural signal regeneration experiment on rats

4 Conclusion

A single channel neural signal regeneration circuit has been realized in the CSMC's 0.6 μm CMOS technology. Connected with microelectrodes, it can be used to regenerate rats' neural signals of the sciatic nerve or the spinal cord in *in-vivo* experiments.

References

[1] Wang Zhigong, Lü Xiaoying, Gu Xiaosong, et al. Microelectronic detecting, processing and rebuilding of central neural signals[C]//*The Third Joint Symposium on Opto- and MicroElectronic Devices and Circuits*. Wuhan, China, 2004: 22 - 26.

[2] Wang Zhigong, Lü Xiaoying, Li Wenyuan, et al. Study of microelectronics for detecting and stimulating of central neural signals[C]//*IEEE Proceedings of International Conference on Neural Interface and Control*. Wuhan, China, 2005: 192 - 200.

[3] Li Wenyuan, Wang Zhigong, Lü Xiaoying, et al. Multi-channel neural signal stimulating module and in-vivo experiments [J]. *Journal of Southeast University*: *English Edition*, 2007, **23**(1): 26 - 30.

[4] Wang Yufeng, Wang Zhigong, Lü Xiaoying, et al. A multichannel neural signal detecting module: its design and test in animal experiments [J]. *Progress in Natural Science*, 2007, **17**(6): 675 - 680.

[5] Wang Yufeng, Wang Zhigong, Lü Xiaoying, et al. Fully integrated and low power CMOS amplifier for neural signal recording[C]//*Proceedings of the* 2005 *IEEE Engineering in Medicine and Biology*. Shanghai, China, 2005: 306.

[6] Li Wenyuan, Wang Zhigong, Zhang Zhenyu. Low-power CMOS IC for function electrical stimulation of nerves[J]. *Chinese Journal of Semiconductors*, 2007, **28**(3): 393 - 397.

[7] Li Wenyuan, Zhang Zhenyu, Wang Zhigong. Function electrical stimulation signals generator circuits for the central nerve and the sciatic nerve[C]//*Proceedings of the* 2005 *IEEE Engineering in Medicine and Biology* 27*th Annual Conference*. Shanghai, China, 2005: 282.

[8] Zhang Zhenyu, Li Wenyuan, Wang Zhigong. Circuit design for function electrical stimulation of central nerve system [J]. *Journal of Electrical and Electronic Education*, 2005, l**27**(5): 45 - 48. (in Chinese)

单通道神经信号再生集成电路

李文渊 王志功

(东南大学射频与光电集成电路研究所,南京 210096)

摘要:将利用分立器件设计的4通道神经信号再生电子系统成功地应用于大鼠和家兔的活体动物实验,再生了它们的神经信号.采用相同的原理,用CSMC 0.6 μm CMOS工艺设计实现了单通道神经信号再生集成电路.电路由增益可调的神经信号探测电路、缓冲器和神经功能电激励电路构成.电路采用±2.5 V双电源电压供电.芯片尺寸为1.42 mm×1.34 mm.在片测试电路的静态功耗小于10 mW,输出电阻为118 mΩ,3 dB带宽大于30 kHz,增益在50~90 dB可调.电路芯片与卡肤电极、针状双体电极一起,用于大鼠的神经信号再生的活体动物实验,成功地再生了大鼠的坐骨神经和脊髓神经信号.

关键词:神经信号再生;功能电激励;集成电路;电极;CMOS工艺

中图分类号:TN722;Q424