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0.18 μm CMOS programmable frequency divider design for DVB-T

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Abstract: The implementation of a programmable frequency divider, which is one of the components of the phase-locked loop (PLL) frequency synthesizer for digital video broadcasting-terrestrial (DVB-T) and other modern communication systems, is presented. By cooperating with a dual-modulus prescaler, this divider can realize an integer frequency division from 926 to 1 387. Besides the traditional standard cell design flow, such as logic synthesis, placement and routing, the interactions between front-end and back-end are also considered to optimize the design flow under deep submicron technology. By back-annotating the back-end information to front-end design, a custom wire-load model is created which is more practical compared with the default model. This divider has been fabricated in TSMC 0.18 μm CMOS technology using Artisan standard cell library. The chip area is 675 μm × 475 μm and the power consumption is about 2 mW under a 1.8 V power supply. Measurement results show that it works correctly and can realize a frequency division with high precision.

Key words: programmable frequency divider; frequency synthesizer; standard cell; DVB-T

In modern communication systems, the phase-locked loop (PLL) frequency synthesizer is one of the basic components. Its operating frequency depends both on the frequency divider and the voltage controlled oscillator(VCO)[1-4]. The function of channel selection in the frequency synthesizer demands programmable division ratios for the frequency divider. Normally, the integer-*N* frequency synthesizer is more practical, less costly and of low spurious sideband performance as compared with the fractional-*N* frequency synthesizer[5-6].

Many researches have focused on programmable frequency dividers with high operation frequency and multi-system application. For example, a high-speed wideband high resolution programmable frequency divider was investigated in Ref. [7], in which an ultra-wide range high resolution frequency divider was achieved with low power consumption for 5-6-GHz wireless LAN applications.

In this paper, a programmable frequency divider is designed and implemented for the application of digital TV. Digital TV programs can be transmitted by cable, satellite, terrestrial, and wireless cable. There are three main terrestrial standards: ATSC, ISDBT-T and DVB-T(digital video broadcasting terrestrial). Unlike many other existing frequency dividers, the proposed one which can be used in the DVB-T receiver is designed based on the standard cell method and then integrated with other modules designed using the full custom method to construct an integer-*N* frequency divider. Measurement results indicate that the chip works well in the frequency synthesizer. With that, the frequency synthesizer can perform multi-modulus division.

1 Architecture of Frequency Synthesizer

In the PLL frequency synthesizer, the digital frequency divider is usually realized by cascading divide-by-2 circuits for high-speed applications[8]. However, this structure can only obtain the division ratios equal to 2^n, where n is the number of divide-by-2 stages. In our design, a dual-modulus divide-by-16/17 prescaler (DMP) and a programmable frequency divider are integrated to obtain different division ratios for PLL frequency synthesizers. An integer-*N* frequency synthesizer structure is adopted in our design since the integer-*N* frequency synthesizer is more practical, less costly, and low spurious sideband effects compared to fractional-*N* frequency synthesizer. In this way, the dividers can obtain any division ratios based on the outside control signal.

Fig. 1 shows the frequency synthesizer consisting of a frequency divider (DIV), a phase-frequency detector (PD), charge-pump and loop-filter (CP/LF), VCO, DMP and a programmable frequency divider. The DMP and frequency divider cooperate to realize integer-*N* divide. DMP is a divided-by-16/17 dual-modulus prescaler. In Fig. 1, f_{OSC} is generated by a crystal oscillator of 16.5 MHz and f_{REF} is a reference signal to detect the frequency and phase generated by the DIV with divide-by-11 of f_{OSC}. f_{VCO}, the output of VCO, is one of the input signals of the DMP with the frequency between 1 389 and 2 080.5 MHz. Another input signal of the DMP is ModCtr which is obtained from the frequency divider divided by 926 to 1 387. The frequency divider has two inputs: one is ClkFront coming from the DMP; the other is the control signal CtrlLogic. Under the control of CtrLogic and in cooperation with the DMP, the divider can realize the required frequency division ratios and outputs LowOut to PD for detecting frequency and phase.

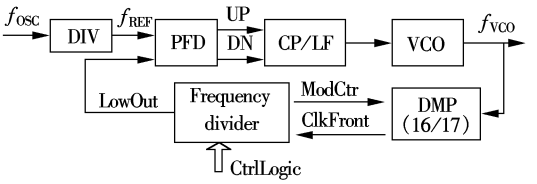

Fig. 1 Block diagram of PLL frequency synthesizer

2 Design of Programmable Frequency Divider

In this section, the structure of the frequency divider is described first, and then the modified standard-cell design flow is employed to obtain a specific custom wire-load model especially for deep submicron(DSM) technology.

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2.1 Basic structure

Fig. 2 shows the basic structure of the frequency divider. It consists of two counters: one is the main counter and the other is the swallow counter. The swallow counter is used to control the DMP which is set to either N or $N+1$. The former is modulus M while the latter is modulus A ($M > A$), where M and A are two control signals that can be configured in practical applications. For any given M and A, both counters count up continuously until their values equal A and M, respectively. Based on DVB-T standards, in our design, N equals 16, M is an integer between 57 and 86, and A varies from 0 to 15. So, M and A can be represented as 7-bit and 4-bit signals, respectively. At the initial reset state, the prescaler is set to a divide ratio of 17, but the swallow counter will change this divide ratio to 16 when it finishes counting A number of cycles. While the swallow counter is less than A, its output ModCtr is high; otherwise it remains low. When the swallow counter counts up to A, ModCtr is set 0, but two counters continue to up-count. When the main counter counts up to M, LowOut completes one period and both counters are cleared, as shown in Fig. 3.

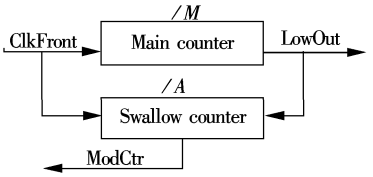

Fig. 2 Basic structure of frequency divider

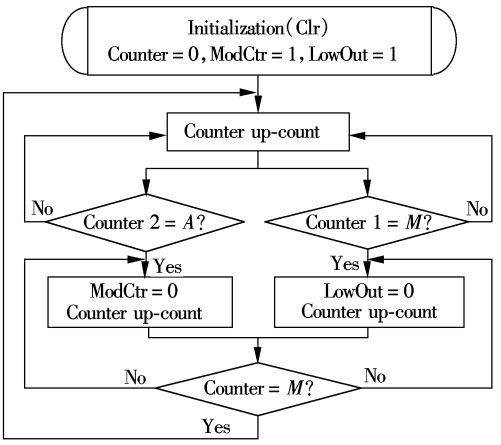

Fig. 3 Principle of frequency division

By combining with DMP, divide-by-P can be realized based on the following formula:

$$P = A \times 17 + (M - A) \times 16 = M \times 16 + A$$

Based on different M and A, the frequency divider can be divided by any integer from 926 to 1 387. As a result, the VCO can work at multiple central frequencies distributing from 1 389 to 2 080. 5 MHz with an interval of 1. 5 MHz, shown in Tab. 1.

2.2 Design and implementation

The frequency divider is designed and implemented based on the ARM TSMC 0. 18 μm standard cell library. Unlike full custom design , standard cell design depends mainly on

Tab. 1 Examples of modulus P and f_{VCO} (f_{REF} = 1. 5 MHz)

M	A	Division index P	f_{VCO}/MHz
57	14	926	1 389
57	15	927	1 390. 5
59	2	946	1 419
59	3	947	1 420. 5
60	8	968	1 452
60	12	972	1 458
81	1	1 297	1 945. 5
81	8	1 304	1 956
84	9	1 353	2 029. 5
84	10	1 354	2 031
86	11	1 387	2 080. 5

EDA tools and the standard cell library. First, the function is realized in Verilog HDL. Then a synthesis tool is used to generate corresponding netlist. At this stage, the wire-load model is required to predict signal delay. It is well known that in submicron technology, especially in DSM, the more accurate the wire-load model is, the more optimal the design is. In most cases, the default wire-load models provided by synthesis tools are linear respect to the fanouts of the circuit. That is to say, the default relationships among the path delay, wire-load and wire length with the fanouts are linear. However, that is not practical. Therefore, it is better to generate a more accurate wire-load model to improve the synthesis results for a specific design[9]. Fig. 4 shows the design flow in the DSM, in which two synthesis stages are included. One is the initialed synthesis and the other is a detailed synthesis. In order to create a custom wire-load model before detailed synthesis, initial synthesis and initial placement and route(P&R) are needed when compared to the traditional design flow(shown as the right part in Fig. 4). The "initial" means that there is no need to pay much attention to timing because initial synthesis and initial P&R are just for creating a practical wire-load model.

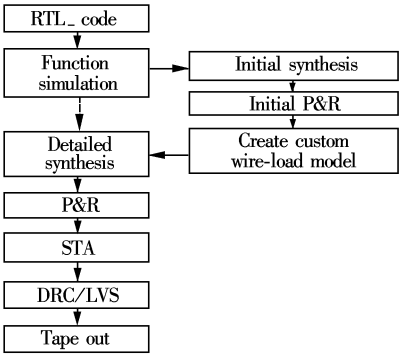

Fig. 4 Design flow in DSM

After finishing initial P& R, RC parameters and wire-load delay are obtained and then back-annotated to synthesis tools. Using the command create_wire_load, custom wire-load models are generated in Fig. 5. From the figure we can see that the wire-length, resistance, capacitance and area do not vary linearly with the fanouts.

Once the custom wire-load models are obtained, the design can go on to the detailed synthesis. Tab. 2 shows the main synthesis constraints set for the synthesis tool. In this design, the clock period should not be more than 8 ns. Considering the margin for the back-end design, the clock period

is constrained to 4 ns for practical purposes. For the clock network, both clock latency and uncertainty are set as 0. 5 ns. ClkFront, a clock signal with low frequency, and clear signal Clr are set as do not touch. Of course, the maximal area is constrained to zero to minimize the chip area. Using the above constraints and the custom wire-load model, better results can be achieved after a detailed synthesis when compared to the default wire-load model.

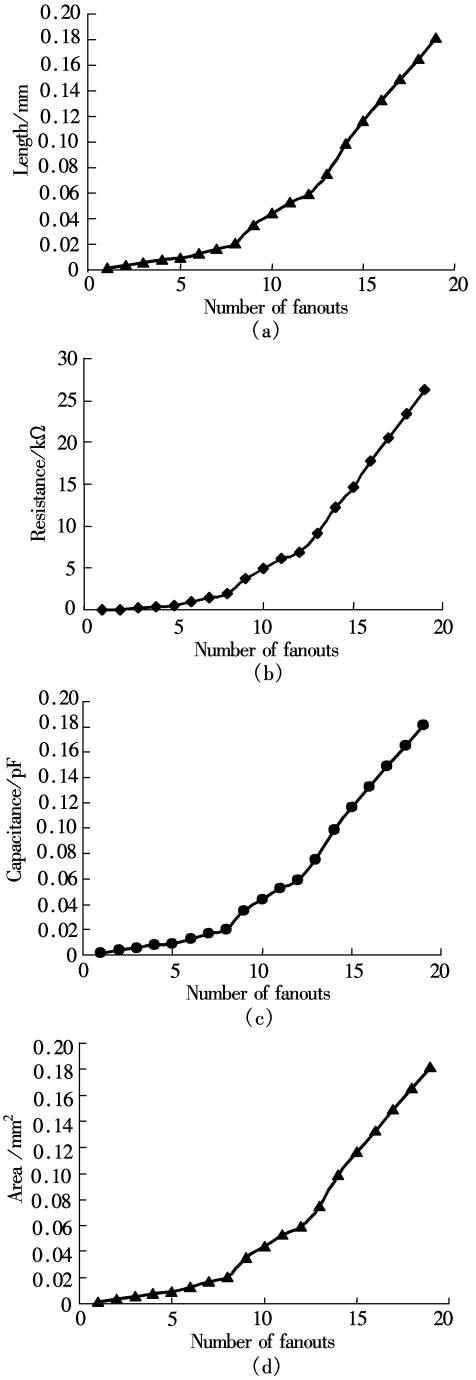

Fig. 5 Generated custom wire-load model. (a) Wire-length vs. fanout; (b) Resistance vs. fanout; (c) Capacitance vs. fanout; (d) Area vs. fanout.

Tab. 2 Synthesis constraints

Properties in DC	Value
Clock period/ns	4
Clock latency/ns	0. 5
Clock uncertainty/ns	0. 5
Do not touch network	ClkFront, Clr
Net drive	ClkFront, Clr
Maximum area	0

The next steps are floorplanning and P& R, which belong to the back-end design and can be completed in Apollo Ⅱ. Normally, there are many steps in back-end design. The chip area, power and ground (P/G) pad numbers, and core aspect ratios are considered according to the synthesis results and I/O numbers and their placements. The chip area should include the core area and P/G network area. Typically, the core aspect ratio is set as 1∶1.

The P/G pad numbers can be evaluated based on the electro-migration and IR drop as follows. Power consumption reports of detailed synthesis show that the core power consumption P_{core} is 0. 76 mW. Thus, the core power consumption should be up to 1. 4 mW if a 50% margin is set. In TSMC 0. 18 μm CMOS technology, the core supply voltage V_{core} is 1. 8 V and the maximum current that an I/O pad can tolerate is 26 mA. So, the core current is calculated as $i_{core} = P_{core}/V_{core} = 0.64$ mA, thus one pair of P/G pads is enough for this design. To determine the width of the power strap, the electro-migration and IR drop should be considered. From the technology data we know that the square resistance of metal 1 $R_{m1} = 0.101\ \Omega$ per square and the current density $J_{strap} = 1$ mA/μm. Based on electro-migration, the minimal width of the power strap should be $W_{strap} = I_{strap}/J_{strap} = 1$ μm wide. Then the power strap length L_{strap} should be checked to see if the IR drop is less than 5% of VDD_{core}. Since L_{strap} is about 150 μm, the IR drop $V_{drop\_strap} = I_{strap} \times R_{strap} = R_{m1} \times J_{metal} \times L_{strap} = 0.016\ V < 0.090\ V$ (= 5% of VDD_{core}). Therefore, the floorplan of the design meets the requirements of both electro-migration and IR drop. Otherwise, the minimal width of a power strap should be recalculated according to the IR drop.

After P& R, a static timing analysis (STA) can be performed. The back-end design results, such as set_load, standard delay format (SDF) and PDEF files can be back-annotated to the timing analyzer to analyze the static timing. The analysis results show that both the hold time and the setup time satisfy the design requirements.

The last step of the design flow is verification. It can be done in Cadence Virtuoso through DRC(design rule check) and LVS (layout-vs-schematic) tools. Additionally, RC parameters are extracted for transient analysis in HSPICE. The results of the transient analysis are shown in Fig. 6. In order to obtain a complete period waveform, the period of both Clr and ClkFront are configured as 320 ns and 8 ns, respectively. The waveform shows that the division precision is identical to the simulation result.

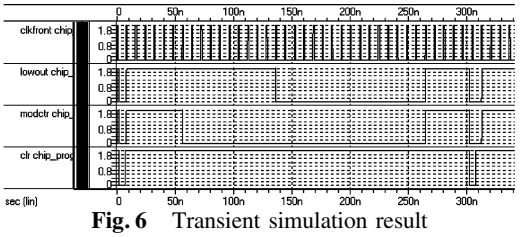

Fig. 6 Transient simulation result

3 Measurement Results

The frequency divider is fabricated using TSMC 0. 18 μm CMOS technology and ARM standard cells. Fig. 7 is its lay-

out with a 675 μm × 475 μm area.

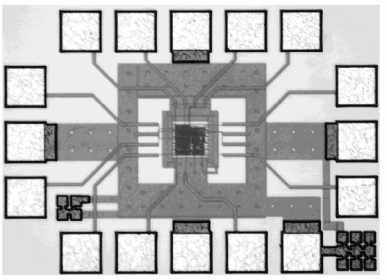

Fig. 7 Die photo of the frequency divider

Fig. 8 shows the measurement results of ModCtr and Tab. 3 gives some of the measurement results of their duty cycle where $A = 15$, $M = 64$ to 112 and ClkFront = 120 MHz. We can see that the duty cycle of LowOut is 53.7% and ModCtr is 23.1% when $M = 64$, both are very close to the simulated results of 50% and 23.4%. In addition, the measured current is about 1.1 mA, thus the power consumption is about 1.8 × 1.1 = 1.98 mW. From the measurement results, we can arrive at the conclusion that the chip meets the design demands and its function is realized correctly.

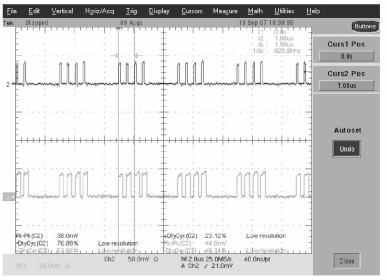

Fig. 8 Measured ModCtr and LowOut($M = 64$, $A = 15$)

Tab. 3 Measurement results of duty cycle ($A = 15$) %

M	LowOut		ModCtr	
	Simulation	Measurement	Simulation	Measurement
64	50	53.7	23.4	23.1
80	50	55.9	18.5	18.8
96	50	54.0	15.6	14.1
112	50	53.5	13.4	12.1

4 Conclusion

A programmable frequency divider is implemented in TSMC 0.18 μm CMOS technology based on standard cell. By back-annotating the useful messages of back-end design to synthesis tools and creating a custom wire-load model, a more precise design flow for DSM technology is obtained. Measurement results indicate that the frequency divider achieves the expected precision. Finally, the PLL frequency synthesis with multiple central frequencies for DVB-T is realized and works well when the frequency divider is mixed with the other modules designed with the full custom method.

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应用于 DVB-T 的 0.18 μm CMOS 可编程分频器设计

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摘要: 可编程分频器是 PLL 频率综合器中的重要单元,用标准单元方法实现了一种适用于数字电视地面广播(DVB-T)接收机的 PLL 频率综合器的可编程分频器. 结合双模分频器,所设计的分频器可实现 926 ~ 1 387 之间的整数分频. 除了传统的逻辑综合、版图规划、布局布线等标准单元设计流程,所设计流程中还考虑了前端设计和后端设计之间的信息交互. 通过将后端信息返标到前端设计工具,生成了用户定义的线负载模型,该模型比缺省的模型更接近实际情况. 该可编程分频器采用 ARTISAN TSMC 0.18 μm CMOS 标准单元库设计并流片,芯片面积为 675 μm × 475 μm,1.8 V 电压下的功耗为 2 mW. 测试结果表明芯片工作正确,能够完成精确的分频比.

关键词: 可编程分频器;频率综合器;标准单元;数字电视地面广播

中图分类号: TN453