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Rail-to-rail op-amp with constant transconductance, SR and gain

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Abstract: A novel general-purpose low-voltage rail-to-rail CMOS (complementary metal-oxide-semiconductor transistor) operational amplifier (op-amp) is introduced, which obtains constant transconductance, slew rate and constant high gain over the entire input common mode voltage range. The proposed scheme has the potential for applications in deep submicrometer technology, as the operation of the circuit does not exclusively rely on the square-law or the linear-law of transistors. The scheme is compact and suitable for applications as VLSI cell. The rail-to-rail op-amp has been implemented in DPDM 0.6 μm mixed-signal process. The simulations show that in the entire range of input common mode voltage, the variations in transconductance, SR and gain are 1%, 2.3%, 1.36 dB, respectively. Based on this, the layout and tape-out are carried out. The area of layout is 0.072 mm^2. The test results are basically consistent with the circuit simulation.

Key words: CMOS analog circuit; op-amp; rail-to-rail; constant transconductance; constant slew rate; constant gain

The trend in IC technology is towards low voltage and low power these years. But an obstacle prevents it from further development—the demand for an acceptable signal-to-noise ratio, especially for the use in portable electronic equipment. For an operational amplifier (op-amp), it is not difficult to obtain a nearly rail-to-rail output range using a simple class A or a class AB output stage; the problem lies in the input stage. One of the best ways to maximize the input range is to utilize a complementary input stage with a p-channel and an n-channel differential pairs in parallel, whose currents flow into a cascode stage called a summation circuit, as shown in Fig. 1. However, both the ac and the dc signals delivered by the input pairs vary as functions of the input common mode voltage V_{cm}, resulting in an inconstant transconductance g_m and slew rate (SR). g_m variation results in problems in optimizing the phase margin (PM), the unit gain bandwidth (UGBW) and differential gain; SR variations will cause problems for system-level designers, who often assume that the response time of an op-amp to a large signal is changeless.

For a general-purpose op-amp, several requirements should be met[1-3]. First, the g_m should be maintained constant over the entire range of V_{cm}. The operation for the constant g_m should not exclusively rely on the square-law or the linear-law between the current and the g_m; otherwise, the scheme cannot be applied to both long-channel and short-channel transistors. Secondly, the SR should be constant in spite of the variations in V_{cm}. This is necessary in order to simplify the design of a mixed signal circuit where a behavioral language is often used to create models of analog cells. The requirement on the SR indicates that the total current of the complementary input differential pairs should be kept constant. Thirdly, to ensure a constant gain, not only the g_m, but also the output impedance should not be influenced by V_{cm}. Fourthly, to be applicable as a VLSI cell, it should be compact to save space. Finally, feedforward control is better than feedback control regarding response time.

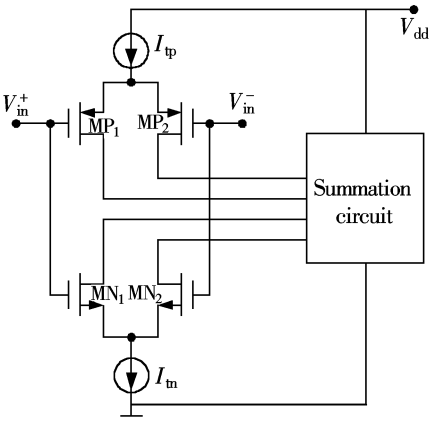

Fig. 1 Basic op-amp with complementary input stage

Many schemes[1-7] have been proposed to stabilize the g_m and/or the SR of a rail-to-rail op-amp. However, none of them has achieved simultaneously a constant g_m, SR and gain. In Ref. [3], only a constant voltage gain is obtained, without any consideration to the g_m and the SR. In Refs. [4 – 5], two types of compact op-amps are shown, which only operate normally with square-law. In Ref. [6], although the scheme can be realized both with long-channel and short-channel transistors, the performance of the SR and the gain is not addressed. In Ref. [7], a scheme using a technique named dynamic current scaling is shown, but its gain varies as a function of V_{cm}. In Ref. [8], the g_m of the op-amp is controlled by a feedback signal. Although the scheme improves the response time of the feedback loop, it is relatively complex. In Refs. [1 – 2], although both a constant g_m and SR are kept regardless of the channel lengths of transistors, the variations in the g_m as a function of V_{cm} is up to 20% in Ref. [1], and the level shifter in Ref. [2] introduces a heavy power supply noise transferred from the digital part in a mixed-signal system.

This paper proposes a novel compact rail-to-rail input stage. Based on this scheme, an op-amp which achieves simultaneously constant g_m, SR, and gain is reported.

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1 Operation Principle and Scheme

1.1 Basic complementary input stage

The basic structure of the complementary input stage is shown in Fig. 1, where double differential pairs, MP_1/MP_2 and MN_1/MN_2, are utilized. Four output currents of double differential pairs are delivered to a summation circuit.

According to the operation of input differential pairs, three regions of V_{cm} can be defined. Note that V_{tn} and V_{tp} are the absolute values of threshold voltage of the n-channel transistor and the p-channel transistor, respectively.

1) Low-voltage region ($V_{cm} < V_{tn}$): Only the p-channel pair (MP_1/MP_2) is active, whose tail current transistor is in a saturation region with a contribution of g_{mp0} and I_{tpsat} to the ac and dc signals, respectively.

2) Mid-voltage region($V_{tn} < V_{cm} < V_{dd} - V_{tp}$): Both of the double differential pairs are active, and with an increase in V_{cm}, the tail current transistor of the n-channel pair (MN_1/MN_2) enters into a linear region and a saturation region successively, while the working region of the p-channel tail current transistor changes in reverse order. The ac and dc signals are the sum of the contributions from both of the double pairs.

3) High-voltage region ($V_{cm} > V_{dd} - V_{tp}$): Only the n-channel pair is active, whose tail current transistor is in a saturation region with a contribution of g_{mn0} and I_{tnsat} to the ac and dc signals, respectively. By proper arrangement of the aspect ratios of input differential pairs, the following equations can be satisfied:

$$I_{tnsat} = I_{tpsat} = I_{t0} \tag{1}$$

$$g_{mn0} = g_{mp0} = g_{m0} \tag{2}$$

1.2 The proposed op-amp

The operation principle of the proposed circuit is to regulate the ac and dc signals which enter into the summation circuit in the mid-voltage region by swaying redundant parts of currents of input pairs.

The proposed op-amp is shown in Fig. 2, which consists of three parts: a V_{cm} sensor including sensing pair MCP_1/MCP_2, an input stage including double input pairs MN_1/MN_2 and MP_1/MP_2 and a regulating pair MDN_1/MDN_2, and an output stage including the summation circuit. MN and MDN have the same aspect ratios and nominal bias currents. By proper arrangement, equation $\beta_{mn} = \beta_{mdn} = \beta_{mp} = \beta_m$ can be satisfied. The tail current of MDN is controlled by MCP through current mirrors M_{in} and MDN.

The operation principle of the proposed input stage can be demonstrated in Fig. 3 and explained by the following equations:

1) In the low-voltage region

$$g_{mt} = g_{mp0} = g_{m0} \tag{3}$$

$$I_t = I_{o1} + I_{o2} = I_{p1} + I_{p2} = 2\frac{I_{tp0}}{2} = I_{t0} \tag{4}$$

2) In the mid-voltage region

$$g_{mt} = g_{mn} + g_{mp} - g_{mdn} = g_{m0} \tag{5}$$

$$I_{tnsat} = I_{tnsat} = I_{t0} \tag{6}$$

3) In the high-voltage region

$$g_{mt} = g_{mp0} = g_{m0} \tag{7}$$

$$I_t = I_{o1} + I_{o2} = I_{n1} + I_{n2} = 2\frac{I_{tn0}}{2} = I_{t0} \tag{8}$$

Among the above Eqs. (3) to (8), Eqs. (5) and (6) are the key parts for the realization of the input stage. For the proposed input stage, the bias current of the n-channel regulating pair MDN is supplied by p-channel pairs MCP. So in the mid-voltage region, when both the gate voltages of MN and MP satisfy the requirement to turn on, MDN also begins to operate. And because they have the same aspect ratio and normal bias current with MN, the ac contribution of MDN is consequently identical to the redundant part of that made by MN and MP, as shown in Fig. 3(a). But with adverse polarities of the input signals, MDN functions to counteract the re-

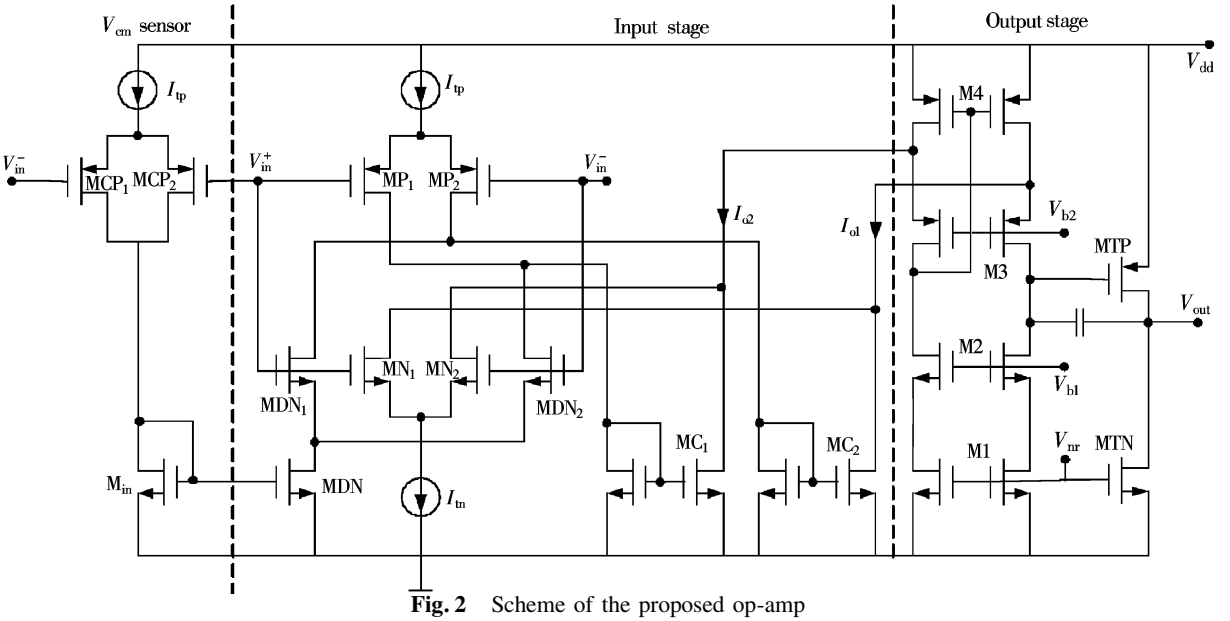

Fig. 2 Scheme of the proposed op-amp

dundant g_m. As to the dc signal, MDN sways the redundant dc part of MP, for the current direction of MDN opposes that of MP. Now, under the functions of MDN, g_{mt} and I_t in the mid-voltage region are identical in the high-voltage and the low-voltage region.

The operation above does not exclusively depend on the square law or the linear law between the current and the g_m, indicating that the proposed input stage has the potential to work both in a strong inversion region and a weak inversion region.

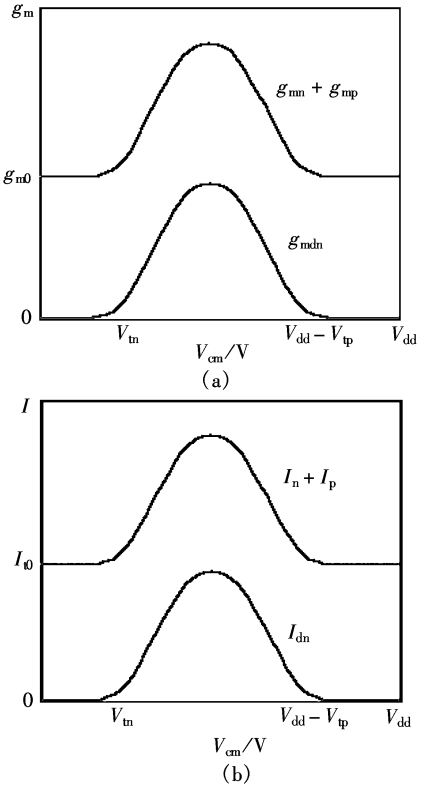

Fig. 3 Illumination of the signals of the proposed input stage. (a) g_m vs. V_{cm}; (b) I vs. V_{cm}

In spite of the stabilization of transconductance, the differential gain cannot be constant without the help of current mirrors MC_1 and MC_2. They add the currents of MN to that of MP prior to the summation circuit. In this way, the static operation point and output impedance of the summation circuit can be kept changeless, because the total current of MN and MP will not have been influenced by V_{cm} as mentioned before.

2 Simulation Results and Discussion

The proposed rail-to-rail op-amp has been designed in a 0.6 μm CMOS technology supported by CSMC, where $V_{tn} = 0.79$ and $V_{tp} = -0.96$. The input pairs work in a strong inversion region with a tail current of 60 μA. Aspect ratios of the transistors are summarized in Tab. 1.

Figs. 4, 5, and 6 show the total transconductance g_{mt} ($= g_{mn} + g_{mp} - g_{mdn}$), the total slewing current I_t ($= I_n + I_p - I_{dn}$) and the dc gain of the op-amp vs. V_{cm}, respectively. The variations in the g_{mt}, I_t, and dc gain in the entire range of V_{cm} are only 1%, 2.3%, and 1.36 dB, respectively. Since there is a simple linear relationship between I_t and the SR, the variation in the SR is also 2.3%. The simulation of g_{mt} is performed by using the square law between the current and the transconductance. The reason for the small variation of g_{mt}, I_t and dc gain shown in simulation results is due to the non-ideal characteristics of the MOS transistor and the mismatch between β_{mn} and β_{mp}.

Tab. 1 Summary of aspect ratios of the transistors

Parameter	Value
MP/MCP	80/4
MN/MDN	24/4
MTP	160/4
MTN/MDN	48/4
M_{in}	48/4
MC	24/4
M1	12/4
M2	48/4
M3	150/2
M4	40/1
MP	300/2
MN	59.2/2

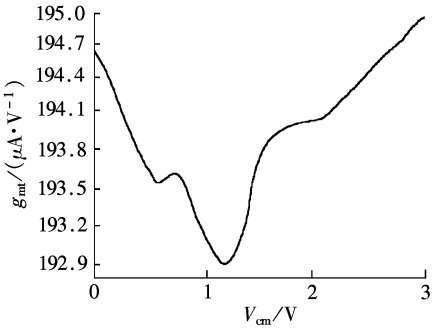

Fig. 4 g_{mt} vs. V_{cm}

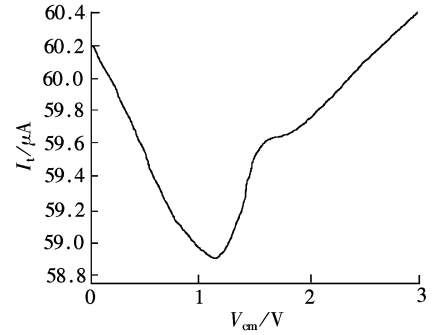

Fig. 5 I_t vs. V_{cm}

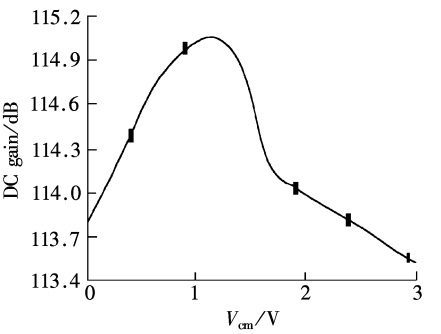

Fig. 6 DC gain vs. V_{cm}

It is interesting to notice the impact of the mismatch between the aspect ratios of the n-channel and the p-channel input transistors. Considering the process deviation which can increase the mismatch and weaken the performance of the proposed op-amp, two methods can be used to weaken the impact. The first one is to use the level shifter as in Refs. [2, 5]. With the help of the level shifter, double n-channel or p-channel input pairs can be utilized at a cost of sensitivity to noise caused by the power supply and variations in temperature. Another method is to make the input pairs work in a weak inversion region. But the SR will decrease drastically, as the tail current of the input pairs has to be reduced.

Fig. 7 shows frequency responses when V_{cm} varies from rail-to-rail in steps of 0.3 V. As observed, UGBW and PM remain almost independent of V_{cm}. It also supports the result shown in Fig. 4 that g_{mt} is constant.

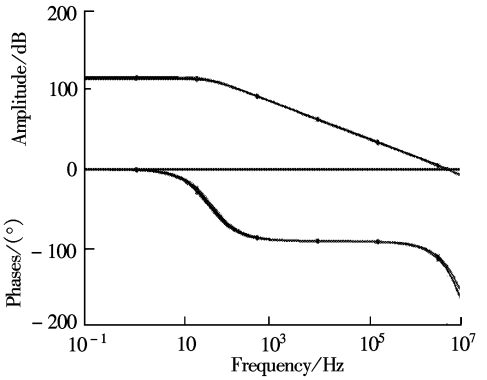

Fig. 7 Frequency responses

Fig. 8 shows large signal responses of the op-amp in unity-gain non-inverting configuration, with a load of 10 pF capacitance in parallel with a 10 kΩ resistor, to a 0.9 V pulse when initial V_{cm} changes from 0.1 to 1.9 V. Except that input voltage is less than 0.1 V or higher than 1.9 V as dotted lines shown in Fig. 8, both the rise rate and fall rate are changeless. Tab. 2 summarizes the performance of the proposed op-amp.

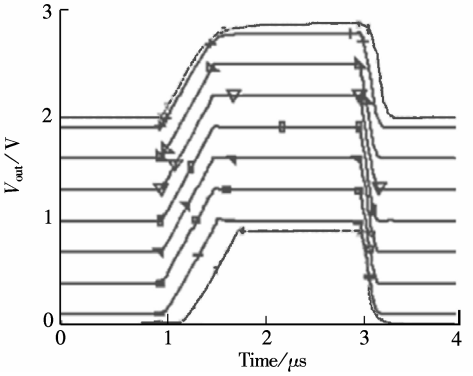

Fig. 8 Responses to large signals when initial V_{cm} varies from 0.1 to 1.9 V in step of 0.3 V

The rail-to-rail op-amp has been fabricated in DPDM 0.6 μm mixed-signal process. The layout of the rail-to-rail op-amp is shown in Fig. 9. The area of the layout is 0.072 mm^2.

Tab. 2 Performance of proposed op-amp

Parameter	Simulation value
Transconductance variation/%	1
Slewing current variation/%	2.3
Gain variation/dB	1.36
UGBW/MHz	4.8
Phase margin/(°)	60
Minimum supply/V	2.3
Power dissipation/MW	1.96
CMRR/dB	>80
PSRR/dB	>80

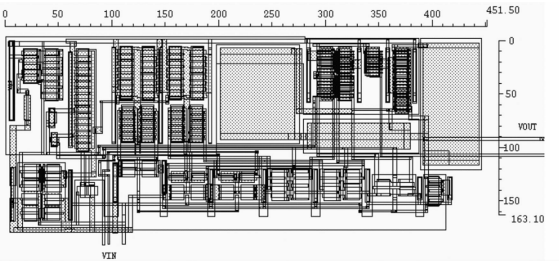

Fig. 9 Layout of rail-to-rail op-amp

Fig. 10 presents the input (A channel) and the output (B channel) waveforms of an improved Miller OTA connected as a unit gain buffer for a power supply of 3 V. Fig. 11 presents the square wave response of rail-to-rail op-amp. It shows that the SR is about 2.6 V/μs.

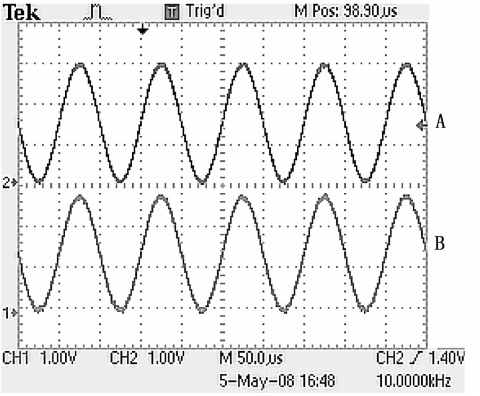

Fig. 10 The op-amp input A and output B waveforms

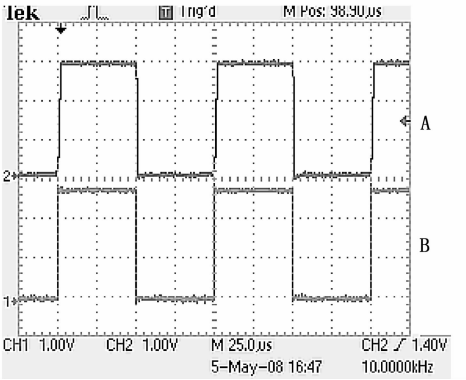

Fig. 11 A rail-to-rail op-amp square wave response

The tests perform closely to the schematic design only with about a 10% error. The parameters unavoidably decline

due to parasitic resistance and capacitance.

3 Conclusion

A novel rail-to-rail input stage is proposed in this paper. An op-amp based on the input stage is designed which shows a constant g_m, SR and gain. The simulation results of the op-amp with the input pairs working in a strong inversion region show that the variations in the g_{mt}, I_t and gain in the entire input common mode voltage range are only 1%, 2.3%, 1.36 dB, respectively. The test results are basically consistent with the circuit simulation.

To further improve the performance of the op-amp, focus should be put on the method to decrease the impact of mismatches between aspect ratios of n-channel and p-channel input transistors. The method should not introduce new sources of noise or weaken other performances of an op-amp.

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一种恒定跨导、摆率和增益的轨至轨运放

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摘要:提出了一种新型的通用低压轨至轨 CMOS 运放. 该运放在整个输入共模电压范围内获得了恒定的跨导、摆率和恒定的高增益. 所提出的电路有应用于深亚微米工艺的潜力,因为运放电路的运行不依赖于晶体管平方率或线性率的约束. 因此该电路比较紧凑,适用于 VLSI 单元的应用. 轨至轨 CMOS 运放采用 DPDM CMOS 混合信号工艺设计,模拟结果表明在整个输入共模电压范围内,跨导、摆率和增益的波动分别为 1%,2.3%和 1.36 dB. 在此基础上进行了版图设计和流片测试,版图面积为 0.072 mm^2,实际测试结果与模拟结果基本一致.

关键词:CMOS 模拟电路;放大器;轨至轨;恒定跨导;恒定摆率;恒定增益

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