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Wideband CMOS LC VCO design and phase noise analysis

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Abstract: A wideband LC cross-coupled voltage controlled oscillator(VCO) is designed and realized with standard 0.18 μm complementary metal-oxide-semiconductor (CMOS) technology. Band switching capacitors are adopted to extend the frequency tuning range, and the phase noise is optimized in the design procedure. The functional relationships between the phase noise and the transistors' width-length ratios are deduced by a linear time variant (LTV) model. The theoretical optimized parameter value ranges are determined. To simplify the calculation, the working region is split into several sub-ranges according to transistor working conditions. Thus, a lot of integrations are avoided, and the phase noise function upon the design variables can be expressed as simple proportion formats. Test results show that the DC current is 8.8 mA under a voltage supply of 1.8 V; the frequency range is 1.17 to 1.90 GHz, and the phase noise reaches −83 dBc/Hz at a 10 kHz offset from the carrier. The chip size is 1.2 mm × 0.9 mm.

Key words: voltage controlled oscillator(VCO); wideband; phase noise

Voltage controlled oscillators(VCOs) are common functional blocks in modern RF communication systems[1]. The VCO performance in terms of phase noise and tuning range determines the basic performance characteristics of a transceiver. The current trend toward multi-band multi-standard transceivers and broadband systems has generated interest in VCOs that simultaneously achieve a very wide tuning range and a low phase noise[2].

LC VCOs have been successfully used in narrowband wireless transceivers. There is a growing interest in extending their tuning range. Recently, several wideband CMOS LC VCOs using a variety of techniques have been demonstrated[3]. The high intrinsic C_{max}/C_{min} in version- or accumulation-type MOS varactors supports a very wide tuning range and their Q is sufficiently high that a good phase noise performance can be maintained[4].

In this paper, a wideband cross-coupled LC VCO is designed and realized with TSMC 0.18 μm CMOS technology. With band switching capacitors, the overall tuning frequency range is divided into 16 bands, which covers the range of 1.17 to 1.9 GHz. A linear time variant(LTV) model is used to quantitatively analyze voltage biased oscillators. In order to minimize the phase noise, MOSFET sizes are optimized.

The VCO can be used in the digital video broadcast (DVB) system[5]. It acts as a local frequency source, which transforms the radio frequency(RF) signal to the intermediate frequency(IF) signal.

1 Circuit Design

The schematics of the wideband LC VCO is shown in Fig. 1. The oscillation core includes both PMOS and NMOS cross-coupled amplifiers. The advantage is current reuse, which means the same current can provide more negative resistance. The tank consists of a symmetrical inductor and two varactors. Four band switching metal-insulator-metal(MIM) capacitor branches are paralleled with the tank, connected with nodes P and N. They are used to adjust the output frequency coarsely. The output buffers are source followers. Two resonant circuits, with a resonant frequency of $2\omega_0$, consist of L_2, C_2 and L_3, C_3. They can depress the deterioration of the tank quality factor, which is caused by the cross-coupled amplifiers. It is called a noise filtering technique[6].

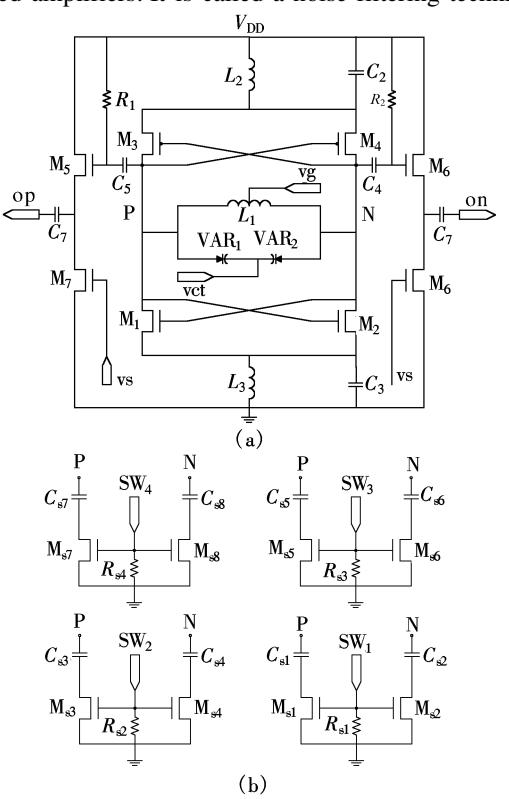

Fig. 1 Wideband VCO schematic. (a) Oscillation circuit; (b) Band switching circuit

2 Band Switching Array

Band switching techniques expand an intrinsically narrow tuning range without incurring excessive tuning sensitivity[7]. In recent years, it has been used extensively. Fig. 2 shows a generic binary-weighted band switching LC tank of size n. It is a half circuit of the resonator in Fig. 1 with n = 4. The minimum and maximum oscillation frequencies can be calculated by

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$$f_{\min}=\frac{1}{2\pi\sqrt{L(C_{\mathrm{v,max}}+(2^n-1)C+C_{\mathrm{para}})}} \quad (1)$$

$$f_{\max}=\frac{1}{2\pi\sqrt{L\left(C_{\mathrm{v,min}}+(2^n-1)\frac{CC_{\mathrm{d}}}{C+C_{\mathrm{d}}}+C_{\mathrm{para}}\right)}} \quad (2)$$

where C is the capacitor value of C_{s}, C_{d} is the parasitic capacitance in the drain of the switching MOSFET, C_{para} is the parasitic capacitance with cross-coupled transistors M_1 to M_4, and C_{v} is the varactor capacitance.

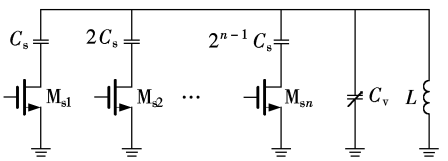

Fig. 2 Band switching capacitor array

Since the band switching capacitors are increased as binary-weights, the switching MOSFET sizes are different. Correctly scaling the transistors can make the band switching capacitors work properly. Capacitor series with too small transistors cannot be switched in the tank. And with too large transistors, parasitic capacitance will still remain in the tank even with the switch tuned off. Sweeping the transistor size, the capacitance switched in the tank can be plotted as in Fig. 3.

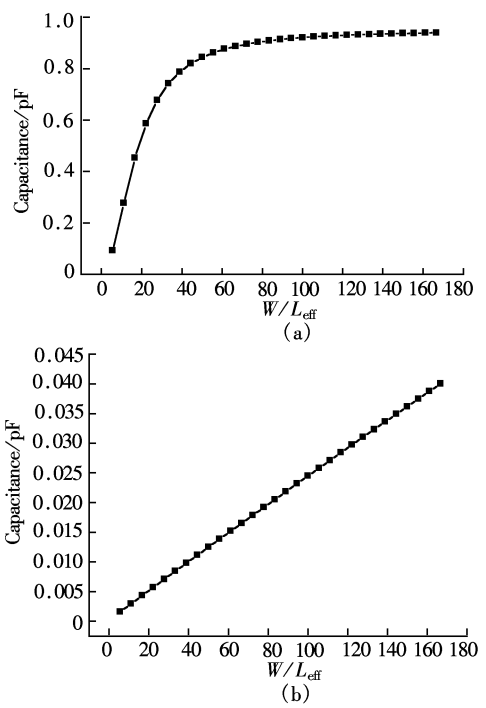

Fig. 3 Capacitance with switch on and off. (a) Switch on; (b) Switch off

The results shown in Fig. 3 are obtained by sweeping the transistor's width-length ratio, and setting the MIM capacitance to 0.95 pF. W is the transistor width, and L_{eff} is the transistor effective length. It can be clearly seen from Fig. 3 that, with this capacitance, a suitable transistor size is between 60 and 80. Increasing capacitance, the corner in Fig. 3 (a) will move rightwards. This indicates the increase in the transistor size. Contrarily, decreasing capacitance will move the corner leftwards. The transistor size should be reduced. Finally, for capacitors in every band switching branch, a suitable transistor size can be determined by simulation.

3 Phase Noise Analysis

3.1 Oscillation amplitude

For a voltage biased oscillator, the bias current varies with transistor size. When W/L_{eff} increases, bias current increases. With a smaller W/L_{eff}, the circuit works in a current limited region. In this region, the oscillation amplitude A is in direct proportion to the total bias current I_{B}[8]

$$A=\frac{4}{\pi}I_{\mathrm{B}}R_{\mathrm{p}} \quad (3)$$

where R_{p} is the equivalent parallel resistance of the tank. The relationship between I_{B} and bias voltage V_{GS} is

$$I_{\mathrm{B}}=2I_{\mathrm{DS}}=K(V_{\mathrm{GS}}-V_{\mathrm{TH}})^2=\mu C_{\mathrm{ox}}\frac{W}{L_{\mathrm{eff}}}(V_{\mathrm{GS}}-V_{\mathrm{TH}})^2 \quad (4)$$

where I_{DS} is the drain current. From Eqs. (3) and (4), it can be seen that the oscillation amplitude A is in direct proportion to W/L_{eff},

$$A=\frac{4}{\pi}\mu C_{\mathrm{ox}}\frac{W}{L_{\mathrm{eff}}}(V_{\mathrm{GS}}-V_{\mathrm{TH}})^2R_{\mathrm{p}}\propto\frac{W}{L_{\mathrm{eff}}} \quad (5)$$

When W/L_{eff} is large enough, the circuit works in a voltage limited region, and the oscillation amplitude approaches $V_{\mathrm{DD}}/2$ and no longer increases with W/L_{eff}. V_{DD} is the supply voltage.

3.2 Transistor size

Properly selected width-length ratio and correct working conditions will reduce phase noise contributed by channel current noise, which is a main contributor to phase noise[9]. The formula used by the LTV model to calculate phase noise contributed by channel current noise is[10]

$$L(\Delta\omega)=10\log\left(\frac{\Gamma_{\mathrm{rms}}^2\overline{i_{\mathrm{ds}}^2}}{2C^2A^2\Delta\omega^2}\right)=10\log\left(\frac{\Gamma_{\mathrm{rms}}^2\alpha^2(\phi)\overline{i_{n0}^2}}{2C^2A^2\Delta\omega^2}\right) \quad (6)$$

where Γ_{rms} is the rms (root-mean-square) value of the ISF (impulse sensitive function) in one period. The ISF describes the noise conversion factor to phase noise. $\overline{i_{\mathrm{ds}}^2}$ is the channel current noise mean square value in unit bandwidth. It can be decomposed into a stationary noise $\overline{i_{n0}^2}$ and a deterministic periodic function $\alpha(\phi)$ describing the noise amplitude modulation[10]. C is the tank node capacitance; A is the tank amplitude. $\Gamma_{\mathrm{rms,eff}}$, with the expression of $\Gamma_{\mathrm{rms,eff}}=\Gamma_{\mathrm{rms}}\alpha(\phi)$, is the root-mean-square value of the effective ISF.

The fraction in parentheses of Eq. (6) is the noise-carrier power ratio

$$\frac{P_{\mathrm{noise}}}{P_{\mathrm{carrier}}}=\frac{1}{2C^2\Delta\omega^2}\frac{\Gamma_{\mathrm{rms}}^2\overline{i_{\mathrm{ds}}^2}}{A^2}=\frac{1}{2C^2\Delta\omega^2}\frac{\Gamma_{\mathrm{rms,eff}}^2\overline{i_{n0}^2}}{A^2} \quad (7)$$

The first product is independent of W/L_{eff}. In the follow-

ing analysis, Eq. (7) is considered as a function of W/L_{eff}. The purpose of optimization is to find a W/L_{eff} which corresponds to the minimum noise-carrier power ratio.

In a current limited region, the tank output signal is assumed as

$$V_{\text{P}} = A\cos(\phi)\ V_{\text{N}} = -A\cos\phi \tag{8}$$

The transconductance of M_1 and M_2 are

$$g_{\text{m1}} = K_{\text{n}}(V_{\text{GS}} + A\cos\phi - V_{\text{TH}}) = K_{\text{n}}A(\cos\phi + \frac{V_{\text{GS}} - V_{\text{TH}}}{A}) = K_{\text{n}}A(\cos\phi - \cos\Phi) \tag{9}$$

$$g_{\text{m2}} = K_{\text{n}}A(-\cos\phi - \cos\Phi) \tag{10}$$

where $(V_{\text{GS}} - V_{\text{TH}})/A = -\cos\Phi$. This equals

$$\Phi = \pi - \arccos\left(\frac{V_{\text{GS}} - V_{\text{TH}}}{A}\right) \qquad \frac{\pi}{2} \leqslant \Phi \leqslant \pi \tag{11}$$

Because $g_{\text{m1}} \geqslant 0$, $\cos\phi \geqslant \cos\Phi$ must be satisfied, we, thus, have $-\Phi \leqslant \phi \leqslant \Phi$. Calling Φ half the conduction angle, it represents that transistors conduct only a fraction of a time period. When overdriven voltage becomes zero, Eq. (11) becomes $\phi = \Phi$.

The channel current noise power density and its ISF are[9]

$$\overline{i_{\text{ds1}}^2} = 4kT\gamma g_{\text{m1}} = 4kT\gamma KA(\cos\varphi - \cos\Phi) = \overline{i_{n0}^2}\alpha(\varphi)^2 \tag{12}$$

$$\Gamma_{\text{ids1}}(\varphi) = -\sin\varphi\frac{g_{\text{m2}}}{g_{\text{m1}} + g_{\text{m2}}} \tag{13}$$

where

$$\overline{i_{n0}^2} = 4kT\gamma KA$$
$$\alpha(\phi) = \sqrt{\cos\phi - \cos\Phi} \tag{14}$$

Substituting Eq. (5) into Eq. (14), we have

$$\overline{i_{n0}^2} = 4kT\gamma KA = \frac{\pi kT\gamma}{(V_{\text{GS}} - V_{\text{TH}})^2 R_{\text{p}}}A^2 \propto A^2 \tag{15}$$

Substituting Eq. (15) into Eq. (7), we obtain the noise-carrier power ratio

$$\frac{P_{\text{noise}}}{P_{\text{carrier}}} \propto \frac{\Gamma_{\text{rms, eff}}^2\overline{i_{n0}^2}}{A^2} \propto \Gamma_{\text{rms, eff}}^2 \tag{16}$$

And

$$\Gamma_{\text{rms, eff}}^2 = \frac{1}{2\pi}\int_{-\Phi}^{\Phi}\Gamma_{\text{ids1}}^2(\varphi)\alpha^2(\varphi)\,\text{d}\varphi = \frac{1}{2\pi}\int_{-\Phi}^{\Phi}\sin^2(\varphi)\left(\frac{g_{\text{m2}}}{g_{\text{m1}} + g_{\text{m2}}}\right)^2\alpha^2(\varphi)\,\text{d}\varphi = \frac{1}{8\pi}\int_{-\Phi}^{\Phi}\sin^2(\varphi)\left(\frac{\cos\varphi + \cos\Phi}{\cos\Phi}\right)^2(\cos\varphi - \cos\Phi)\,\text{d}\varphi \tag{17}$$

With computer calculation, the integration of Eq. (17) can be obtained:

$$\Gamma_{\text{rms, eff}}^2 = \frac{46\sin\Phi\cos^4\Phi - 17\cos^2\Phi\sin\Phi + 16\sin\Phi + 15\Phi\cos\Phi - 60\Phi\cos^3\Phi}{480\pi\cos^2\Phi} \tag{18}$$

Substituting Eqs. (5), (11) and corresponding technology parameters into Eq. (18), it can be proved that the noise-carrier power ratio is a function of W/L_{eff}. Their relationship is plotted in Fig. 4.

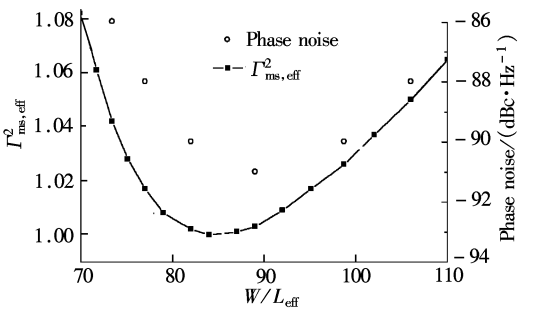

Fig. 4 Phase noise optimization

The curve is noise-carrier power ratio. The Y axis is normalized to its minimum value. The scattered circles are simulated phase noise. The results of calculation and simulation are similar. With W/L_{eff} of NMOS around 90, the circuit has the lowest phase noise. Because the mobility ratio of electrons and holes is 4 : 1, W/L_{eff} of PMOS should be four times that of NMOS.

In a voltage limited region, the amplitude A increases very slowly, and the half conduction angle Φ does not change. From Eq. (18), Γ_{rms} is constant. The channel current noise can be obtained from Eq. (14)

$$\overline{i_{n0}^2} = 4kT\gamma KA \propto \frac{W}{L_{\text{eff}}} \tag{19}$$

So in a voltage limited region, the noise-carrier power ratio is in direct proportion to W/L_{eff}.

From the analysis above, the minimum noise-carrier power ratio is in a current limited region. And the corresponding W/L_{eff} is the optimized MOSFET parameter.

4 Measurement

The circuit is realized with TSMC's 0.18-μm 1P6M CMOS technology. Fig. 5 shows the die microphotograph. The size is 1.2 mm × 0.9 mm.

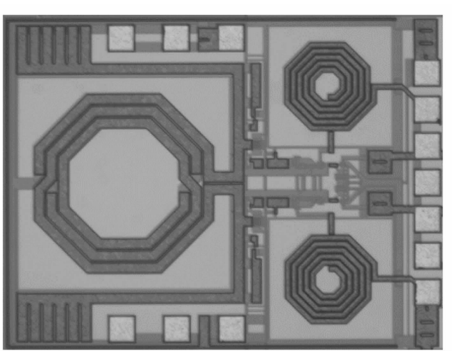

Fig. 5 Die microphotograph of the VCO

The VCO chip is measured using on-wafer probes together with a spectrum analyzer. Under a voltage supply of 1.8 V, the DC current is 8.8 mA. The frequency-voltage characteristics are shown in Fig. 6. Sixteen bands cover 1.17 to 1.90 GHz.

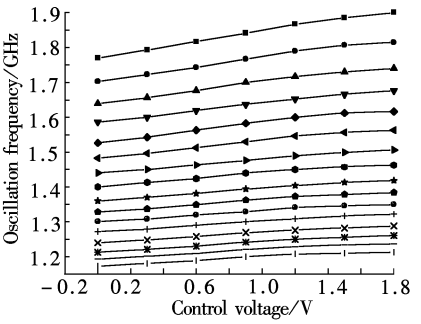

Fig. 6 Frequency vs. tuning voltage

The measured phase noise of the output signal is shown in Fig. 7. The output power of one single-ended signal across a 50 Ω load is −8 dBm, and the phase noise is −83 dBc/Hz at a 10 kHz offset from the carrier.

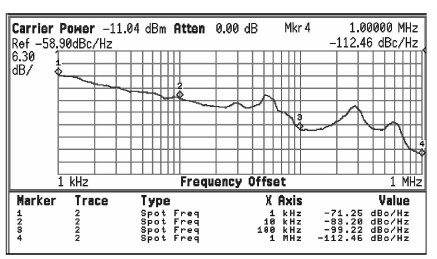

Fig. 7 Phase noise

5 Conclusion

The tuning frequency range and the phase noise are VCOs' key parameters. This paper presents the design of a wideband CMOS LC VCO with a 47% tuning range. The design of a band-switching capacitors array is discussed in detail. Phase noise analysis for voltage-biased cross-coupled LC oscillators is based on the LTV model. By means of mathematical deduction, the relationships among the phase noise and transistor parameters, the phase noise and the inductance are given, and the optimized transistor parameters are obtained quantitatively.

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宽带 CMOS LC 压控振荡器设计及相位噪声分析

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摘要：应用标准 0.18 μm CMOS 工艺设计并实现了宽带交叉耦合 LC 压控振荡器. 采用开关电容阵列拓宽频率范围. 设计过程中对相位噪声进行了优化. 应用线性时变模型(LTV)推导出相位噪声与 MOS 晶体管宽长比之间的函数关系，从理论上给出相位噪声性能最优的元件参数取值范围. 为简化推导过程，针对电路特点按晶体管工作状态来细分电路工作区域，从而避免了大量积分运算，以尽可能简单的比例形式得到相位噪声与设计变量间的函数关系. 测试结果表明，在 1.8 V 电源电压下，核心电路工作电流为 8.8 mA，压控振荡器的频率范围为 1.17 ~ 1.90 GHz，10 kHz 频偏处相位噪声达到 −83 dBc/Hz. 芯片面积为 1.2 mm × 0.9 mm.

关键词：压控振荡器；宽频带；相位噪声

中图分类号：TN75