

Implementation and noise optimization of a 433 MHz low power CMOS LNA

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Abstract: A low power 433 MHz CMOS (complementary metal-oxide-semiconductor transistor) low noise amplifier (LNA), used for an ISM (industrial-scientific-medical) receiver, is implemented in a 0.18 μm SMIC mixed-signal and RF (radio frequency) CMOS process. The optimal noise performance of the CMOS LNA is achieved by adjusting the source degeneration inductance and by inserting an appropriate capacitance in parallel with the input transistor of the LNA. The measured results show that at 431 MHz the LNA has a noise figure of 2.4 dB. The S_{21} is equal to 16 dB, $S_{11} = -11$ dB, $S_{22} = -9$ dB, and the inverse isolation is 35 dB. The measured input 1-dB compression point ($P_{1\text{dB}}$) and input third-order intermodulation product (IIP3) are -13 dBm and -3 dBm, respectively. The chip area is 0.55 mm \times 1.2 mm and the DC power consumption is only 4 mW under a 1.8 V voltage supply.

Key words: low noise amplifier (LNA); cascode; low power; noise figure; noise optimization

The first stage of a wireless RF receiver is typically a low noise amplifier whose performance is very important for the entire receiver, as it dominates the sensitivity. In fact, the LNA design always involves trade-offs between noise and other performances, such as gain, power, impedance matching, stability, and linearity^[1-3]. Generally, the main goal of the LNA design is to achieve simultaneously low noise and good input matching for the given power consumption and request frequency conditions. CMOS has become an attractive process for radio transceiver implementation of various wireless communication systems due to larger down scaling, higher level of integrability, lower cost, etc. A number of CMOS LNA design techniques have been reported to satisfy these goals, including classical noise matching techniques, simultaneous noise and input matching techniques, power-constrained noise optimization techniques and power-constrained simultaneous noise and input matching techniques^[4]. However, those previously reported works did not present a comprehensive analysis for low power and several hundreds megahertz LNA design optimization techniques.

1 Noise Optimization Techniques

A single-stage cascode amplifier shown in Fig. 1 (a) is chosen to minimize the power dissipation and improve the

IIP3 performance. The cascode configuration is chosen to improve reverse isolation and reduce the Miller effect. Optimal noise performance, however, is achieved with inductive degeneration at the source and shunt capacitance at the gate. Along with transistor M_1 , M_3 forms a current mirror. To minimize the power overhead of the bias circuit, the gate width of that of M_3 is a small fraction of that of M_1 . The current through M_3 is set by the supply voltage and R_{ref} in conjunction with the V_{gs} of M_3 . The resistance R_{bias} is chosen great enough so that its equivalent noise current is very small and can be ignored.

Fig. 1 (b) shows the simplified small-signal equivalent circuit for the noise analysis including a transistor noise model, where C_{gs} represents the gate-source capacitance of the input transistor M_1 and $C_t = C_{\text{gs}} + C_{\text{ex}}$. In Fig. 1 (b), the effects of the common gate transistor M_2 on the noise and frequency response are ignored to simplify the analysis; furthermore, the parasitic resistances of gate, body, source, and drain terminal are also ignored^[5-6].

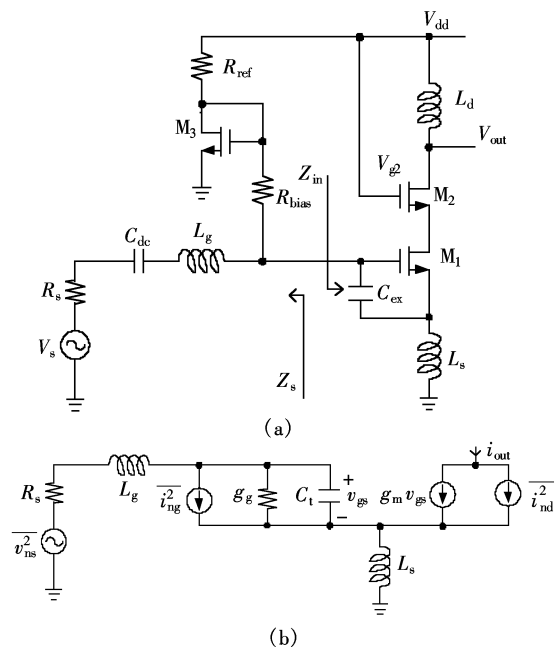


Fig. 1 The proposed topology of cascode LNA. (a) Schematic; (b) Simplified small-signal equivalent circuit for noise analysis

In Fig. 1 (b), the mean-squared channel thermal noise current is given in Ref. [7].

$$\overline{i_{\text{nd}}^2} = 4KT\gamma g_{\text{d0}} \Delta f \quad (1)$$

where g_{d0} is the drain-source conductance at zero V_{ds} . The parameter γ has a value of unity at zero V_{ds} and, in long devices, approaches a value of 2/3 in saturation.

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As given in Ref. [7], the mean-squared gate-induced noise current can be expressed as

$$\overline{i_{ng}^2} = 4KT\delta g_g \Delta f \quad (2)$$

where $g_g = \omega^2 C_{gs}^2 / (5g_{d0})$. van der Ziel gave a value of $4/3$ (twice γ) for the gate noise coefficient δ in long-channel devices.

Since the gate-induced noise current has a correlation with the channel noise current, a correlation coefficient is formally defined as

$$c \equiv \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}} \sqrt{\overline{i_{nd}^2}}} \quad (3)$$

For long channel devices, the value of c is theoretically $-j0.395$; i.e. c is purely imaginary, reflecting the capacitive coupling between the channel and gate-induced noise sources.

Based on the definition of the noise factor, the analytical expressions for the noise parameters shown in Fig. 1(b) can be obtained and expressed as

$$R_n = \frac{\gamma}{a} \frac{1}{g_m} \quad (4)$$

$$Z_{opt} = Z_{opt}^o - j\omega L_s \quad (5)$$

$$F_{min} \approx 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \quad (6)$$

where $a = g_m / g_{d0}$, $\omega_T = g_m / C_{gs}$ and

$$Z_{opt}^o = \frac{\sqrt{\frac{a^2\delta}{5\gamma} (1 - |c|^2)} + j\left(\frac{C_t}{C_{gs}} + a|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs} \left\{ \frac{a^2\delta}{5\gamma} (1 - |c|^2) + \left(\frac{C_t}{C_{gs}} + a|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2 \right\}} \quad (7)$$

Eqs. (4), (5) and (6) are the derived noise parameters as shown in Fig. 1(b). Compared with the two-port noise parameter expressions of an intrinsic MOSFET, the circuit shown in Fig. 1(a) only adds passive inductors and capacitors, which cannot induce noise degeneration in theory if these components are ideal; the minimum noise figure and noise resistance are not affected by the additional components; just the optimized source impedance is changed under the assumed conditions. This topology has the benefit of simultaneously achieving both input and noise matching for the LNA^[8-9].

For Fig. 1(a), the source impedance of the LNA is

$$Z_s = R_s + j\omega L_g \quad (8)$$

In the LNA design, the main goal is to achieve noise matching in the input termination to obtain the minimum noise factor. The condition that allows the noise matching is

$$Z_{opt} = Z_s = Z_{opt}^o - j\omega L_s \quad (9)$$

For the topology illustrated in Fig. 1(a), the input impedance of the amplifier can be derived from the equivalent circuit

$$Z_{in} = j\omega L_s + \frac{1}{j\omega C_t} + \frac{g_m L_s}{C_t} \quad (10)$$

As can be seen from Eq. (10), the source degeneration inductance generates the real part of the input impedance. This is important because there is no real part in Z_{in} without degeneration, while there is in Z_s and Z_{opt} . Furthermore, the imaginary part of Eq. (10) is changed by $j\omega L_s$, and this is followed by the same change in Z_{opt} . These characteristics are very important in order to achieve simultaneous noise and input matching at any given amount of power dissipation.

From Eq. (7), in a low power LNA design, the gate-source parasitic capacitance C_{gs} (the small transistor size) is very small; the product of ω and C_{gs} becomes increasingly smaller with decreasing frequency. If there is no shunt capacitance C_{ex} , the multiple factor C_t / C_{gs} is equal to unity which makes the real part of Z_{opt} greater than the real part of Z_s . In addition, the sum of L_g and L_s has to be very large so that the imaginary part of Z_{opt} is equal to the imaginary part of Z_s . At the same time, in order to guarantee input impedance matching to achieve simultaneous noise and input matching, $g_m L_s / C_t$ should be equal to R_s , so that the value of L_s does not charge too much due to the addition of C_{ex} . The value of L_g must be greater than a certain value. As a result, the minimum achievable noise figure of the LNA can be considerably higher than F_{min} of the common-source transistor, spoiling the idea of simultaneous noise and input matching. The main reason is that the parasitic resistance of a large L_g can become non-negligible, which can cause noise deterioration^[10]. Furthermore, the ratio C_t / C_{gs} inside the square part of the denominator compensates for the decrease in the product ωC_{gs} . Considering the relationship between the cutoff frequency f_t and the total input capacitance, the addition of C_{ex} leads to the reduction in the f_t , furthermore leading to power-gain degradation^[4].

The qualitative description of the power constrained simultaneous noise and input matching technique is given as follows. First, the bias and the transistor sizes are chosen according to the power constraint. There is an optimized bias point and transistor size that provides the minimum F_{min} in theory. Secondly, the additional capacitance C_{ex} , as well as the degeneration inductor L_s , is chosen to make the real part of Z_{opt} and Z_{in} equal R_s simultaneously. The value of C_{ex} is chosen according to the size of L_s and the available power gain. Finally, the gate series inductance L_g is chosen to make the imaginary part of Z_{opt} equal the imaginary part of Z_s . For a given L_s in Eq. (10), the imaginary value of the optimum noise impedance will be automatically approximately equal to that of the imaginary input impedance with an opposite sign.

2 LNA Design

In this design, the value of L_s is 4.2 nH, implemented by an on-chip spiral inductor and wire bonding. The value of L_g is 130 nH, implemented by combining an off-chip inductor and wire bonding. C_{ex} is 450 fF and implemented on-chip. The size of transistors M_1 and M_2 is 0.18 $\mu\text{m} \times 96 \mu\text{m}$. L_d

is also implemented by an on-chip spiral inductor, and is initially chosen to achieve a maximum transducer gain. The value of L_d is 5.1 nH. A simple off-chip L-C network is added to match the output of the LNA. The gate voltage of M_1 is set to 0.6 V through the bias circuit. The LNA dissipates the total current of 2 mA from the supply voltage of 1.8 V in simulation.

Fig. 2 shows the simulated noise figure (NF), the minimum noise figure NF_{min} , and S_{21} as a function of frequency for the LNA topology shown in Fig. 1(a). As can be seen in Fig. 2, in addition to good noise matching, the NF of the LNA coincides with the NF_{min} of the transistor at the requested frequency, while the gain S_{21} is maximal. It proves that at this frequency a simultaneous noise and input matching is achieved. From Eq. (4), the noise resistance R_n of the proposed topology is not affected by adding C_{ex} , but depends only on the value of g_m . Therefore, the small transistor size and low-power dissipation can lead to a very high R_n , so the NF of the LNA increases sharply at the frequencies away from the optimum point.

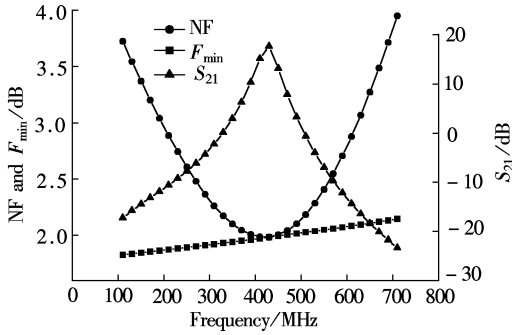


Fig. 2 The simulated NF, NF_{min} and S_{21}

3 Experimental Results

With the above description, the LNA shown in Fig. 1(a) is realized in the 0.18 μm SMIC (Shanghai, China) CMOS process. Fig. 3 shows the die photo of the implemented LNA. The chip area is 0.55 mm \times 1.2 mm. A ring ground-inductance package is used to improve reverse isolation. It

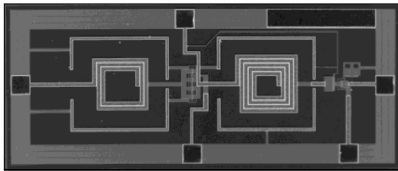


Fig. 3 Die photo of the LNA

can be seen that L_d and the on-chip degeneration inductor occupies about 40% of the chip area. The die is bonded to test the chip. The S -parameters and the noise figure of the realized LNA are measured with an Agilent E8363B VNA and an Agilent 8593A Spectrum Analyzer, respectively. The measured S -parameters of the LNA are shown in Fig. 4. At 431 MHz, the values of the S -parameters are as follows: $S_{21} = 16$ dB, $S_{11} = -11.8$ dB, $S_{12} = -35.8$ dB and $S_{22} = -9$ dB. A bond-wire should be added to the off-chip L-C output matching network for testing but the length of the bond-wire is difficult to control. The parasitical inductance of the bond-

wire makes S_{22} deviate from the central frequency. The main reason why reverse isolation is more than 35 dB is due to the use of a ground-shielded inductor and a cascode amplifier topology. The measured noise figure and gain of the LNA are shown in Fig. 5. The measured minimal NF is 2.4 dB at 430 MHz, while the maximal gain is 17.3 dB. As explained above, this achieves simultaneous noise and input matching at the requested frequency. The parasitic resistances of a large L_g and matching output network cause the noise deterioration and makes the measured NF larger than the simulated NF. Fig. 6 shows that the measured input 1-dB compression point P_{1dB} is -13 dBm and the input third-order intermodulation product IIP3 is -3 dBm. The LNA dissipates a 2.2 mA current from a 1.8 V supply. Due to the use of a single-stage topology, the linearity of the amplifier is good.

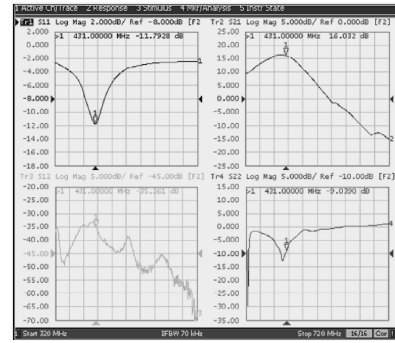


Fig. 4 Measured S -parameters

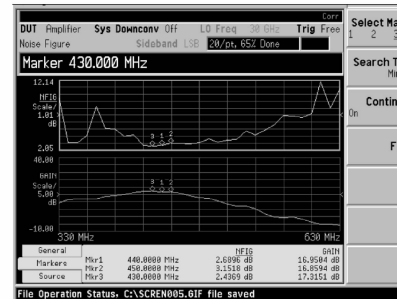


Fig. 5 Measured noise figure and gain of the LNA

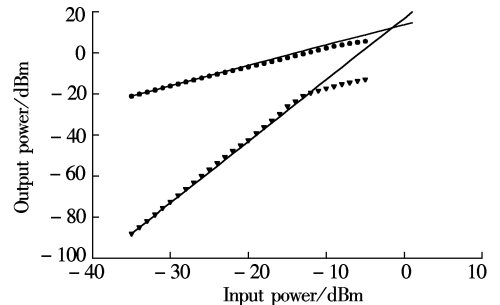


Fig. 6 Measured P_{1dB} and IIP3 of the LNA

4 Conclusion

A 433 MHz low-power CMOS LNA used for ISM is designed and implemented in SMIC's 0.18 μm CMOS technology. Measured results give an NF of 2.4 dB, a power gain of 16 dB, a 1-dB compression point of -13 dBm, and an input third-order intermodulation product of -3 dBm while dissipating a 2.2 mA current from a 1.8 V supply.

The low power consumption makes the direct ISM receiver architecture become a promising choice for long time communication. The overall behavior of the implemented LNA shows a good agreement with the proposed design principle and the theoretical analysis.

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433 MHz 低功耗 CMOS LNA 的噪声优化与实现

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摘要: 采用 0.18 μm SMIC 数模混合与射频(RF)CMOS 工艺实现了一个应用于 ISM(工业、科学和医疗)频段接收机的 433 MHz 低功耗低噪声放大器(LNA)的设计。电路通过调节源级反馈电感和在 LNA 输入晶体管上并联电容的方法实现了最优的噪声性能。测试结果表明, LNA 在 431 MHz 处的噪声系数为 2.4 dB, $S_{21} = 16$ dB, $S_{11} = -11$ dB, $S_{22} = -9$ dB, 反向隔离度大于 35 dB。测量的 1-dB 压缩点($P_{1\text{dB}}$)和输入三阶交调(IIP3)分别为 -13 dBm 和 -3 dBm。芯片面积为 0.55 mm \times 1.2 mm, 在 1.8 V 供电时整个电路功耗仅 4 mW。

关键词: 低噪声放大器; 共源共栅; 低功耗; 噪声系数; 噪声优化

中图分类号: TN924