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CMOS low-dropout regulator with 3.3 μA quiescent current without off-chip capacitor

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Abstract: A CMOS (complementary metal-oxide-semiconductor transistor) low-dropout regulator (LDO) with 3.3 V output voltage and 100 mA output current for system-on-chip applications to reduce board space and external pins is presented. By utilizing a dynamic slew-rate enhancement (SRE) circuit and nested Miller compensation (NMC) on the LDO structure, the proposed LDO provides high stability during line and load regulation without off-chip load capacitors. The overshot voltage is limited within 550 mV and the settling time is less than 50 μs when the load current decreases from 100 mA to 1 mA. By using a 30 nA reference current, the quiescent current is 3.3 μA. The proposed design is implemented by CSMC 0.5 μm mixed-signal process. The experimental results agree with the simulation results.

Key words: low-dropout regulator; off-chip capacitor; slew-rate enhancement circuit; nested Miller compensation(NMC)

With the rapid development of system-on-chip designs, there is a growing trend toward power-management integration. Compared with switching regulators, LDOs can provide low-noise and precision supply voltage with less chip area and fewer off-chip components. Thus, on-chip and local LDOs are widely utilized to power up sub-blocks individually in battery-powered communication systems, which can significantly reduce crosstalk and improve voltage regulation. In addition, system-on-chip designs with on-chip and local LDOs can significantly reduce both board space and external pins. However, the conventional LDO needs a large output capacitor to lower the dominant pole for stability considerations, and this becomes the main obstacle to fully integrating LDOs in system-on-chip design.

Due to the emerging needs of the LDO without off-chip capacitors for low-voltage mixed-signal systems, many researchers have proposed a variety of advanced methods to eliminate the off-chip capacitor. Leung et al. proposed a frequency compensation method, a damping factor control, to stabilize the LDO without off-chip capacitors[1]. Wang et al. proposed a method using nested Miller compensation with a feed-forward G_m stage[2]. Lam et al. proposed a method using direct current feed-back[3]. The main aims of all the proposed methods are: 1) To eliminate the off-chip capacitor; 2) To stabilize the feed-back loop; 3) To improve load regulation and transient response. However, the above methods cost a lot of quiescent current which is not suitable for low power design.

Based on the former study of low quiescent current LDOs[4-5], a CMOS LDO that is targeted for CMOS system-on-chip design is presented in this paper. Both the low quiescent current and the low overshot voltage are achieved due to the dynamic SRE structure and the large capacitor which is used in NMC.

1 Structure of Proposed Design

Fig. 1 shows the structure of the proposed design of the LDO. In Fig. 1, A_1 is a folded differential amplifier with single output, and A_2 is a source follower where a PMOS device is used as the input transistor; A_1 and A_2 form the error amplifier(EA) together. M_0 is the power transistor, and resistors R_{F1} and R_{F2} form the feedback networks. Block VREF is a bandgap voltage reference which provides a 0.6 V reference voltage. Capacitors C_{m1} and C_{m2} form the nested Miller compensation to stabilize the system loop. The dynamic SRE block is added between the OPOUT node and the VOUT node, and it provides an extra current, I_{SRE}, to charge the gate capacitor of M_0 when the output current changes from heavy load to light load. A 30 nA current reference[6] is used in the proposed design.

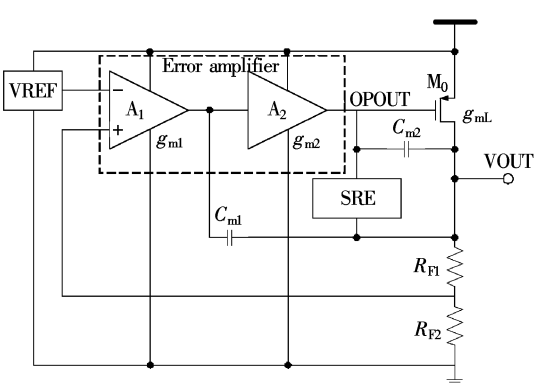

Fig. 1 The structure of proposed design of LDO

2 Dynamic Slew-Rate-Enhancement Circuits

Fig. 2 shows a novel SRE circuit which contains three modules: a reference block, a differentiator, and an operation device M_S. With this topology, the expression of extra current provided by the SRE circuit is

$$I_{SRE} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{M_s} \cdot \left(V_{DD} - V_{ref2} - \frac{dV_{OUT}}{dt}C_d R_d - |V_{THP}|\right)^2 \quad (1)$$

where V_{ref2} is the reference voltage of block VREF2.

According to Eq. (1), the SRE circuit is only sensitive to

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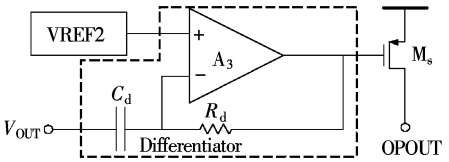

Fig. 2 The topology of the SRE circuit

the changes of V_{OUT}, and the DC magnitude of V_{OUT} will not change the value of I_{SRE}. Thus, this topology reduces the complexity of bias circuits for SRE, and is suitable for the LDO with programmable output voltage. With proper designed magnitude for V_{ref2}, the voltage drop between the supply voltage and V_{ref2} is less than a threshold voltage; thus, M_S is turned off to reduce the power consumption when V_{OUT} is stable. Then the quiescent current is saved. Moreover, since V_{OUT} changes the most at the beginning of load regulation, according to Eq. (1), the SRE circuit provides the maximum extra current at the same time which will push the OPOUT node to higher voltage and reduce the output current.

In order to clearly show the operation of the SRE circuit, the SRE circuit is simulated. Fig. 3 shows the transient simulation results of I_{SRE} and V_{OUT}. In such a simulation, V_{OUT} is used as an input signal to the SRE circuit and is generated by a piece-wise linear voltage source with three rising slopes and one falling slope; a parallel resistor and capacitor network is used as the load to M_S. As shown in Fig. 3, I_{SRE} is proportional to the changes of V_{OUT}, and equal to zero when V_{OUT} is stable.

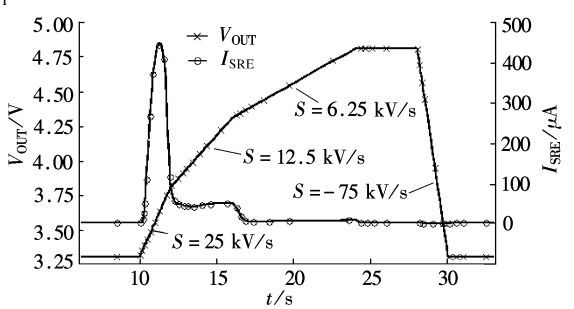

Fig. 3 V_{OUT} and source-drain current of M_S

3 Load Transient Responses

Although the SRE circuit provides the maximum I_{SRE} at the beginning of load regulation, it still needs time to charge the gate capacitor of M_0 and push the OPOUT node to a high voltage. In order to prove the load regulation, the capacitance of the Miller capacitor C_{m2} increases to a comparable level with the gate capacitor of M_0. Since, in the low power design, the error amplifier has low unit-gain bandwidth, it can be assumed that there is no output current from the error amplifier at the beginning of load regulation when an overshot voltage V_{over} occurs at the VOUT node. According to the theory of charge conservation and capacitors connected to OPOUT as shown in Fig. 4, it can be calculated that

$$V'_{OPOUT} = V_{OPOUT} + (V'_{OUT} - V_{OUT})\frac{C_{m2}}{C_P + C_{m2}} = V_{OPOUT} + V_{over}\frac{C_{m2}}{C_P + C_{m2}} \quad (2)$$

where V_{OPOUT} and V_{OUT} are the node voltages of OPOUT and VOUT before the beginning of load regulation; V_{OPOUT} and V_{OUT} are the node voltages after the beginning of load regulation; and C_P is the gate capacitor of M_0. According to Eq. (2), V_{OPOUT} will be pushed to a higher level immediately when overshot voltage occurs at the VOUT node. Fig. 5 shows the node voltages of VOUT and OPOUT during the load regulation. It can be seen that both voltages simultaneously increase.

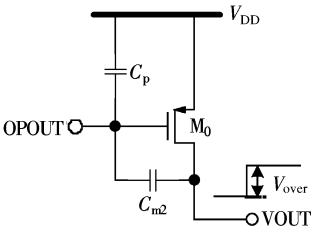

Fig. 4 The capacitors connected to OPOUT during load regulation

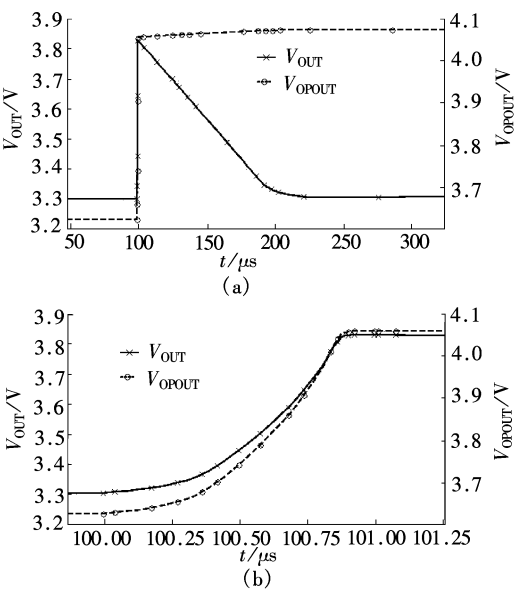

Fig. 5 The node voltages of VOUT and OPOUT during the load regulation without SRE circuit. (a) The whole procedure; (b) Details of rising part

Until V_{OUT} becomes stable again, the source follower stops to charge C_{m2} and C_p. As shown in Fig. 5, this procedure requires 120 μs without the SRE circuit, since the maximum output current of the error amplifier is 600 nA in this low power design. With the cooperation of C_{m2} and the SRE circuit, according to the experimental results, the overshot voltage is reduced to 550 mV, and the settling time is only 50 μs.

4 Nested Miller Compensation and Small Signal Analysis

Since the off-chip capacitor has been eliminated, and a large nested Miller capacitor and an SRE circuit have been added to the error amplifier, the pole-zero distribution and frequency compensation strategies are much more different from the LDO with off-chip capacitors. As shown in Fig. 1, the LDO can be viewed as a three-stage-amplifier with the power transistor as the last stage. Fig. 6 gives the schematic of

the core circuit of the proposed design, which includes the error amplifier, the power transistor, NMC, feedback network and the equivalent load capacitor and the resistor. Unlike the common NMC strategy[7], the first capacitor, C_{m1}, does not connect the output of the first gain stage to the VOUT, but is placed between the source of the cascade device M_C and VOUT.

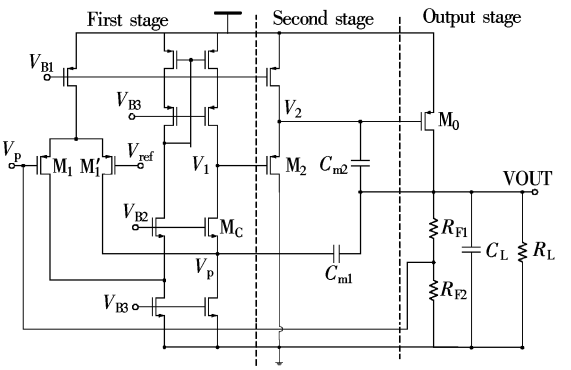

Fig. 6 The topology of the core circuit of LDO

By this method, the pole on VOUT has been pushed to a higher frequency by $g_{mc}R_{o1}$ times[8], where g_{mc} is the transconductance of the cascade device, M_C.

Fig. 7 gives the small signal model of the circuit shown in Fig. 6, where g_{mi} and R_{oi} are defined as the transconductance and the output resistance of the i-th gain stage respectively; g_{mL} is the transconductance of the power transistor, and R_L and C_L are the equivalent load resistor and the load capacitor caused by the load of the LDO.

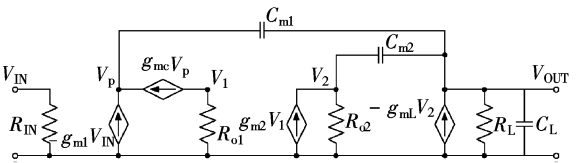

Fig. 7 The small signal model of the core circuit of LDO

Assume that C_{m1} and C_{m2} are much greater than the lumped output capacitor of each stage, based on such a small signal model and assumption, the transfer function is

$$A_{open}(s)=\frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left(1-s\frac{C_{m2}}{g_{mL}}-s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}g_{mc}R_{o1}}\right)}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1+s\frac{C_{m2}(g_{mL}-g_{m2})}{g_{m2}g_{mL}}+s^2\frac{C_{m2}C_L}{g_{m2}g_{mL}g_{mc}R_{o1}}\right]} \tag{3}$$

Besides, with an additional condition that $g_{mL}\gg g_{m1}$ and g_{m2}, the transfer function is rewritten as

$$A_{open}(s)=\frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left(1-s\frac{C_{m2}}{g_{mL}}-s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}g_{mc}R_{o1}}\right)}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1+s\frac{C_{m2}}{g_{m2}}+s^2\frac{C_{m2}C_L}{g_{m2}g_{mL}g_{mc}R_{o1}}\right]}\approx\frac{1-s\frac{C_{m2}}{g_{mL}}-s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}g_{mc}R_{o1}}}{\frac{sC_{m1}}{g_{m1}}\left[1+s\frac{C_{m2}}{g_{m2}}+s^2\frac{C_{m2}C_L}{g_{m2}g_{mL}g_{mc}R_{o1}}\right]} \tag{4}$$

According to the transfer function, there are two right-plane zeros and three left-plane poles. The poles and zeros are shown below:

The dominant pole

$$p_0=\frac{1}{C_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L} \tag{5}$$

The nondominant poles

$$p_2=\frac{g_{m2}}{C_{m2}} \tag{6}$$

$$p_3=\frac{g_{mL}g_{mc}R_{o1}}{C_L} \tag{7}$$

Two zeros

$$z_1=\frac{g_{mL}}{C_{m2}} \tag{8}$$

$$z_2=\frac{g_{m2}g_{mc}R_{o1}}{C_{m1}} \tag{9}$$

According to the theory of multistage amplifier frequency compensation[7], in order to separate three poles, condition $GBW\leqslant p_2/2\leqslant p_3/4$ must be satisfied and this is achieved by

$$\frac{g_{m1}}{C_{m1}}\leqslant\frac{1}{2}\frac{g_{m2}}{C_{m2}}\leqslant\frac{1}{4}\frac{g_{mL}g_{mc}R_{o1}}{C_L} \tag{10}$$

When using this topology, the pole at the output will be the nondominant pole. According to Eq. (7), the frequency of this pole depends on the transconductance of the power transistor and load capacitance. Larger transconductance and smaller load capacitance result in higher frequencies of the nondominant pole. Therefore, the worst case stability occurs at zero load-current condition since the transconductance has the minimum value (about 76 μA/V, typically) when only a current equalling $V_{OUT}/(R_{F1}+R_{F2})\approx 1$ μA drains from the power transistor. AC analysis is done under this condition, and simulation results are shown in Fig. 8. It can be seen that

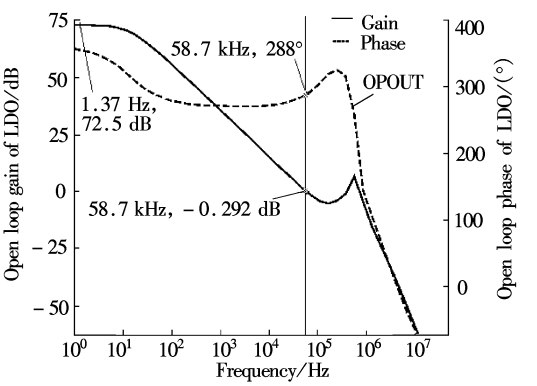

Fig. 8 Open-loop frequency response of LDO

there is a doublet above the unit-gain-bandwidth, and the zero of the doublet helps the phase margin reach 108°. Thus, the loop is stable. In the proposed design, most of the settling time is caused by limited charging current into the gate of M_0 and C_{m2}; thus, the affection of the doublet to the settling time can be neglected in this application.

5 Results and Discussion

The proposed design of the LDO is implemented by using a CSMC 0.5 μm mixed-signal process. The chip occupies 0.76 mm^2 of area and consumes 3.3 μA of quiescent current. The microphotograph of the proposed LDO with a dynamic SRE circuit is shown in Fig. 9; most of the area is invested in the 100 pF Miller compensation capacitor and power transistor. The LDO is designed to provide a 3.3 V output voltage with a maximum 100 mA output current and a 200 mV dropout voltage. All the performance of the LDO is measured without off-chip output capacitor, and Tab. 1 summarizes the performance of the proposed LDO.

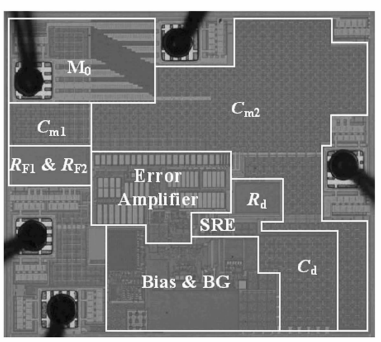

Fig. 9 The microphotograph of the proposed LDO

Tab. 1 Summary of the performance of the proposed LDO

Parameters	Value
Technology	0.5 μm CSMC
Chip area/μm^2	927 × 819
Supply voltage/V	3.5 to 5
Quiescent current/μA	< 3.3
Dropout voltage	200 mV @ 100mA
Present output voltage/V	3.3
Error due to line and load changes/%	< 0.39
Overshot voltage	550 mV @ 100 mA to 1 mA load regulation
Settling time(the worst case)	50 μs @ 100 mA to 1 mA load regulation
PSRR(V_{IN} = 5 V, I_{OUT} = 100 mA)	56.6 dB @ 10 Hz 52.3 dB @ 1 kHz

The output voltage and quiescent current during the line and load regulations are measured by Agilent 34411A 6.5 Digit Multimeter, and experimental results are shown in Fig. 10 and Fig. 11, respectively. Due to the 72.5 dB loop gain, the total error of the output voltage caused by line and load variation is just 0.39%. Because of the dynamic SRE circuit and the 30 nA current reference, the quiescent current remains less than 3.3 μA during the line and load regulation.

The load and line transient response of the LDO are observed by a Tektronix TDS5034B digital phosphor oscilloscope, and the experimental results are shown in Fig. 11 and Fig. 12, respectively. Since the quiescent current is only 3.3 μA, the overshot voltage and the settling time are larger than that of Leung's design[1]. Fig. 12 shows that the overshot voltage is less than 550 mV and the settling time is less than 50 μs during the load transient response. Fig. 13 shows that the overshot voltage is less than 400 mV during the line transient response.

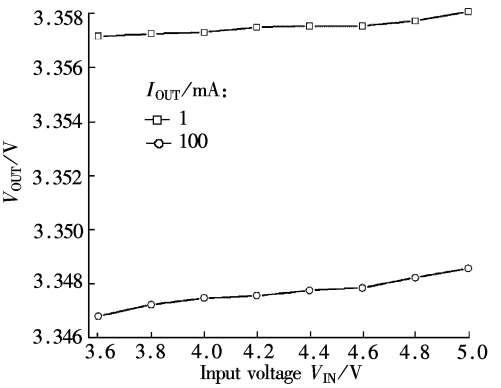

Fig. 10 The output voltage of LDO during load and line regulation

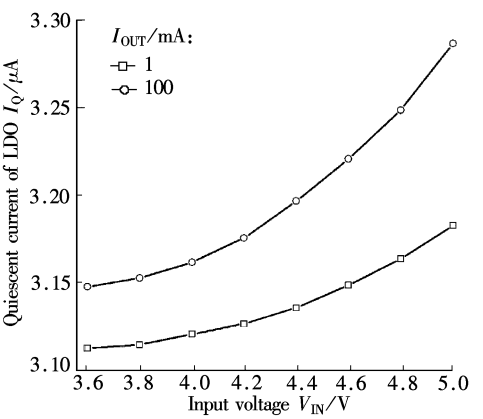

Fig. 11 The quiescent current of LDO during load and line regulation

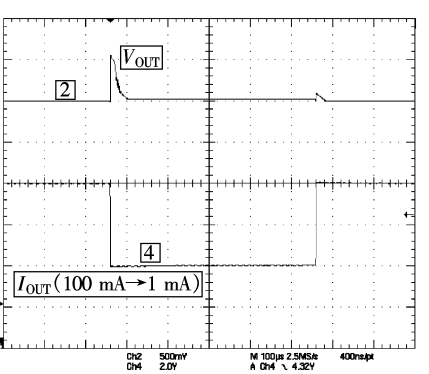

Fig. 12 The output voltage of LDO during load transient response

6 Conclusion

A CMOS LDO, which needs no off-chip capacitor, based on the architecture of a three-stage amplifier and NMC frequency compensation, is presented. In order to satisfy the low power requirement, a dynamic SRE circuit is used to reduce the overshot voltage and the settling time, and only 3.3 μA quiescent current is used in the proposed design. The behaviors of the SRE circuit and the Miller capacitor C_{m2}, theoretical analysis on the stability, and the experimental results are provided. The proposed LDO structure is ben-

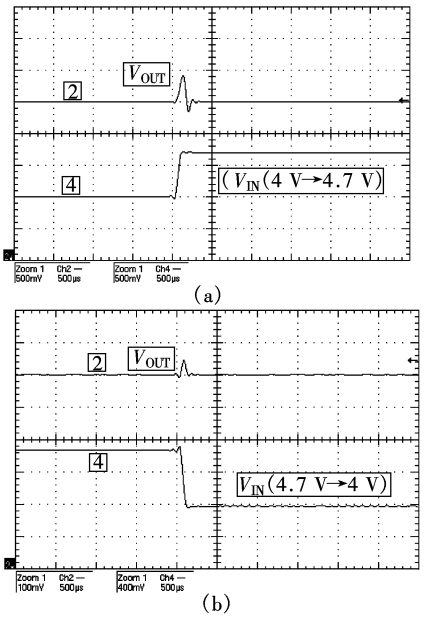

Fig. 13 The output voltage of LDO during line transient response. (a) V_{IN} changes from 4 to 4.7 V; (b) V_{IN} changes from 4.7 to 4 V

eficial for system-on-chip designs since it helps to eliminate many off-chip capacitors while preserving high static-state, frequency, and transient performances.

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3.3 μA 静态电流无片外电容的 CMOS 低压差线性稳压器

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摘要:设计了一种用于片上系统的无片外电容的 CMOS 低压差线性稳压器(LDO),其输出电压为 3.3 V,最大输出电流为 100 mA. 该设计可以有效地减少芯片引脚和电路板面积. 通过在传统结构上使用动态摆率增强电路和嵌套式米勒补偿技术,LDO 在线性和负载响应过程中都有很强的稳定性. 当输出电流从 100 mA 减小到 1 mA 时,过冲电压被限制在 550 mV 以内,稳定时间小于 50 μs. 由于采用了 30 nA 的电流基准,本设计的静态功耗仅为 3.3 μA. 通过 CSMC 公司 0.5 μm CMOS 工艺进行设计并流片验证,芯片测试结果与仿真结果吻合.

关键词:低压差线性稳压器;无片外电容;摆率增强电路;嵌套式米勒补偿

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