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Analysis and design of high linearity current reference for current mode circuits

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Abstract: A complementary metal-oxide-semiconductor transistor (CMOS) voltage-to-current (VTC) converter with high linearity for current-mode analog and digital integrated circuits is described. A high gain operational amplifier (OPA) is utilized to form negative feedback. A proportional to absolute temperature (PTAT) current reference with transistors operated in a weak inversion is used as the bias circuit. The resistor and the OPA nonlinearity behavior are analyzed in detail. By optimizing parameters in OPA and adopting a small voltage coefficient poly-silicon resistor as a linear device, a high linearity is achieved. The circuit is implemented in a standard 0.6 μm CMOS technology. The low frequency gain of the OPA exceeds 90 dB. The test results indicate that the total harmonic distortion (THD) is 0.000 2%. The common-mode input linearity range is 0 to 2.6 V. Correspondingly, the output current range is 50 to 426 μA. The sensitivity of the PTAT current reference to V_{dd} is approximately 0.021 7. The chip consumes a power of less than 1.3 mW for a 5 V supply, and occupies an area of 0.112 mm^2.

Key words: linear voltage-to-current converter; harmonic distortion; operational amplifier; PTAT current reference

Current-mode analog and digital integrated circuits are employed popularly in low-power and high-speed designs. The voltage-to-current converter serves an important function as the interface in current-mode mixed signal systems. The compact voltage-to-current converter is basic in realizing the high performance offered by the current-mode system.

Many researchers have proposed several approaches to improve the VTC linearity and linear range. An all-MOS VTC was proposed by Fotouhi[1], but the input and output linear range is limited mainly by the body effect factor, which is 0 to 1.8 V with ±0.5% nonlinearity for a 5 V supply. Chen and Hung used PMOS transistors to avoid the body effect and achieve a linear input range from 1.2 to 2.4 V with 1.5% THD for a 3.3V supply[2]. A flipped folded voltage follower was also applied in the VTC[3] to achieve a simulation THD of 0.005%.

These works above improved the linearity and linear range of the VTC. However, to achieve higher linearity, the nonlinearity factor in these circuits must be considered particularly. This paper presents a VTC architecture using a resistor, a PTAT current reference and a high gain OPA. Since the OPA and the resistor are the main sources to introduce nonlinearity distortion, the phasor method proposed by Hernes and Sansen in Ref. [4] is applied in the third harmonic analysis as a function of circuit parameters and input frequency.

1 Theoretical Analysis and Circuit Design

1.1 Nonlinearity analysis

As shown in Fig. 1, the input voltage is accurately followed by the voltage across R_1 because of the high gain of the OPA. Therefore, the current in M_5 equals the input voltage divided by R_1. This architecture has an accurate transfer shown as

$$I_o = \frac{1}{R_1}\left[\frac{1}{1+1/(g_{m5}A_v R_1)}\right]V_i \approx \frac{V_i}{R_1} \tag{1}$$

where g_{m5} is the transconductance of M_5 and A_v is the gain of the OPA.

To achieve a higher linearity, a poly-silicon resistor with a small voltage coefficient should be used as R_1 because poly-crystalline silicon does not exhibit the voltage modulation problems that plague most types of diffused and implanted resistors[5]. The resistor value is the function of the voltage as

$$G(v) = G_0[1 + V_{C1}\mathrm{d}v + V_{C2}(\mathrm{d}v)^2] \tag{2}$$

where G_0 is layout-dependent and calculated from sheet resistance. V_{C1} and V_{C2} are voltage coefficients. Therefore, V_{C1} is the main factor in introducing nonlinearity. The current i_g across R_1 can be expressed as

$$i_g = G_0 v + G_0 V_{C1} v^2 + G_0 V_{C2} v^3 \tag{3}$$

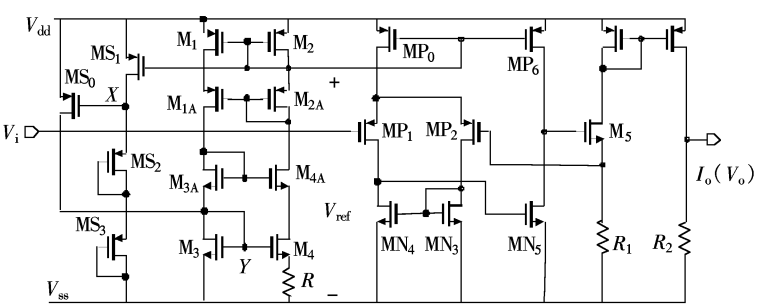

Fig. 1 Linear voltage-to-current converter

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When the input voltage is $V_m \cos(\omega t)$. The amplitudes of the fundamental frequency i_{g_1} and the second and the third harmonics are shown as follows:

$$\left.\begin{aligned} i_{g\_1} &= G_0 V_m + \frac{3}{4} G_0 V_{C2} V_m^3 + \cdots \\ i_{g\_2} &= \frac{1}{2} G_0 V_{C1} V_m^2 + \cdots \\ i_{g\_3} &= \frac{1}{4} G_0 V_{C2} V_m^3 + \cdots \end{aligned}\right\} \tag{4}$$

The second harmonic i_{g_2} depends on all the even order nonlinear coefficients, while the third harmonic i_{g_3} depends on all the odd order nonlinear coefficients.

As shown in Eq. (1), to achieve a high linearity, a high gain OPA with less nonlinearity is necessary. The strongest contribution to the third harmonic comes from the input differential pair MP_1 and MP_2, and the output transistors MN_5 and MP_6. $H_{3,\,P1/2}$ is the contribution to the third harmonic by MP_1 and MP_2,

$$H_{3,\,P1/2} \approx H_{3,\,0,\,P1/2} K_{2,\,2,\,0,\,0,\,P1}^2 \left(1 + \mathrm{j}\frac{\omega}{\omega_1}\right)^3 V_i^3 \tag{5}$$

The relationship between the nonlinear coefficients $K_{n,\,i,\,j,\,k}$ and the three-dimensional drain current i_d is given as

$$i_d = f(v_{gs}, v_{bs}, v_{ds}) = g_m v_{gs} + g_d v_{ds} + g_{mb} v_{bs} + \sum_{n=2}^{3} K_{n,\,i,\,j,\,k} v_{gs}^i v_{bs}^j v_{ds}^k \tag{6}$$

For example, $K_{2,\,2,\,0,\,0,\,P1}$ is the nonlinear coefficient, which is equal to $\mu_p C_{ox} W(1 + \lambda V_{ds})/(2L)$. ω_1 is the dominant pole. The low-frequency constant $H_{3,\,0,\,P1/2}$ is expressed as

$$H_{3,\,0,\,P1/2} = \frac{\frac{1}{8}\left(\frac{1}{g_{m,\,N2} R_1}\right)^3 \left(\frac{g_{m,\,N2} R_1}{g_{m,\,5} R_1 + 1}\right)}{g_{m,\,P1}(g_{ds,\,P0} + 2g_{m,\,P1} + 2g_{mb,\,P1} + 2g_{ds,\,P1})(A_1 A_2)^3} \tag{7}$$

where A_1 and A_2 are the gain of the first and the second stage of the OPA. The third harmonic equations for MN_5 are given by

$$H_{3,\,N5} \approx H_{3,\,0,\,N5/P6}\left(1 + \mathrm{j}\frac{3\omega}{\omega_{out1}}\right) \cdot \sum_{i=0}^{n=3} \frac{K_{3,\,i,\,0,\,(n-i),\,N5}}{(-A_2)^i}\left(1 + \mathrm{j}\frac{\omega}{\omega_{out}}\right)^i V_i^3 \tag{8}$$

The contribution to the third harmonic from MN_5 second order nonlinear coefficients is given by

$$H_3^{K_2,\,N5} \approx H_{3,\,0,\,N5/P6}\left(1 + \mathrm{j}\frac{3\omega}{\omega_{out1}}\right) \cdot \sum_{i=0}^{n=3} \alpha_i \frac{K_{2,\,2,\,0,\,0,\,N5}^{i-1} K_{2,\,1,\,0,\,1,\,N5}^{n-i}}{(-A_2)^i}\left(1 + \mathrm{j}\frac{\omega}{\omega_{out}}\right)^i V_i^3 \tag{9}$$

where $\alpha_{i=\{1,2,3\}} = \{1, 3, 2\}$. Eq. (10) describes the contribution from MP_6,

$$H_{3,\,P6} \approx H_{3,\,0,\,N5/P6}\left(1 + \mathrm{j}\frac{3\omega}{\omega_{out1}}\right) K_{3,\,0,\,0,\,3,\,P6} V_i^3 \tag{10}$$

where ω_{out1} and ω_{out} are the poles of the capacitances in the first and the second stage output nodes.

The low-frequency constant $H_{3,\,0,\,N5/P6}$ is expressed as

$$H_{3,\,0,\,N5/P6} = \frac{1}{32}\left(\frac{1}{g_{m,\,N5} R_1}\right)^3 \cdot \frac{1}{\left(A_1 A_2 \frac{g_{m,\,N5} R_1}{g_{m,\,N5} R_1 + 1}\right)(g_{ds,\,N5} + g_{ds,\,P6} + G_L)} \tag{11}$$

To obtain the OPA with low distortion, it is necessary to do the thorough analysis of the nonlinear behavior of the components. According to the third harmonic analysis in Eqs. (5) to (11), a low distortion OPA can be designed.

1.2 Current reference

The PTAT current reference shown in Fig. 1 is utilized to supply a stable bias to the operational amplifier. NMOS transistor M_3 and M_4 are in a weak inversion region. When $V_{ds,\,4} \gg V_T$, the drain current of M_4 is

$$I_4 = S_4 I_t \exp\left(\frac{V_{gs,\,4} - V_t}{n V_T}\right) \tag{12}$$

There is an exponential characteristic between the drain-source current and the gate-source voltage. Where S is the ratio of the channel width to the channel length, I_t is a parameter which depends on process specification, and V_t is the threshold voltage[6-7]. The thermal voltage $V_T (= kT/q)$ is 26 mV at room temperature. M_3 has the same exponential characteristic as M_4. PMOS transistors M_1 and M_2 act as a current mirror and are in a strong inversion region; therefore, the drain-source currents of M_1 and M_2 satisfy

$$I_1/I_2 = S_1/S_2 \tag{13}$$

With $I_1 = I_3$ and $I_2 = I_4$, using Eqs. (12) and (13), the voltage across R can be expressed as $V_T \ln(S_1 S_4/S_2 S_3)$.

The start-up circuit is required to drive the current reference circuit toward the desired stable state. When V_{dd} rises from 0 to 5 V, the voltage at the point X is 0 because the initial voltage across the capacitor is 0. Thus, PMOS MS_0 is on. This action causes a current to flow into M_3. The mirror effect in the current mirror circuit also causes the current to flow into M_4. Therefore the PTAT circuit starts to work. The diode-connected MS_2 and MS_3 operate as small-signal resistors. By selecting a proper size, the series resistor of MS_2 and MS_3 can be much larger than the drain-source resistor of MS_1. As a result, the voltage at the point X goes up to V_{dd}, and MS_0 is off. The start-up circuit does not affect the steady-state current values.

1.3 Operational amplifier

Fig. 1 illustrates the architecture of the two-stage operational amplifier. The small-signal model of this circuit is shown in Fig. 2. The gain of the first stage it is $-g_{m,\,P2}/(g_{ds,\,P1} + g_{ds,\,N3})$ and the second stage is $-g_{m,\,N5}/(g_{ds,\,P6} + g_{ds,\,N5})$, where g_m is the transconductance and g_{ds} is the channel conductance[8]. The PMOS transistor which has a small channel modulation effect is used as the input transistor to

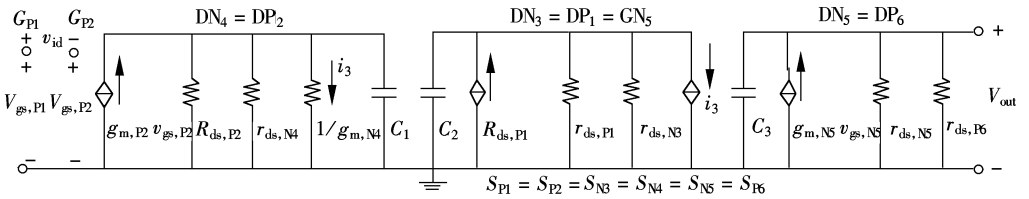


Fig. 2 Small-signal model of the OPA

achieve a large gain. As shown in Fig. 2, the OPA frequency response is mainly affected by C_1, C_2 and C_3. C_1 consists of $C_{db,P2}$, $C_{gs,N4}$, $C_{db,N4}$, and $C_{gs,N3}$. C_2 consists of $C_{db,N3}$ and $C_{gs,N5}$. C_3 consists of $C_{gd,P6}$, $C_{db,P6}$, $C_{db,N5}$ and C_L. When $g_{m,N4}/C_1 \gg (g_{ds,N3} + g_{ds,P1})/C_2$ is satisfied, the poles of the OPA are $(g_{ds,N5} + g_{ds,P6})/C_3$ and $(g_{ds,N3} + g_{ds,P1})/C_2$. As the drain-source currents of MP_6 and MN_5 are equal, to decrease the systematic offset voltage, the ratio W/L should satisfy

$$\frac{S_{N3}}{S_{N5}} = \frac{S_{N4}}{S_{N5}} = \frac{S_{P0}}{2S_{P6}} \tag{14}$$

According to Eq. (6), to lower the contribution to the third harmonic by MP_1, it is needed to reduce $K_{2,2,0,0,P1}$ and increase ω_1. Because $K_{2,2,0,0,P1}$ is equal to $\mu_p C_{ox} W(1 + \lambda V_{ds})/(2L)$, the parameters W/L and λ can be regulated to reduce $K_{2,2,0,0,P1}$. The PMOS is used as the input transistor for its small channel modulation effect to reduce nonlinear distortion and acquire high gain. But high gain leads to low bandwidth, so there is a tradeoff between them.

2 Simulation and Optimization

The circuit is realized in CSMC 0.6 μm CMOS technology. Fig. 3(a) gives the curve of bias voltages when the PTAT current reference starts up. At first, the supply voltage is 0, and all the node voltages are 0. When the supply voltage steps from 0 to 5 V within 1 μs rise time, the circuit state can be observed. As seen from the curve, during the period from 1 to 1.5 μs, the voltage V_X increases slowly to 500 mV. So the voltage difference between V_{dd} and V_X is large enough to turn MS_0 on. Then the current flows into M_3 through MS_0 and V_Y is pulled up gradually to approximately 2 V. Subsequently, V_X rises rapidly to 5 V, and MS_0 is off. Finally, the start-up circuit is disconnected. These results are consistent with the previous theoretical analyses. The voltage of the output signal bias observed in post-layout simulation is 3.848 V. The results indicate that there are parasitic elements which cause an 18 mV voltage drop compared with 3.866 V in pre-layout simulation.

Fig. 3(b) shows the OPA voltage gain as a function of frequency. The estimate curve is deduced according to the model in Fig. 2. The gain of the first stage is 43.8 dB, and the second stage is 46.2 dB. So the gain of the two-stage OPA is 90 dB. As C_1 is 60.299 4 fF, C_2 is 30.71 fF, and C_3 is approximately equal to the load capacitor C_L which is 10 pF. The frequency of the dominant pole is 2.07 kHz, and the second pole is 683 kHz. Therefore, the estimate curve agrees with the simulation curve in Fig. 3(b).

In Fig. 1, a larger R_1 can also contribute a small increment

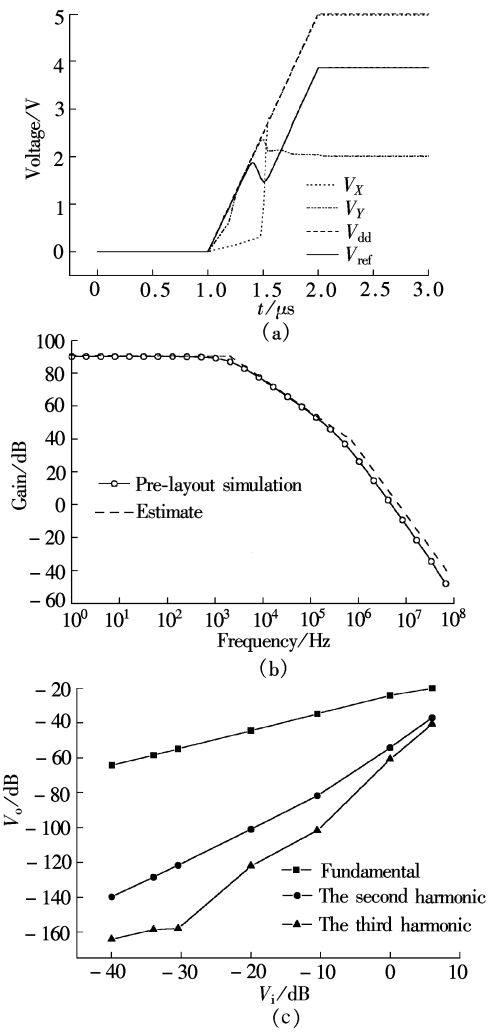


Fig. 3 Simulation results. (a) Start-up curve of the PTAT current reference; (b) Gain curve of the OPA; (c) Harmonic distortion of the output voltage as a function of input voltage amplitude

to the linear range. R_2 is added to the architecture for test convenience because the voltage signal is easier to test than the current signal. R_2 does not affect the linearity range of the output current. In this design, R_1 is 10 kΩ, and R_2 is 500 Ω.

The harmonic distortion as a function of the amplitude of the input voltage is shown in Fig. 3(c). The post-layout simulated data consisting of the fundamental frequency, the second harmonic, and the third harmonic are shown in Fig. 3(c).

3 Measurement

The chip photomicrograph is shown in Fig. 4, which occupies 0.112 mm^2. Fig. 5 shows the measured performance of the PTAT current reference. It can be seen from Fig. 5 (a) that the bias has taken 6.66 ms to rise from 0 to 3.766

V at start-up. As the bias is applied to the gate of the PMOS, the voltage difference between V_{dd} and V_{ref} should not be sensitive to V_{dd}. The measured amplitude of $V_{dd} - V_{ref}$ is shown in Fig. 5(b). The sensitivity of the current reference to V_{dd} can be calculated by

$$S_{V_{dd}}^{V_{dd}-V_{ref}} = \frac{\partial(V_{dd} - V_{ref})/(V_{dd} - V_{ref})}{\partial(V_{dd})/V_{dd}} \quad (15)$$

Unlike the sensitivity in the pre-layout and post-layout simulation being 0, the test result is 0.021 7.

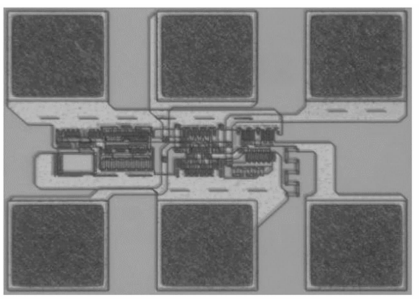
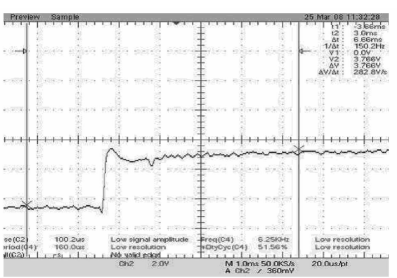
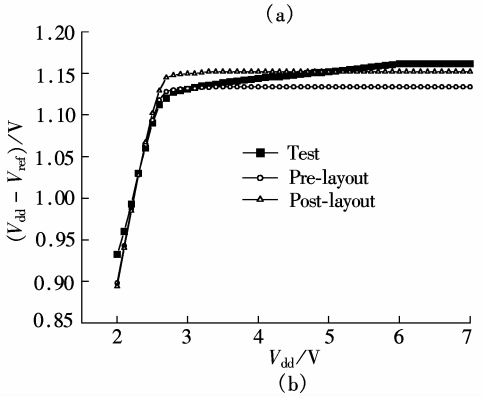


Fig. 4 The chip photomicrograph



(a)



(b)

Fig. 5 The measured result of the current reference. (a) Start-up curve of the current reference; (b) The measured V_{ref} as a function of the V_{dd}

Fig. 6(a) shows the transfer curve of I_o vs. V_i. The output voltage V_o is measured as a function of the input voltage V_i, and divided by R_2 to obtain the output current I_o. The input linearity range is from 0 to 3.3 V in the simulation, whereas it is 0 to 2.6 V in the measurement. The linear range is not rail-to-rail since the PMOS is utilized as the input transistor in the OPA. When the input voltage increases to 3.3 V, MP_1 does not have enough gate-source voltage to turn on, then the OPA will not work in the amplification region. Consequently, the converter is out of the linear region. The linear output current range is from 50 to 426 μA. Due to the mismatch between differential transistors in the OPA during the fabrication, there is a 50 μA offset between the simulation and the measurement results. Fig. 6(b) shows the derivative of the measured I_o, which shows a better view of the linearity achieved by the proposed schematic. The results show a THD 0.000 2%. In Tab. 1, a nonlinearity contrast with the reference is done.

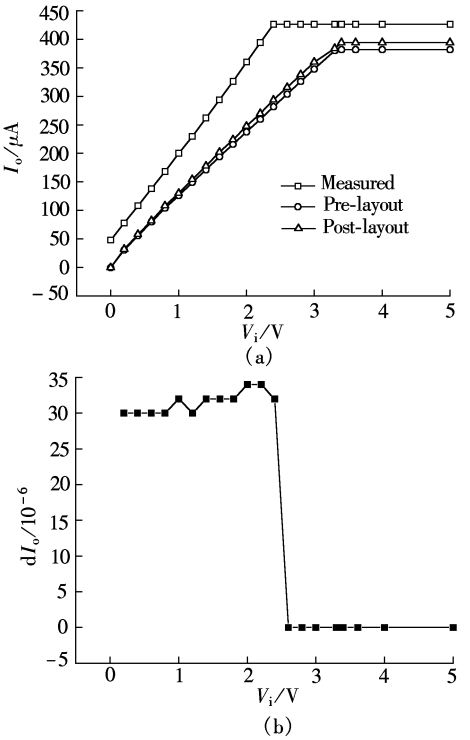


Fig. 6 Test results. (a) The output current I_o vs. the input voltage V_i; (b) Derivative of the measured I_o

Tab. 1 The nonlinearity of the VTC

Power/V	Linear range/V	Nonlinearity(THD)/%	References
5	0 to 1.8	±0.5	Ref. [1]
3.3	1.2 to 2.4	1.5	Ref. [2]
		0.000 5(simulation)	Ref. [3]
5	0 to 2.6	0.000 2	This paper

4 Conclusion

In this paper, a high linearity voltage-to-current converter is designed and implemented in CSMC 0.6 μm CMOS technology. The resistor and the OPA nonlinearity behavior are analyzed. The use of a poly-silicon resistor as a linear device with a low voltage coefficient introduces little additional nonlinearity and achieves a high linearity between output and input. The output current has a comparatively high linearity. The high-gain operational amplifier and the PTAT current reference are utilized to assure the circuit stability and performance.

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电流模逻辑电路中高线性度电流参考源的分析与设计

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摘要:描述了应用于电流模逻辑电路中的高线性度电压-电流转换电路的设计与实现. 该电路采用高增益两级运算放大器构成负反馈,偏置电路利用工作在弱反型区的 MOS 管电压电流呈指数律关系构成 PTAT(proportional to absolute temperature)基准电流源. 详细分析了电阻的类型以及运算放大器的参数对线性度的影响. 通过优化运算放大器的参数并采用电压系数较小的多晶硅电阻作为线性器件获得了较高的线性度. 本电路已采用 CSMC 0.6 μm CMOS 工艺实现,测试结果表明:输出的总谐波失真为 0.000 2%. 输入动态范围为 0 ~ 2.6 V,输出电流为 50 ~ 426 μA. PTAT 基准电流源对电源变化的灵敏度为 0.021 7. 芯片采用 5 V 供电,功耗约为 1.3 mW,芯片面积为 0.112 mm^2.

关键词:线性电压电流转换电路;谐波失真;运算放大器;PTAT 基准电流源
中图分类号:TN432