

High performance differential CMOS LNA design for low-IF GPS receiver

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Abstract: A 1.575 GHz CMOS (complementary metal-oxide-semiconductor) low noise amplifier (LNA) suitable for a low intermediate frequency (IF) global positioning system (GPS) receiver is presented. Considering parasitic effects resulting from bond pad and input electrostatic discharge (ESD) protection diodes, the optimization of the input matching and noise performance is analyzed, and a narrowband inductor model is applied to the circuit design and optimization. Based on the Volterra series, the nonlinearity of the LNA is analyzed and an equation describing input-referred third-order intercept points (I_{IP3}) which indicate the nonlinearity effects is derived; accordingly, the trade-off between the power consumption and linearity is made. The LNA is designed and simulated with TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm radio frequency (RF) technology. Simulation results show that the LNA has a noise figure of only 1.1 dB, -8.3 dBm I_{IP3} with 3 mA current consumption from a 1.8 V voltage supply, and the input impedances match well.

Key words: low noise amplifier (LNA); nonlinearity; electrostatic discharge (ESD) protection diode

Due to the continuous growth in the market for global positioning system (GPS) receivers, the design and analysis of GPS radio-frequency (RF) integrated circuits are receiving much attention from research communities. Traditionally, GPS RF integrated circuits are mostly implemented in bipolar or GaAs technologies and cannot be integrated with digital CMOS baseband modules in a single chip. Thus, there are strong requirements for low cost, low power consumption and highly integrated solutions. Owing to improved performance in CMOS technology, CMOS implementation for GPS RF front-end is becoming more and more popular and competitive.

As a key component in the RF front-end, the CMOS low noise amplifier (LNA) plays a critical role in determining the performance of GPS receivers. The GPS RF signals coming from the antenna are amplified by an LNA which precedes a filter or a mixer. For civil GPS, the received GPS signal (C/A code) power at the antenna is about -130 dBm^[1] which spreads over a 2 MHz bandwidth centered at 1.575 GHz. While in the 2 MHz main lobe of the C/A code, the thermal noise power is about -111 dBm, so the LNA must provide reasonable power gain to amplify the weak GPS signal and simultaneously have a very low noise

figure (NF) to meet the demands of the receiver sensitivity.

Many discussions on input matching and noise performance of the CMOS LNA are presented^[2-4]. Ref. [2] discussed four different input matching methodologies and the impact on the noise figure of the CMOS LNA. Ref. [3] presented a noise optimization with considerations for the induced gate noise and the loss of the gate inductor. However, the literature mentioned above did not consider the parasitic effects of the input bond pad. In practice, the parasitic effects of the bond pad and input electrostatic discharge (ESD) protection devices often limit the performance of the LNA, so they must be taken into account in the design procedure. On the other hand, the linearity of the LNA is important for GPS receivers, while the nonlinearity of the CMOS LNA produces the intermodulation distortion which can corrupt the desired signal down-converted by a mixer. Thus, the nonlinearity analysis of the CMOS LNA is necessary in the design. Based on the Volterra series, an equation describing IIP_3 which indicates the nonlinearity effects is derived in this paper. Based on the derived equation, relationships between the nonlinearity effects and the parameters of the circuit are revealed explicitly.

1 CMOS LNA Input Matching and Noise Analysis

The commonly used cascode architecture with inductive degeneration is chosen in this paper, which provides good reverse isolation between the input and output stages and superior noise performance. The cascode architecture including the parasitic effects of the bond pad and ESD protection devices is shown in Fig. 1.

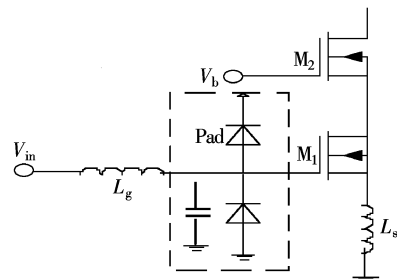


Fig. 1 The cascode structure with pad

The input stage small-signal circuit of the LNA is shown in Fig. 2. The capacitance C_p represents the contribution of the parasitic capacitance due to the RF pad and the parasitic capacitances due to ESD diodes. Using the circuit shown in Fig. 2, the input impedance is approximated as

$$Z_{in} \approx sL_g + \frac{1}{s(C_p + C_{gs})} + \left(\frac{C_{gs}}{C_{gs} + C_p} \right)^2 \frac{g_m}{C_{gs}} L_s \quad (1)$$

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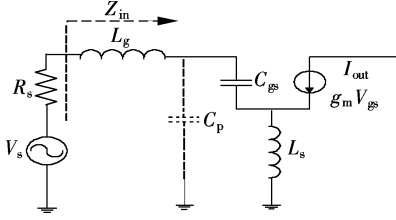


Fig. 2 Small-signal circuit for Z_{in} calculation

where g_m and C_{gs} are the transconductances of transistor M_1 and the gate-source capacitance, respectively. For conjugate matching in the LNA input we can obtain

$$\left(\frac{C_{gs}}{C_{gs} + C_p} \right)^2 \frac{g_m}{C_{gs}} L_s = R_s \quad (2)$$

$$sL_g + \frac{1}{s(C_p + C_{gs})} = 0 \quad (3)$$

The corresponding resonance angular frequency ω_0 is determined by

$$\omega_0 = \frac{1}{\sqrt{L_g (C_p + C_{gs})}} \quad (4)$$

The noise figure of the cascaded LNA can be computed by analyzing the small-signal circuit shown in Fig. 3.

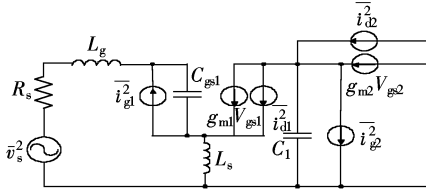


Fig. 3 Small-signal circuit for the cascaded LNA noise calculations

In Fig. 3, \bar{i}_g^2 and \bar{i}_d^2 represent the mean-squared gate-induced noise current and the channel thermal noise current, respectively. They are given by

$$\bar{i}_g^2 = 4kT\Delta f \delta g_g, \quad \delta g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (5)$$

$$\bar{i}_d^2 = 4kT\Delta f \gamma g_{d0} \quad (6)$$

where k is the Boltzmann constant, T is the absolute temperature, and Δf is the bandwidth. The gate-induced noise is partially correlated with the channel noise, and the correlation coefficient is given by

$$c = \frac{\bar{i}_g^* \bar{i}_d}{\sqrt{\bar{i}_g^2 \bar{i}_d^2}} \quad (7)$$

Without considering the parasitic effects, the noise figure of the cascaded LNA is given by^[5]

$$F = 1 + \gamma_1 g_{d01} R_s \left(\frac{\omega_0}{\omega_T} \right)^2 \left[1 + \left(\frac{\omega_0 C_1}{g_{m2}} \right)^2 \left(\frac{\gamma_2 g_{d02}}{\gamma_1 g_{d01}} \right) \left(1 + \frac{\omega_T L_s}{R_s} \right)^2 \right] \quad (8)$$

The parameter g_{d0} is the zero-bias drain conductance, γ is a bias-dependent thermal noise factor, and C_1 is the total ca-

pacitance at the drain of M_1 . From Eq. (8), the noise contribution of M_2 can be obtained as

$$F_{M2} \approx F_{M1} \left(1 + \frac{\omega_T L_s}{R_s} \right)^2 \left(\frac{\omega_0}{\omega_T} \right)^2 \quad (9)$$

where F_{M1} is the noise contribution of M_1 . In practice, $(\omega_0/\omega_T)^2 \ll 1$, the noise contribution of M_2 can be ignored here. Just considering the parasitic effect and the input stage, the noise figure of the LNA is recalculated as follows^[5-6]:

$$F \approx 1 + \frac{\gamma}{\alpha} \frac{1}{k^2 Q} \frac{\omega_0}{\omega_T} + 2 \frac{|c|}{k^2 Q} \sqrt{\frac{\delta \gamma \omega_0}{5 \omega_T}} + \frac{(k^4 Q + 1) \delta \alpha}{5 k^2 Q} \frac{\omega_0}{\omega_T} \quad (10)$$

where $k = C_{gs}/(C_{gs} + C_p)$; Q is the quality factor of the input matching network. Compared to the conventional analysis without the parasitic effects, from Eqs. (2) and (4), it can be seen that the input impedance of the LNA is decreased by a factor of $2(C_{gs}/(C_{gs} + C_p))$ due to the parasitic capacitance C_p . Also, the gate inductance is required to be smaller in order to resonate at the working frequency. Due to the parasitic effects, the noise performance of the LNA degenerates. So the dimensions of the input and output ESD protection circuits must be very small to significantly reduce the parasitic capacitances. The number of gate fingers is selected to minimize the noise contribution of the gate resistances. Fig. 4 shows the LNA NF as a function of the gate fingers. The NF reaches the minimum while the gate fingers number equals 48 and gate width per finger equals $2.5 \mu\text{m}$. The size of M_2 is selected as equal as the size of M_1 ; this can reduce the junction capacitance and improve the noise figure.

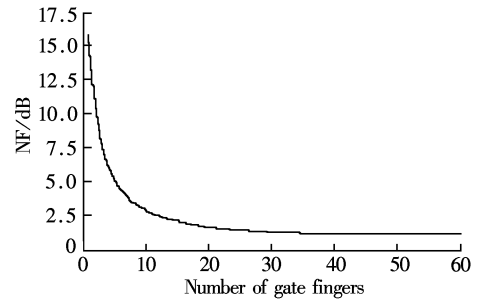


Fig. 4 NF as a function of the number of gate fingers

Besides active devices, the passive inductors will also degrade the noise performance of the LNA to some extent. By improving the quality factor of the inductor, the noise performance can be improved. Due to the parasitic effects, the RF spiral inductor model has to be included in the simulation procedure. The RF spiral inductor model is illustrated in Fig. 5.

The inductance and resistance of the spiral inductor are represented by the series inductance L_s and the series resistance R_s , respectively. C_p is the parasitic capacitance between the inter-wires. The other elements represent the losses due to the substrate effects. The spiral inductor is designed to have a small chip area and a large quality factor. The quality factor is calculated as

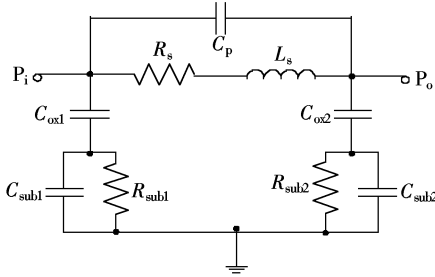


Fig. 5 Lumped physical model for on-chip spiral inductor

$$Q = \frac{\omega L_s}{R_s} \frac{R_p}{R_p + [(\omega L_s / R_s)^2 + 1] R_s} \cdot \left[1 - (C_p + C_s) \left(\omega^2 L_s + \frac{R_s^2}{L_s} \right) \right] \quad (11)$$

Compared to square spiral inductors, octagonal inductors give a better quality factor and they are adopted in our design. In order to yield an optimum inductor, the inductor layout parameters such as the number of turns, metal width, inner diameter and spacing need to be adjusted. To reduce the series resistance of the spiral inductor, the highest metal layer should be used. The metal width is around 6 μm at 1.575 GHz, and the spacing between metal segments is selected as 2 μm as minimum spacing results in maximized magnetic coupling.

2 CMOS LNA Nonlinearity Analysis

In RF receivers, the third-order interception point and the second-order interception point are the two most important performance metrics for indicating the nonlinearity effects. The second-order nonlinearity of the LNA will generate an unwanted DC signal or a low frequency signal. For a zero IF receiver, the desired signal is directly down-converted to baseband. So the separation of the desired signal from the unwanted DC signal or a low frequency signal due to the second-order nonlinearity becomes troublesome. Since the structure of the GPS receiver used in our design is a low IF, our analysis mainly focuses on the third-order nonlinearity of the LNA. Based on the theory of Volterra's series^[7-11], we analyze the nonlinearity of the input stage of the LNA, and I_{IP3} is derived as follows.

In the first step, we calculate the first-order kernels. The circuit used for the first-order kernel analysis is shown in Fig. 6.

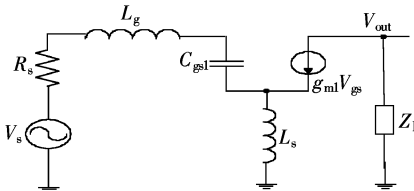


Fig. 6 Small-signal equivalent circuit for the first-order kernel calculation

Nodal analysis in Fig. 6 yields the results which can be represented by

$$\begin{bmatrix} R_s + s(L_s + L_g) + \frac{1}{sC_{gs1}} + \frac{g_{m1}L_s}{C_{gs1}} & 0 \\ g_{m1}z_L & 1 \end{bmatrix} \begin{Bmatrix} H_{1gs1}(s) \\ H_{1out}(s) \end{Bmatrix} = \begin{Bmatrix} \frac{1}{sC_{gs1}} \\ 0 \end{Bmatrix} \quad (12)$$

where $H_{mgs1}(s)$ and $H_{mout}(s)$ ($m = 1, 2, \dots$) are the m -th-order kernels of the gate-source voltage and the output voltage in the frequency domain, respectively.

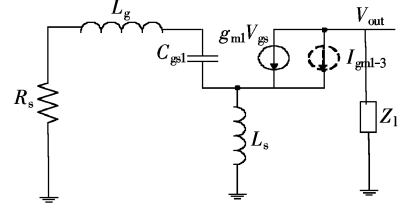


Fig. 7 Small-signal circuit for the third-order kernel calculation

In order to obtain the third-order kernel, the circuit in Fig. 6 with the third nonlinear current source i_{gm1-3} is placed in parallel with the nonlinear elements, and the linear input is shortened. Simultaneously, the frequency variable s is replaced by $s_1 + s_2 + s_3$. The circuit used for the third-order kernel analysis is shown in Fig. 7. The nodal analysis in Fig. 7 yields the following matrix equation:

$$\begin{bmatrix} R_s + (s_1 + s_2 + s_3)(L_s + L_g) + \frac{1}{(s_1 + s_2 + s_3)C_{gs1}} + \frac{g_{m1}L_s}{C_{gs1}} & 0 \\ g_{m1}z_L & 1 \end{bmatrix} \begin{Bmatrix} H_{3gs1}(s_1, s_2, s_3) \\ H_{3out}(s_1, s_2, s_3) \end{Bmatrix} = \begin{Bmatrix} -\frac{i_{gm1-3}L_s}{C_{gs1}} \\ -i_{gm1-3}z_L \end{Bmatrix} \quad (13)$$

The value of the third-order nonlinear current source i_{gm1-3} is given by^[11]

$$i_{gm1-3} = K_{3gs1} H_{1gs1}(s_1) H_{1gs1}(s_2) H_{1gs1}(s_3) + \frac{2}{3} K_{2gs1} [H_{1gs1}(s_1) \cdot H_{2gs1}(s_2, s_3) + H_{1gs1}(s_2) H_{2gs1}(s_1, s_3) + H_{1gs1}(s_3) \cdot H_{2gs1}(s_1, s_2)] \approx K_{3gs1} H_{1gs1}(s_1) H_{1gs1}(s_2) H_{1gs1}(s_3) \quad (14)$$

where K_{mgs1} ($m = 1, 2, 3, \dots$) is the m -th-order coefficient in the Taylor expression of the drain current of the MOS transistor.

In the saturation region, the drain current of the MOS transistor is

$$I_d = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} \frac{V_{od}^2}{1 + V_{od}/(LE_{sat})} \quad (15)$$

where C_{ox} is the gate oxide capacitance per unit area; W and L are the width and the length of the channel, respectively; V_{od} is the over-drive voltage of the transistor and equal to $V_{GS} - V_{th}$.

I_{IP3} is defined as^[11]

$$I_{IP3} = \frac{2}{\sqrt{3}} \sqrt{\frac{|H_{1out}(j\omega_1)|}{|H_{3out}(-j\omega_1, j\omega_1, j\omega_1)|}} \quad (16)$$

Using Eqs. (12) to (16), we can obtain

$$I_{IP3} \approx 3L_s \omega_0 \mu_0 C_{gs1} \frac{1}{L^2} \sqrt{\frac{2V_{od}^3(2 + \theta V_{od})^3}{3\theta(1 + \theta V_{od})^2}} \quad (17)$$

where $\theta = 1/(E_{sat}L)$ is the mobility modulation factor.

From Eq. (17), it can be seen that using multiple-finger transistors can improve I_{IP3} . This is because the decrease in gate resistance denotes the increase in L_s for input matching; accordingly, I_{IP3} is increased. I_{IP3} can also be improved by increasing V_{od} , but simultaneously, the power consumption is also increased, so the performance trade-off between them is needed in the design procedure.

3 Simulation Results

The CMOS LNA designed in this paper is a differential one with the cascode configuration analyzed above. This is because the fully differential design is the best way to reject power supply noise and the unwanted signals coupling from the substrate. The schematic of the LNA is shown in Fig. 8.

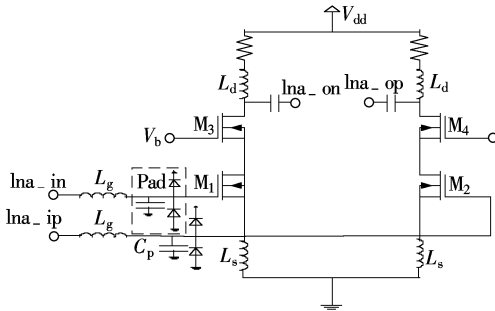


Fig. 8 Simplified circuit of the LNA

In order to minimize the junction capacitance, the cascode transistors can be laid out as a dual-gate transistor for the same W and L . Besides, the layout should be made symmetrical as far as possible in order to alleviate the mismatch and even-order nonlinearity. The octagonal signal pads are adopted and they should be implemented using the top metal layer. Thus, the impact of the parasitic capacitance can be reduced to a great extent.

The LNA circuit is simulated using Cadence SpectreRF simulator in TSMC 0.18 μm 1P6M CMOS technology. The simulated S -parameters of the LNA are shown in Fig. 9 and Fig. 10. The input return loss (S_{11}) of the LNA is equal to -16.31 dB at 1.575 GHz. This shows that the LNA exhibits good input matching at the operating frequency. The LNA achieves a peak gain (S_{21}) of 14.8 dB. After noise optimization, a low noise figure (NF) of 1.1 dB at 1.575 GHz is achieved and shown in Fig. 11. The I_{IP3} simulation result of the LNA is shown in Fig. 12. A two-tone signal has been applied to the input of the LNA at the frequencies of 1.575 GHz and 1.580 GHz. The input-referred third-order intercept point (IIP3) is -8.3 dBm. A comparison of the designed LNA and some recent reported LNA used in GPS receivers are listed in Tab. 1.

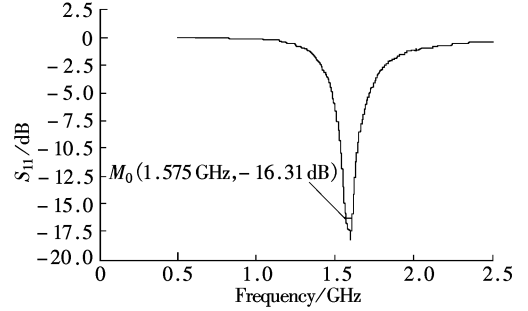


Fig. 9 Simulated S_{11}

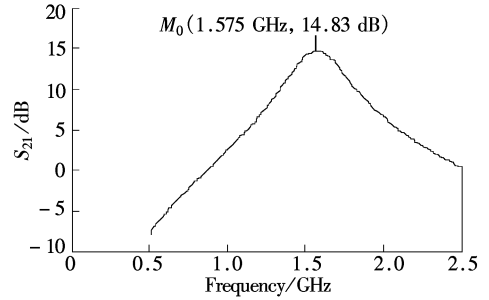


Fig. 10 Simulated S_{21}

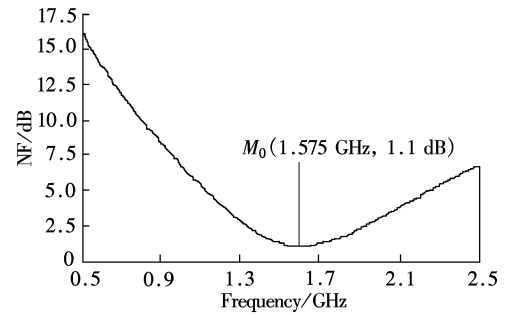


Fig. 11 Simulated noise figure

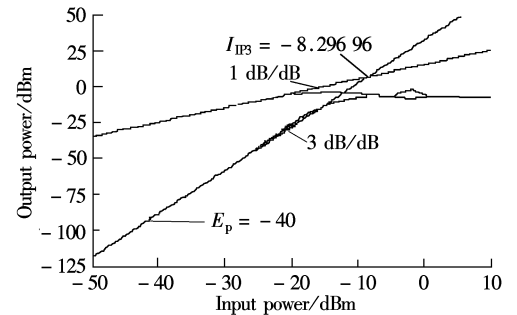


Fig. 12 Simulated I_{IP3}

Tab. 1 Performance comparison of recently published LNA for GPS

intercept point (IP3) is -8.5 dBm. A comparison of the designed LNA and some recent reported LNA used in GPS receivers are listed in Tab. 1.			Center frequency/GHz	Supply voltage/V	Current consumption/mA	S_{11} /dB	S_{12} /dB	S_{21} /dB	NF/dB	I_{IP3}
			This paper	1.575	1.8	3	-16.3	-36.8	14.83	1.1
2.8	5		26	3.6	-3	0.35 μm CMOS				
1.5	4	-23	32	1.5	-6.8	0.18 μm CMOS				
1.8	3.49	-15.7	14.8	2.6		0.18 μm BiCMOS				

4 Conclusion

The analysis and design of the CMOS LNA for the low-IF GPS receiver are presented based on TSMC 0.18 μm CMOS RF technology. Discussions of parasitic effects re-

sulting from bond pad and ESD protection diodes for LNA design are given. Based on the Volterra series, the nonlinearity analysis of the LNA is carried out and equation IIP3 is derived. SpectreRF simulation shows that the LNA achieves the following specifications: 1.1 dB noise figure,

14. 8 dB gain, -8.3 dBm IIP3 with 3 mA current consumption from a 1.8 V voltage supply.

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用于低中频 GPS 接收机的高性能 CMOS 差分低噪声放大器设计

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摘要:设计了一个可用于低中频 GPS 接收机系统的 1.575 GHz 的低噪声放大器. 首先考虑了 ESD 保护二极管和焊盘的寄生效应, 对输入匹配和噪声性能的优化做了分析, 并将窄带电感模型用于电路设计优化. 其次基于 Volterra 级数, 对放大器的非线性做了分析, 推导了电路各参数与 I_{IP3} 的关系表达式, 据此在功耗和线性度之间做了折衷考虑. 采用 TSMC 0.18 μm 射频工艺对低噪声放大器进行设计和仿真. 仿真结果表明: 在 1.8 V 工作电压下, 噪声系数仅为 1.1 dB, I_{IP3} 为 -8.3 dBm, 电流消耗 3 mA, 电路的输入匹配良好.

关键词:低噪声放大器; 非线性; ESD 保护二极管

中图分类号: TN722