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Neuronal signal detecting and stimulating circuit array for monolithic integrated MEA

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Abstract: A neuronal signal detecting circuit and a neuronal signal stimulating circuit designed for a monolithic integrated MEA(micro-electrode array) system are described. As a basic cell of the circuits, an OPA(operational amplifier) is designed with low power, low noise, small size and high gain. The detecting circuit has a chip area of 290 μm × 400 μm, a power dissipation of 2.02 mW, an equivalent input noise of 17.72 nV/Hz, a gain of 60.5 dB, and an output voltage from −2.48 to +2.5 V. The stimulating circuit has a chip area of 130 μm × 290 μm, a power dissipation of 740 μW, and an output voltage from −2.5 to 2.04 V. The parameters show that two circuits are suitable for a monolithic integrated MEA system. The detecting circuit and MEA have been fabricated. The test results show that the detecting circuit works well.

Key words: neuronal signal; detecting; noise; micro-electrode array (MEA); complementary metal-oxide-semiconductor transistor (CMOS) technology

With the rapid development of the semiconductor, microelectronics has been applied more and more in the study of life science. In the macroscopic studies of neural signals, our research group has been researching a nerve signal regeneration system in recent years.

The microscopic study of neuronal populations is a key point in cognitive science[1-2]. In such kinds of studies, different MEAs(micro-electrode-array) are widely used[3-4]. An MEA is generally realized by using a semiconductor technology because of its advantages of high density and high precision. To contact neurons cultivated on the MEA chip with the outside environment, metallic electrodes are used. The electrodes should be made by using the top metal for the consideration of neuron growth. Compared with hybrid MEA systems, the advantages of the monolithic integrated MEA system include small size and lower interference.

At present, several types of integrated MEA systems have been reported. Most of them are fabricated on silicon for their low cost and easy integration. Such a system contains a surface MEA, many channels of low-noise amplifiers, low-pass filters, ADCs and so on[5-6].

Considering the cultivation of neuronal cells, the temperature should be kept constant and the heating of the semiconductor must be low. Thus, the circuit used in a monolithic MEA system must be of low power. The neuronal signal detection is in a strong noise environment. So the detecting load or detecting circuit must offer a high SNR(signal-to-noise ratio) with low noise. On the other hand, the microscopic study of the neuronal population needs a large-scale MEA. So multi-channels for detecting loads and stimulating loads are needed. The layout of each circuit is very important.

In addition, the circuit for a monolithic MEA system must be of low power, high SNR and small chip size. Thus, the circuit should be specially designed. In consideration of large-scale fabrication, a monolithic integrated MEA system must be realized in a standard Si technology.

In this paper, a neuronal signal detecting circuit and stimulating circuit are designed in a standard 0.5 μm CMOS process(CSMC, Wuxi, China). In the following sections, the system architectures, the circuit techniques, the simulation results, the layout designs of two circuits and the test results of the detecting circuit will be discussed.

1 System Architecture

The monolithic integrated MEA system consists of a surface MEA, a column of detecting circuits, and a row of stimulating circuits. A neuron assembly is expected to grow on the chip surface. So, a neuronal network can be formed by synaptic joints. An electrode can detect the neuronal signal from one or more neurons. The contents concerning the acquisition method of detecting signals and the stimulation method are not discussed in this paper. Here only the detecting and stimulating circuits are discussed.

1.1 Detecting circuit

The detecting circuit consists of a three-stage OPAs(operational amplifier), as shown in Fig. 1. The first two stages are configured as an in-phase amplifier and the third stage is a voltage follower. As usual, the OPA is designed with differential input and single-ended output. Since bioelectrical signals are bipolar against the ground, the OPA is supplied with voltages of ±2.5 V and a central level at 0 V. Therefore, both the positive and the negative neuronal signals can be amplified by the detecting and stimulating circuits.

One input terminal of each detecting circuit is connected to one electrode. Thus, the detecting circuit has a single-

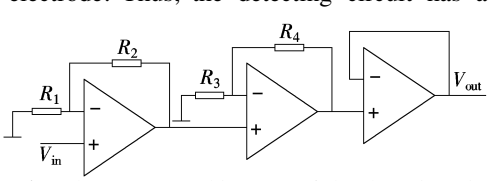

Fig. 1 The system architecture of the detecting circuit

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ended input and the reference potential is the ground. The neurons cultivated on the MEA are the source of bioelectrical signals. As a neuronal signal source, it is of high resistance and the signal is weak. Thus, the input stage of the detecting circuit is designed as an in-phase amplifier, and the input terminal is connected to the gate of an MOS transistor whose input-resistance is in the magnitude of $10^{20}\,\Omega$.

In order to realize a small size, three OPA stages are adopted for the detecting circuit. Therefore, the second stage is also designed as an in-phase amplifier. The total small-signal gain is

$$A_{\mathrm{V}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{R_1 + R_2}{R_1}\,\frac{R_3 + R_4}{R_3} \tag{1}$$

As shown in Fig. 2, each stage of the cascaded system has a gain G and a noise factor F. The total noise factor F_{total} is[7]

$$F_{\mathrm{total}} = F_1 + \frac{F_2 - 1}{G_{\mathrm{A1}}} + \frac{F_3 - 1}{G_{\mathrm{A1}} G_{\mathrm{A2}}} \tag{2}$$

Eq. (2) suggests that the noise factor F_1 and G_{A1} of the first-stage play an important role in a cascaded system.

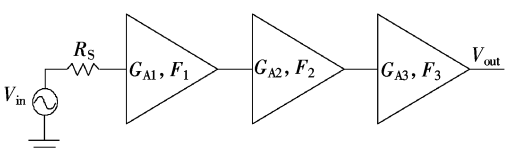


Fig. 2 A three-stage system with noise factor

1.2 Stimulating circuit

In order to effectively stimulate neurons on a chip surface, the output resistance of the stimulating circuit must be low. As shown in Fig. 3, the stimulating circuit is in fact a voltage follower or a unity gain buffer with an output resistance of several tens of ohms. The OPA used in the stimulating circuit is identical with that in the detecting circuit. The signal is applied to the in-phase input and the reverse-phase input is directly connected to the output, $V_{\mathrm{out}} = V_{\mathrm{in}}$.

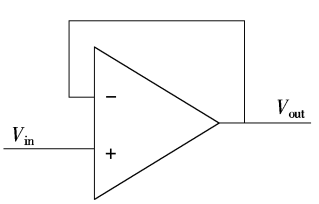


Fig. 3 The system architeture of the stimulating circuit

2 Circuit Techniques

From Fig. 1 it is known that the basic cell of both the detecting circuit and the stimulating circuit is an OPA. Therefore, the key point of the circuit design is the design of a high-performance OPA.

The OPA we designed consists of three parts: the amplifying sub-circuit, the biasing sub-circuit and the startup sub-circuit.

Fig. 4 shows the circuit schematic of the amplifying sub-circuit. Since the amplifying sub-circuit is the core part of the OPA, it will be discussed in detail. According to the cascade noise formula, as shown in Eq. (2), the noise of the first-stage differential input transistors is critical for the system. In our design, PMOS transistors are adopted as input pairs since their noise coefficients are lower than those of their NMOS counterparts.

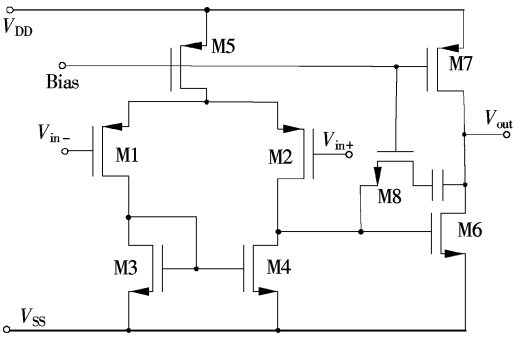


Fig. 4 The circuit schematic of the amplifying sub-circuit

Fig. 5 shows the input stage including noise sources. The equivalent input noise introduced by the input pair can be deduced[8−12]. The noise spectral density of the input pair is

$$e_{\mathrm{eq}}^2 = 2e_{\mathrm{n1}}^2\left[1 + \left(\frac{g_{\mathrm{m3}}}{g_{\mathrm{m1}}}\right)^2\left(\frac{e_{\mathrm{n3}}^2}{e_{\mathrm{n1}}^2}\right)\right] \tag{3}$$

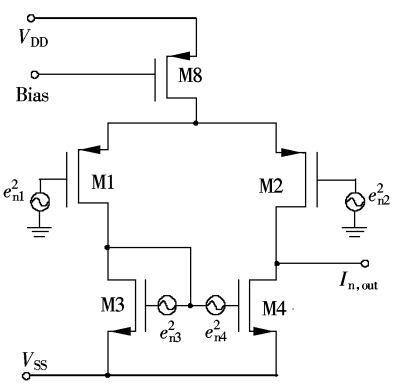


Fig. 5 The input stage including noise sources

The noise analyses are mainly centralized on $1/f$ noise and thermal noise. They are irrelevant and described as

$$e_{ni}^2 \approx e_{\mathrm{flick}}^2 + e_{\mathrm{thermal}}^2 \approx \frac{B}{fW_iL_i} + \frac{8kT}{3g_{\mathrm{m}}} \tag{4}$$

Substituting Eq. (4) into Eq. (3), we have

$$e_{\mathrm{eq}}^2 = 2e_{\mathrm{n1}}^2\left[1 + \left(\frac{K_{\mathrm{N}}B_{\mathrm{N}}}{K_{\mathrm{P}}B_{\mathrm{P}}}\right)\left(\frac{L_1}{L_3}\right)^2 + \sqrt{\frac{K_{\mathrm{N}}W_3L_1}{K_{\mathrm{P}}W_1L_3}}\right] \tag{5}$$

Eq. (5) suggests that in order to decrease the noise, the PMOS should have a large product of W_1 and L_1 and the ratio of L_3/L_1 should be increased. Eq. (3) shows that increasing g_{m1} can decrease the noise. Using the EKV-model, the g_{m} of the MOS in weak- and strong-inversion can be deduced to

$$g_{\mathrm{m,\,weak}} = \frac{I_{\mathrm{D}}}{nV_{\mathrm{T}}} \tag{6}$$

$$g_{\mathrm{m,\,strong}} = \frac{2nI_{\mathrm{D}}}{V_{\mathrm{eff}}} \tag{7}$$

and

$$\frac{g_{\mathrm{m,\,weak}}}{g_{\mathrm{m,\,strong}}}=\frac{V_{\mathrm{eff}}}{2n^2V_{\mathrm{T}}} \tag{8}$$

where $n\approx1.25$ is the slope factor and $V_{\mathrm{T}}\approx26.7$ mV at 37 ℃, the ratio of $g_{\mathrm{m,\,weak}}$ and $g_{\mathrm{m,\,strong}}$ is about 5.6 for a typical effective voltage of 300 mV. Therefore, the PMOS should work in weak inversion to increase g_{m} and decrease the noise. At the same time, power dissipation is reduced.

Further, an NMOS inverter with current-mirror load is adopted as the output stage. Functionally, the input stage provides high gain and the output stage ensures large output voltage swing. The amplifying circuit has a gain of

$$A_{\mathrm{V}}=A_{\mathrm{V1}}A_{\mathrm{V2}}=\frac{-g_{\mathrm{m1}}}{g_{\mathrm{ds2}}+g_{\mathrm{ds4}}}\frac{-g_{\mathrm{m6}}}{g_{\mathrm{ds6}}+g_{\mathrm{ds7}}} \tag{9}$$

The input transistors are greater than hundreds square micron, so the trade-off problem of compensation for phase margin is serious. In this design, the Miller capacitance C has a value of 5 pF. The zero point introduced by the Miller capacitance can affect the system stability. In our design, it is eliminated by a resistance, formed by an NMOS operated in a linear region, and $g_{\mathrm{m6}}=r_{\mathrm{ds8}}$.

The robustness of the biasing sub-circuit is very important for the design of an OPA. The detecting circuit consists of three-stage OPAs and they use one common biasing source, so it can realize power consumption reduction and strengthen system reliability. By analysis and simulation, the biasing output in this design is stable with the variations in power, temperature and process corners. In order to solve the idle-state problem of the biasing and amplifying sub-circuits, a startup sub-circuit is designed. Fig. 6 shows the schematic of the biasing sub-circuit and startup sub-circuit.

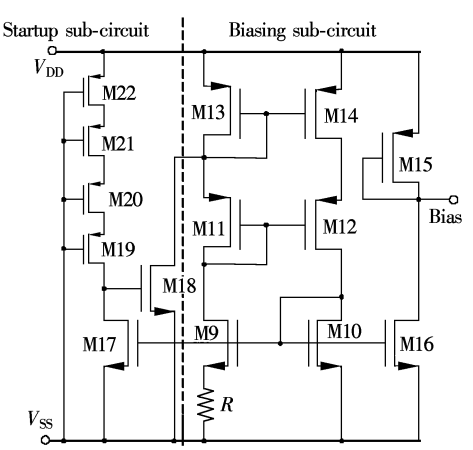


Fig. 6 The circuit schematic of the biasing sub-circuit and startup sub-circuit

3 Layout and Simulation

The placement of the monolithic MEA system is very important. Since the circuit has been designed for array design, the signal and power lines should be considered carefully. Fig. 7 shows the layout of the OPA and stimulating circuit. The upper side is the layout of the amplifying sub-circuit; the lower side is the layout of the biasing sub-circuit and the startup sub-circuit. In order to decrease the voltage offset, the layout of the amplifying sub-circuit is designed with a longitudinal symmetry. The size of the capacitor for the phase compensation occupies nearly half the size of the layout of the amplifying circuit. The chip size is 130 μm × 290 μm.

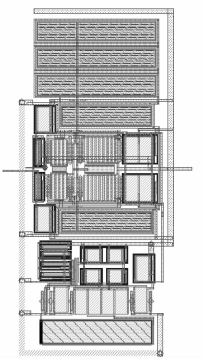


Fig. 7 The layout of the OPA and the stimulating circuit

The circuit has been simulated by using HSpice. The results of post-simulation are listed in Tab. 1. These key parameters have good compromise. And the OPA is of low power, low noise, small size and high gain.

The chip size of the detecting circuit is 290 μm × 400 μm. The results of post-simulation of the detecting circuit are listed in Tab. 2. The results show that the detecting circuit is of low power, low noise, small size and high gain.

Tab. 1 The post-simulation results of the OPA

Parameters	Value
Supply voltage/V	±2.5
Gain/dB	86.9
Phase margin/(°)	75
Input common-mode range/V	−2.5 ~ +2
Output range/V	−2.46 ~ +2.5
Power/μW	740
Equivalent input noise (not including 1/f noise)/(nV · Hz^{-1})	17.2
PSRR +/dB	87
PSRR −/dB	87
Area/mm^2	0.13 × 0.29

Tab. 2 The post-simulation results of the detecting circuit

Parameters	Value
Supply voltage/V	±2.5
Gain/dB	60.5
−3 dB frequency/kHz	67.2
Output range/V	−2.46 ~ +2.5
Power/mW	2.02
Equivalent input noise (not including 1/f noise)/(nV · Hz^{-1})	17.72
PSRR +/dB	60
PSRR −/dB	60
Area/mm^2	0.29 × 0.40

4 Chip Realization and Test

The detecting circuit is designed as one chip. The chip photo is shown in Fig. 8, the size is 0.81 mm × 0.46 mm, and the supply voltage is ±2.5 V. Fig. 9 shows the result of on-chip testing. Fig. 9(a) shows that the output signal with a

gain of 60 dB, the input signal is sinusoidal with V_{in} = 2 mV, 100 Hz. Fig. 9(b) shows that the output signal with a gain of 60 dB, input signal is an ECG signal with V_{in} = 2 mV, 10 Hz. Test results show that the performance of the detecting circuit satisfies the demand of neuron signal detecting.

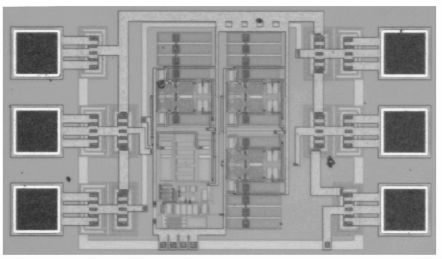
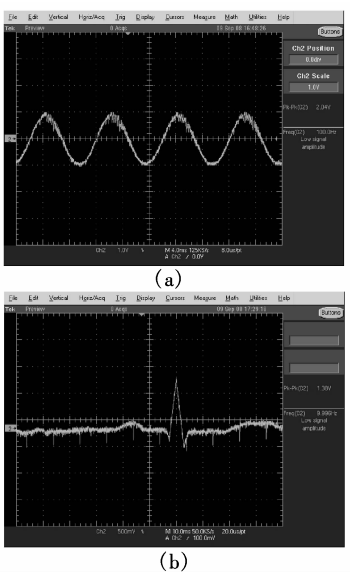


Fig. 8 The chip photo of the detecting circuit



(a)

(b)

Fig. 9 The waveform graphs of the output signal of the detecting circuit testing. (a) Input signal is sinusoidal signal with V_{in} = 2 mV, 100 Hz; (b) Input signal is ECG signal with V_{in} = 2 mV, 10 Hz

The monolithic integrated MEA is designed with 14 channel detecting loads and stimulating loads. Fig. 10 is the chip photo. The size is 3.1 mm × 2.6 mm.

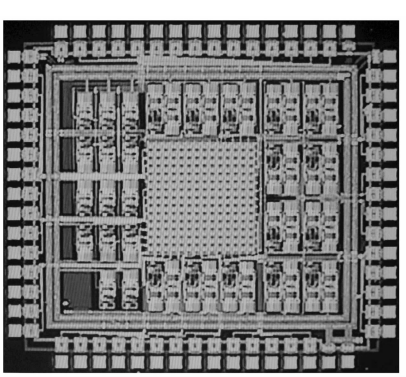


Fig. 10 The chip photo of the monolithic integrated MEA

5 Conclusion

A neuronal signal detecting circuit and a stimulating circuit are designed for the application of a large-scale MEA system. The scale of the MEA should be large enough for a microscopic study of a neuronal population. The circuits we designed satisfy the system demand: small size, low power, low noise, and high gain. The test results of the detecting circuit show that it works well. The future work will be devoted to experiments of neuron cultures on chips.

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用于单片集成 MEA 系统的神经信号探测电路和激励电路阵列

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摘要:介绍了单片集成 MEA 系统和用于该系统的神经元信号探测电路和激励电路,基本单元电路是低功耗、低噪声、高增益和小版图尺寸的运算放大器. 详细讨论了探测电路、激励电路和基本单元运算放大器的设计. 神经元信号探测电路版图面积 290 μm × 400 μm,功耗 2.02 mW,等效输入噪声 17.72 nV/Hz,增益 60.5 dB,输出电压摆幅 -2.48 ~ +2.5 V. 激励电路版图面积 130 μm × 290 μm,功耗 740 μW,输出电压摆幅 -2.5 ~ 2.04 V. 参数表明这 2 种电路适用于单片集成 MEA 系统. 探测电路和单片集成 MEA 系统已经流片. 探测电路的测试结果表明电路工作正常.

关键词:神经信号;探测;噪声;微电极阵列;CMOS 工艺
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