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Design of CMOS class-E power amplifier for low power applications

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Abstract: A fully integrated class-E power amplifier (PA) at 2.4 GHz implemented in a 0.18 μm 6-metal-layer mixed/RF CMOS (complementary metal-oxide-semiconductor transistor) technology is presented. A two-stage amplification structure is chosen for this PA. The driving stage produces a high swing switch signal by using resonation technology. The output stage is designed as a class-E topology to realize the power amplification. Under a 1.2 V power supply, the PA delivers a maximum output power of 8.8 dBm with a power-added efficiency (PAE) of 44%. A new power control method for the class-E power amplifier is described. By changing the amplitude and duty cycle of the signal which enters the class-E switch transistor, the output power can be covered from –3 to 8.8 dBm through a three-bit control word. The proposed PA can be used in low power applications, such as wireless sensor networks and biotelemetry systems.

Key words: class-E power amplifier; complementary metal-oxide-semiconductor transistor (CMOS) technology; low power application

As the minimum feature size in microelectronic devices reduces to deep submicron values, CMOS technology has become a feasible choice for implementation of radio frequency integrated circuits (RFIC) building blocks. In addition, portable devices are required to operate for extended periods of time without the need to charge the battery, which shows the importance of low-power circuits. The power amplifier (PA) vsually consumes a large percent of power in the RF transmitter front-end, which means that efficiency is important in the design of PAs. The class-E PA, first introduced by Sokal in 1975[1], is attractive to engineers because of its potential for high efficiency, which is 100% in theory. However, there are two challenges in the design of fully-integrated low-power PAs. First, unlike the high-power PAs, the low-power PAs require larger output loads and inductors. But such on-chip inductors in standard CMOS technology have very low quality factors, which degrade the PAs' performance greatly. Secondly, the power consumption of the driving stages is not negligible and severely degrades overall transmitter efficiency, which is less considered in high-power PAs. Therefore, in order to achieve high transmitter efficiency in low-power PAs, not only the output power stage, but also the driving stage needs to be optimized.

In this paper, a fully-integrated 2.4 GHz class-E PA with digital-control output power for low power applications, e.g., wireless sensor networks, biotelemetry systems, is presented in standard 0.18 μm RF CMOS technology, which achieves a maximum output power of 8.8 dBm with a 44% PAE and a minimum of –3 dBm with a 9% PAE at a 1.2 V supply.

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1 Class-E Power Amplifier Operation

The concept of class-E was introduced by Sokal[1] and it offered a new means to raise power amplification efficiency. Later in 1977, Raab expanded Sokal's work by providing an analytical basis for class-E operation[2]. A major improvement in class-E design was reported in 1987, Zulinski et al.[3] showed that class-E design may be maintained with the RF choke replaced by a smaller reactance, increasing the power output capability by a factor of about 2.5, which made a fully integrated class-E PA possible. Li et al. developed the idea and different design equations to optimize the operation by accurately tuning the output network[4-6]. The high efficiency properties of class-E PA make them attractive in the RF transmitter front-end.

All the parameters in the load network of class-E PAs, which operate in a switch-mode, need to be properly designed, so the following three criteria must be considered[2]: 1) The voltage across the switch at off-mode should not rise until the transistor is fully off; 2) The voltage across the switch should return to zero immediately before turn-on; 3) The slope of the switch voltage as a function of time should be zero at the moment of turn-on[7]. Basically, the design of the class-E PA load network is, from a mathematical point of view, a transcendent problem. The designer needs to iteratively solve the system of equations for a certain set of input parameters in order to fulfill the criteria of optimal operation. Recently, some new approaches have been proposed to address this problem. Milosevic et al.[5] developed a group of explicit, directly usable equations based on a certain number of discrete points of parameters which are interpolated by the Lagrange polynomial. The typical circuit structure of a class-E PA is shown in Fig. 1. The optimally designed values are calculated as follows[5]:

$$R_{\mathrm{L}} = \frac{V_{\mathrm{dd}}^2}{P_{\mathrm{out}}}(1.979 - 0.7783z + 0.1754z^2 - 0.01397z^3) \tag{1}$$

$$B = \omega C_1 = \frac{1}{R_{\mathrm{L}}}(1.229 - 0.7171z + 0.1881z^2 - 0.01672z^3) \tag{2}$$

$$X = \omega L_X = R_{\mathrm{L}}(-1.202 + 1.591z - 0.4279z^2 + 0.03894z^3) \tag{3}$$

$$z = \frac{\omega_0 L_1 P_{\mathrm{out}}}{V_{\mathrm{dd}}^2} \tag{4}$$

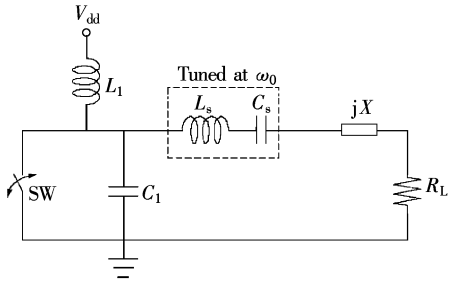

Fig. 1 Class-E PA circuit

where L_s and C_s act as a resonant circuitry at the frequency of interests and suppress other harmonics, with an extra inductance L_X for optimization consideration. The capacitance C_1 is a major design parameter in tuning the output network of class-E PAs. It contains non-linear output capacitances of transistors (C_{db} and C_{ds}), in addition to the layout parasitic capacitance.

2 Design Implementation of Proposed PA

The proposed PA consists of two stages, a class-E output stage and a driver stage, as shown in Fig. 2. The aim of the driver stage is to generate a square wave in order to efficiently switch the output transistor. Generally, there are two common approaches to generating square-like waves: a class-F amplifier and a pseudo-class-E amplifier. A class-F driving amplifier implemented by El-Desouki et al. [8] is based on peaking the odd harmonics and attenuating the even ones, but two on-chip inductors are needed at the expense of increasing the chip area and high Q inductors in CMOS technology is not available. The pseudo-class-E driving amplifier[9] is also not suitable in the low-power case, since the input power (e.g. $P_{in} < -10$ dBm) is too small to drive it.

Moreover, in the case of low power application, the power dissipation in the driver stage is also critical and should be carefully considered. To reduce the power in the driving stage, a matching network containing C_1, C_2 and L_t is inserted between the two stages to generate a certain resonance frequency at the gate of the output stage, as proposed by Oh et al. [10]. The separation of resonation and class-E operation nodes will bring extra benefits by avoiding interfering signals coming through the antennas compared with the class-E PA with cross-coupled NMOS oscillators[11].

2.1 Design of the load network for class-E PAs

The goal is to determine the values of the class-E load network elements for the following PA specifications: $V_{dd} = 1.2$ V, $P_{out} = 10$ mW, $f_0 = 2.45$ GHz and $L_1 = 4$ nH. There are two more things to be considered. First, the load resistance R_L is better set as 50 Ω, which is the impedance of the transmission line. In this way, the impedance transformer network which consumes extra power due to the non-ideal effect of the passive components is not necessary. Secondly, the output power should have a margin to compensate for the power loss in the circuit. There are two major losses: the loss in the switch transistor since we cannot generate an ideal square wave from the driving stage, and the loss in the passive components, especially the inductor, because of the low Q. Based on these considerations, P_{out} is trebled when calculating. From Eq. (4), we find $z = 1.326$ and applying Eqs. (1) to (3), we obtain the following values: $R_L = 57$ Ω, $B = 0.01$ S, $X = 13.96$ Ω. The calculated values of B and X correspond to a shunt capacitance C_d of 652 fF and a series inductance L_X of 0.91 nH, respectively.

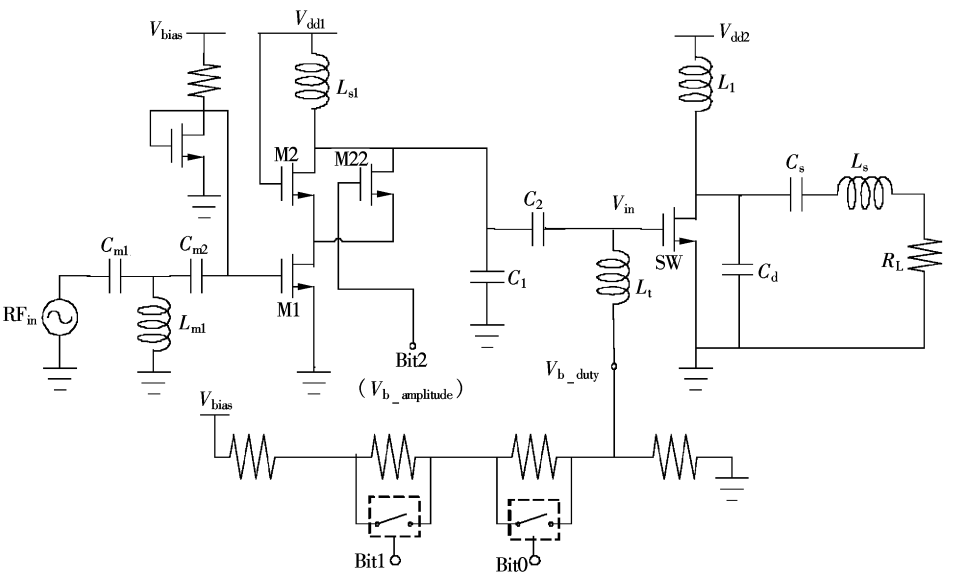

Fig. 2 Schematic of the proposed PA

The width of the switch transistor in the output stage is an important optimum parameter. In the traditional consideration, the width should be as great as possible to reduce the turn-on resistance r_{on} of the transistor. An estimation of this factor on drain efficiency(DE) is[7]

$$E_{DE} \approx \frac{1}{1 + 1.365(r_{on}/R_L)} \tag{5}$$

$$r_{on} = \frac{1}{\mu_n C_{ox}(W/L)(V_{gs} - V_{th})} \tag{6}$$

Choi et al. [12] found the relationship between the maximum PAE and the width based on the analytical model of a transistor. The larger the transistor, the larger the parasitic capacitance C_{db} and C_{ds} are. The device parasitic parameters and resultant degradation in transconductance severely im-

pact the circuit performance, especially the maximum PA operating frequency. According to the rule of thumb, the width making r_{on} one tenth of the load resistor R_L is a recommended initial value, which makes E_{DE} about 88% from Eq. (5).

2.2 Implementation of digital power-control

One important issue in the design is to implement the output power control which is often required in practical applications. Since the input signal provides only timing information in a class-E amplifier, the output power cannot be controlled by changing the width of the input transistor as is normally done in a linear amplifier. Instead, the output power control can be realized through a variable supply implemented by a DC-DC converter. But in practical applications, it is not easy to apply such an additional variable supply and the DC-DC converter circuit will consume extra power which reduces the overall efficiency.

In this paper, a three-bit control pad (Bit2-Bit0), as shown in Fig. 2, is designed to change the output power digitally. With a control word "111", the maximum power is available, while the minimum is at "000". The control of output power is achieved by changing the duty cycle and the amplitude of the signal (V_{in}) which is the input to the gate of switch transistor SW.

Since the turn-on resistance r_{on} of switch transistor SW is a factor which degrades the output power and efficiency, changing the amplitude of V_{in} will accordingly change the output power. The amplitude of V_{in} is controlled by the gain of the first stage, which can be altered by the width of the cascade transistor. Bit2 controls the state of M22 in Fig. 2. When Bit2 is high, M22 is paralleled into the circuit and the gain of the first stage increases. So is the amplitude of V_{in}.

Another method to control the power is by altering the duty cycle of the V_{in}, because all the values of the load network components depend on the signal's duty cycle[2]. This method is implemented by controlling the bias voltage of switch transistor V_{b_duty} in this paper. When V_{b_duty} increases, the duty cycle of V_{in} increases, so a higher output power is obtained. The way to control V_{b_duty} is very simple. A resistor voltage divider can be utilized as shown at the bottom of Fig. 2. Bit1 and Bit0 are used here to control the two switches to change the bias voltage V_{b_duty}.

Combining the change of amplitude and the duty cycle of the input signal V_{in} will give a wider adjustable output power range, and no more components are needed when compared with the traditional method.

3 Experimental Results and Analysis

The circuit is designed in a standard 6-metal layer, 0.18 μm RF CMOS technology. Fig. 3 shows the layout of the PA including pads that occupies an area of 0.95 mm^2. All major interconnections and inductors are laid out using the top metal layer to minimize the parasitic effects. Fig. 4 shows P_{out} and PAE of the class-E PA vs. input power with a 1.2 V supply voltage at 2.45 GHz. A PAE of 44% is achieved with a 10-dBm input power while delivering an output power of 8.8 dBm, as shown in Fig. 4.

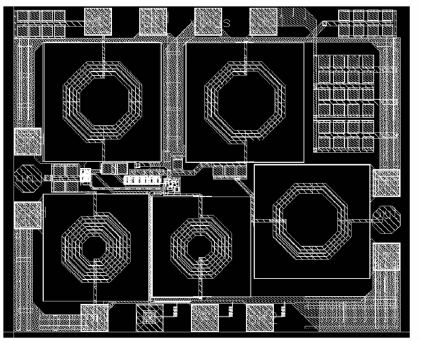

Fig. 3 Layout of the proposed Class-E PA

As the supply voltage V_{dd2} increases, the output power as well as the efficiency becomes greater as shown in Fig. 5. The minimum output power can be as low as 0.3 dBm at a 0.4 V supply with a PAE of 21%, which can be used in a WSN system where a 0-dBm output power is typically needed. When using the digital controlling method, a DC-DC converter which dissipates extra power is not needed. With the control word "111", the maximum power is available, while the minimum is at "000". A power from −3.0 to 8.8 dBm is obtained in this case with the PAE from 9% to 44%, as shown in Fig. 6.

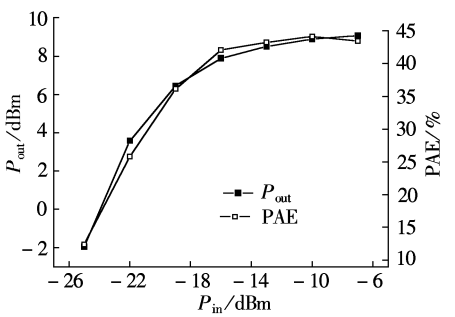

Fig. 4 P_{out} and PAE vs. input power P_{in} with a 1.2 V supply voltage

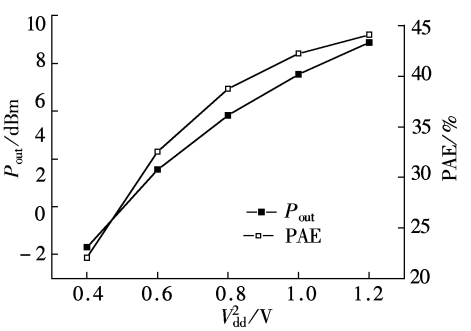

Fig. 5 P_{out} and PAE vs. supply voltage of the second stage

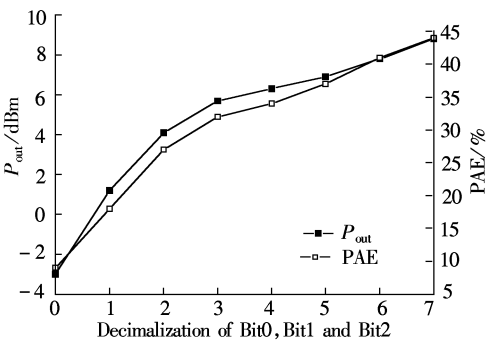

Fig. 6 3-bit digital power control of class-E PA

A traditional way to test the stability of an amplifier is to simulate the *K*-factor. The circuit designer has to make sure that the *K*-factor is greater than one in the whole frequency range; otherwise, compensation is needed. The *K*-factor of the proposed class-E PA is shown in Fig. 7, where the value of *K* is always greater than one. However, we still cannot guarantee stability because the class-E PA operates in a large signal state while the *K*-factor is a measurement of a small signal condition. Time-domain simulations should also be checked. The time-domain simulation in Fig. 8 shows that the PA quickly returns to the stable state (after 5 ns) as an impulse signal is applied. Tab. 1 presents the summary of performances compared with the previously reported works.

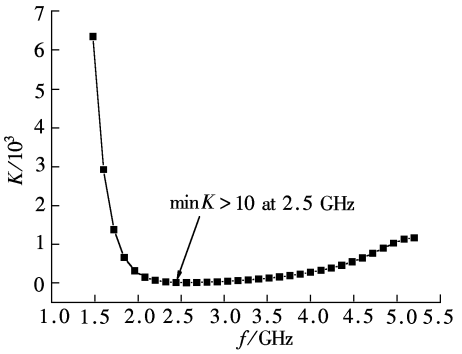

Fig. 7 Trace of *K*-factor up to 5. 5 GHz

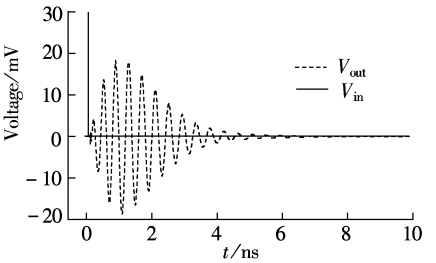

Fig. 8 Impulse input and the corresponding response at output

Tab. 1 Performance comparison between CMOS low-power PAs

Reference	Technology CMOS/μm	Frequency/ GHz	PA class	Supply voltage/V	Output power/dBm	Power gain/dB	PAE/ %	Chip area/ mm^2	Integration level
Ref. [13]	0. 18	2. 40	AB	1. 8	9	19	16		Off-chip
Ref. [14]	0. 13	1. 90	AB	1. 2	4. 1		26		Off-chip
Ref. [10]	0. 18	2. 35	E	1. 0	9. 5	15. 5	43	1. 7	Fully-integrated
Ref. [8]	0. 18	2. 40	E	1. 2	9. 5	11	33	1. 1	Fully-integrated
This paper	0. 18	2. 45	E	1. 2	8. 8	18. 8	44	0. 95	Fully-integrated

4 Conclusion

A class-E PA for low power applications is presented, and a digital method is proposed for output power controlling to achieve a maximum output power of 8. 8 dBm with a 44% PAE and a minimum of −3 dBm with a 9% PAE at a 1. 2 V supply. The proposed class-E PA can achieve high PAE, which shows the feasibility of using class-E PAs for low power applications. The chip has been sent to SMIC by the MPW center of the Institute of RF- & OE-ICs of the Southeast University.

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低输出功率应用的 E 类 CMOS 功率放大器设计

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摘要:利用标准的 0.18 μm 6 层金属混合信号/射频 CMOS 工艺设计了一种工作在 2.4 GHz 频段的全集成 E 类功率放大器. 电路采用两级放大器级联结构,其中驱动级利用谐振技术生成高摆幅开关信号;输出级采用 E 类结构实现了信号的功率放大. 在 1.2 V 电源电压下,设计的功率放大器最高输出功率为 8.8 dBm,功率附加效率(PAE)达到 44%. 同时,提出了一种 E 类功率放大器功率控制方法. 通过改变进入 E 类开关晶体管的信号幅度和占空比,在 3 位数字控制字的控制下,输出功率达到 -3 ~ 8.8 dBm. 所设计的功率放大器可以满足诸如无线传感网络(WSN)和生物遥测等低功率系统的应用.

关键词:E 类功率放大器;CMOS 工艺;低功率应用

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