Journal of Southeast University (English Edition) Vol. 25, No. 2, pp. 185 – 188 June 2009 ISSN 1003—7985

New battery management system for multi-cell li-ion battery packs

Chen Chen Jin Jin He Lenian

(Institute of VLSI Design, Zhejiang University, Hangzhou 310027, China)

Abstract: This paper proposes a new battery management system (BMS) based on a master-slave control mode for multi-cell li-ion battery packs. The proposed BMS can be applied in li-ion battery packs with any cell number. The whole system is composed of a master processor and a string of slave manager cells (SMCs). Each battery cell corresponds to an SMC. Unlike the conventional BMS, the proposed one has a novel method for communication, and it collects the battery status information in a direct and simple way. An SMC communicates with its adjacent counterparts to transfer the battery information as well as the commands from the master processor. The nethermost SMC communicates with the master processor directly. This method allows the battery management chips to be implemented in a standard CMOS (complementary metal-oxide-semiconductor transistor) process. A testing chip is fabricated in the CSMC 0.5 μm 5 V N-well CMOS process. The testing results verify that the proposed method for data communication and the battery management system can protect and manage multi-cell li-ion battery packs.

Key words: battery management system; CMOS integrated circuits; master-slave control

The li-ion battery has become the most widely used chargeable battery nowadays due to its many advantages, such as higher voltage level, higher energy density, no memory effects and no pollution to the environment[1]. Li-ion battery packs of multicells in series, which provide a high-voltage power supply, have become more and more popular in many applications, e. g. hybrid electric vehicles, electro motors, etc. However, as the power supply voltage rises, the cell number should also increase. Battery management for battery packs composed of multicells is quite different from single cell applications, and thus challenges arise.

For battery management, the information of each battery cell must be acquired and processed to ensure the safety operation of every single cell and hence the whole battery pack. Refs. [2 – 3] proposed methods of sampling each battery voltage in turn. The sampling is controlled by a multi-phase clock. Therefore, the battery voltage is not monitored at any moment. Moreover, a multi-phase clock generator is desired. As the number of the battery cells changes, the multi-phase clock generator must be redesigned as well. Another intuitive way to realize a BMS is to implement the system in an expensive high-voltage process as described in Ref. [4]. Ref. [4] employs a master-slave control mode. Each battery cell has a corresponding data acquisition module (slave) which is identical with each other. The data acquisition module acquires the information of the corresponding battery cell and then sends it to the central processor (master). When the number of the battery cells changes, only the number of the data acquisition modules need to be altered accordingly. However, the voltage levels at each data acquisition module are quite different and may be rather high with reference to the negative terminal voltage of the battery pack. In order to make effective communications with the central processor, the data acquisition module employs a costly communication interface implemented in a high-voltage process.

This paper proposes a new BMS which can be implemented in a standard CMOS process and which has a lower cost than that of a high-voltage process. The proposed BMS employs a master-slave control mode. The whole system is composed of a master processor and a string of identical SMCs. Unlike the existing BMS, the SMC in the proposed system communicates with its adjacent counterparts to transfer the battery information as well as the commands from the master processor. This method makes the application easy and flexible. A testing chip is fabricated in the CSMC 0.5 μm 5 V CMOS process. The testing results verify that the proposed method for data communication and the whole system function well.

1 System Description

1.1 Block diagram

Fig. 1 is the application diagram of the presented BMS for a battery pack with n cells. The presented system is composed of a number of chips, i. e., a master processor chip and a string of identical SMC chips. The SMC obtains the information about the corresponding battery cell and communicates with the adjacent counterparts. The master proces-

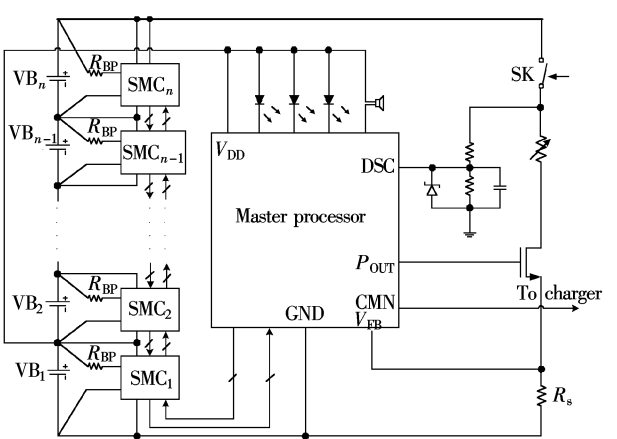

Fig. 1 The application diagram of the presented BMS

Received 2008-10-21.

Biographies: Chen Chen (1982—), female, graduate; He Lenian (corresponding author), male, professor, helenian@vlsi.zju.edu.cn.

Foundation item: The Key Science and Technology Project of Zhejiang Province (No. 2007C21021).

Citation: Chen Chen, Jin Jin, He Lenian. New battery management system for multi-cell li-ion battery packs[J]. Journal of Southeast University (English Edition), 2009, 25(2): 185 – 188.

sor receives data and sends out commands through the nethermost SMC only. The batteries are numbered from bottom to top, as VB_1, VB_2, …, VB_n. The corresponding SMC of VB_i ($i = 1, 2, \ldots, n$) is named as SMC_i accordingly. The resistor R_{BP} beside each SMC is used for equalization. The arrow lines in Fig. 1 are the communication routes. CMN from the master processor interacts with the charger. The input voltage of DSC indicates whether the switch SK has been pressed or not. And once abnormality has arisen when discharging, the output port P_{OUT} turns off the MOS switch to terminate discharging.

1.2 Slave manager cell

Each SMC is an individual chip. The SMC is powered by a corresponding battery cell. The positive terminal of the corresponding battery cell is the power supply V_{DD} of the SMC chip and the negative terminal is the ground. Thus, the SMC directly senses the voltage of the battery cell and compares it with the built-in references.

Different cells in the same battery pack are potentially unequal[5-6]. Therefore, some may be charged fast and some may have a slower charge rate. In order to avoid the inequality between different battery cells becoming so severe that the whole battery pack cannot be used any more, an equalization mechanism is adopted in the charge management. When a battery cell charges faster than some other ones, its charging current will be shunted by the bypass resistor R_{BP}. Then the battery cells with a slower charge rate will be able to catch up with the faster ones. The equalization circuit is illustrated in Fig. 2. An NMOS pass device N_0 is used as the bypass switch. There are four spots during the charging process, i. e., 3.9, 4.0, 4.1 and 4.2 V. At the beginning of the charging process, the reference V_{ref_EQ} is initialized at 3.9 V and it is compared with the battery voltage V_B. At the same time, the NMOS pass device is turned off for a few milliseconds. Once the battery voltage reaches 3.9 V, N_0 is turned on and the actual charging current of the battery is reduced. Meanwhile, the signal /ARV becomes "0" to flag that this battery has reached the level of current V_{ref_EQ}. When all the batteries reach 3.9 V, the master processor will send out the pulse signal /CLR to clear all the bypass branches. Simultaneously, V_{ref_EQ} goes to the next step 4.0 V. The above moves repeat until V_{ref_EQ} reaches 4.2 V. In the equalization circuit, an RS latch, where reset is prior to set, is used to control the bypass switch N_0. The bypass current is designed to be 150 mA. As a result, N_0 is fairly large and needs a driver.

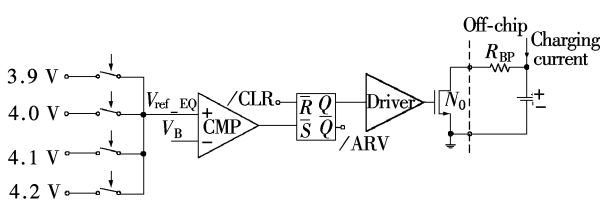

Fig. 2 The equalization circuit in the SMC

When the battery voltage reaches 4.2 V while charging, the SMC will give out the signal TOV to indicate that the charging loop should be cut off. Similarly, once the battery voltage gets lower than 2.75 V while discharging, the SMC will send out the signal SDC so that discharge will terminate. Li-ion batteries also need temperature protection. Signals TCHG and TDSC indicate whether the temperature goes beyond the limited ranges while charging and discharging respectively.

In order to save the power consumption of the battery pack, the whole system stays in sleep mode most of the time. The master processor becomes active only when the charger is plugged in or the load is connected. Once the master processor awakes, it sends out the signal /SDN to SMC_1 in order to wake up the SMCs. Meanwhile, another signal /DSC is produced and sent to SMC_1 at the same time so that the SMCs will know whether the battery pack is about to charge or discharge.

Communications are essential in this system. The signals about the status of the battery cells are transferred from top to bottom; and the signals containing the commands from the master processor are delivered from bottom to top. Fig. 3 shows the circuit module transferring a signal downwards. And the circuit module transferring a signal upwards is illustrated in Fig. 4. /ARV, TOV, SDC, TCHG and TDSC are transferred from top to bottom. Each of them has an individual transferring circuit as shown in Fig. 3. Down_in is the input port and down_out is the output port. The down_in in SMC_i ($i = 1, 2, \ldots, n$) is connected to the down_out from SMC_{i+1}. Down_in is either $V_{DD} + 2V_D$ or V_{DD}. V_D is the forward voltage of a diode. $V_{DD} + 2V_D$ is taken as a logic one and V_{DD} is viewed as a logic zero. A comparator achieves the task of converting the analog input into a logic signal. Since the input can be greater than V_{DD} by a voltage of $2V_D$, down_in is divided into a half and compared with ($V_{DD} + V_D$)/2. In order to have little effect on down_in, R_2 and R_3 are much greater than R_1. Down_in of the uppermost SMC, i. e., SMC_n, is connected with V_{DD}, which stands for a logic zero. If a logic one is desired to pass onto the next SMC, the NMOS switch at down_out will turn off and down_out will output a voltage of $2V_D$, which is $V_{DD} + 2V_D$ for the SMC below. Similarly, if a logic zero is desired, the NMOS switch will turn on and down_out will produce a voltage of zero, which is V_{DD} for the next SMC. Logicin in Fig. 3 is fed with

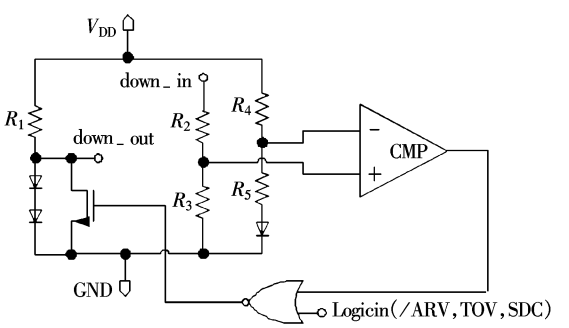

Fig. 3 The circuit module transferring signal downwards

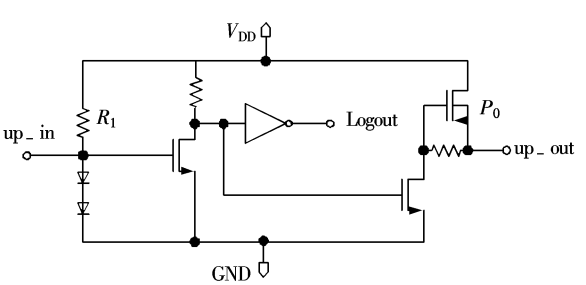

Fig. 4 The circuit module transferring signal upwards

the logic signal standing for the status of this battery cell. Taking /ARV, for example, down_out is renamed as /ARV_out and down_in is renamed as /ARV_in. The nethermost /ARV_out will produce a logic true signal only when all the bypass branches are turned on. The uppermost /ARV_in has been stuck as a logic zero. As a result, logic zero must stand for true in this case. If the logical value of /ARV_in is true, it means that all the above SMCs have bypass branches turned on. /ARV_out will be logic true if /ARV_in and the /ARV in this SMC are both true. As for SDC, down_in is renamed as SDC_in, and down_out is renamed as SDC_out correspondingly. This time, logic one must be viewed as true since the nethermost SDC_out will become logic true if any of the SMCs has its SDC logic as true. The same holds for transferring TOV, TCHG and TDSC.

/SDN, /CLR and /DSC are the signals being transmitted from bottom to top. Up_in is the input port and up_out is the output port. The up_out in $SMC_i(i = 1, 2, \ldots, n)$ is connected to the up_in from SMC_{i+1}. The PMOS switch P_0 plays the same role as the NMOS switch in Fig. 3. The only difference is that, when P_0 is closed, it shorts the diodes in the upper SMC. When transferring logic one, P_0 is opened so that up_out is $V_{DD} + 2V_D$ and up_in of the upper SMC is $2V_D$. Since up_out can be higher than V_{DD} by $2V_D$, the bulk of P_0 is tied to up_out. When transferring logic zero, P_0 is closed and up_out is shorted to V_{DD} which is zero for the upper SMC. An NMOS transistor as well as a resistor forms an inverter with a relatively low threshold voltage. It converts up_in into a digital signal which is suitable for normal logic circuits. The output logout controls the operation of the internal logic circuits. The highest voltage in the transferring circuits is $V_{DD} + 2V_D$, which is definitely lower than 6.0 V. Consequently, it can be implemented in a standard CMOS process.

1.3 The master processor

Fig. 5 shows the block diagram of the master processor. The master processor only needs to deal with the signals from SMC_1. In the same way as SMC_1, the master processor takes the negative terminal of the battery pack as the ground. Thus Down_out from SMC_1 is either $2V_D$ or 0 for the master processor. With the same mechanism illustrated in Fig. 4, the inputs can be easily converted into digital signals. On the other hand, if the master processor wants to send out a logic one, floating the input port of SMC_1 will do; if a logic zero is desired, the master processor just needs to short the input port of SMC_1 to the ground. As a result, a sole NMOS is suitable for the output stage of the communication interface.

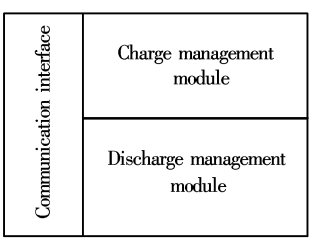

Fig. 5 The block diagram of the master processor

At the beginning of the charging process, the master processor issues a pulse on the signal /CLR to clear all the bypass branches as initialization. The pulse width of /CLR is about 1 ms. During the charging process, the master processor sends out a pulse on /CLR once it receives a logic zero on the signal /ARV. Then all the bypasses are cleared and $V_{ref, EQ}$ in the SMCs goes to the next step. If the logic one on TCHG is observed, the charging process pauses; and when the logic one on TOV appears, the charging loop cuts off.

While discharging, the user can select whether to use the soft start function or not. During the soft start, the average discharging current increases step by step. Similarly, the pulse width modulation is an available option for the user. When overload tends to happen and the pulse width modulation mode is selected, the switch in series with the load is regulated so that the average discharging current remains constant. In addition, the discharging process pauses when the battery temperature is beyond the limited range, and the discharging process terminates when the logic one on SDC appears.

2 Experimental Results

The slave manager cell has been implemented in the CSMC 0.5 μm 5 V N-well CMOS process. Fig. 6 shows the photograph of the chip and Fig. 7 is the photograph of the test bench of five SMCs. In order to observe the changes on /ARV one by one when testing the equalization mechanism, the initial voltage of $VB_i(i = 1, 2, \ldots, 4)$ is set to be lower than VB_{i+1}. So the bypass branch for VB_5 turns on first and that for VB_1 turns on last. Tab. 1 shows the measured points where the bypass branches turn on.

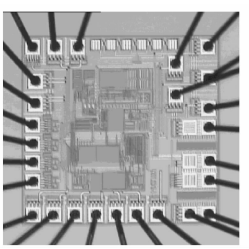

Fig. 6 The photograph of the chip of SMC

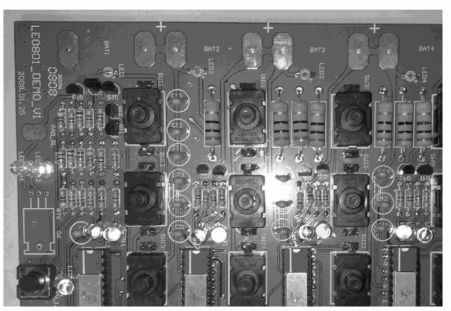

Fig. 7 The photograph of the test bench

When testing the discharge management, we decrease the voltage of one battery while keeping the other four greater than 3 V. When the battery voltage gets lower than the preset discharge termination voltage, SDC_out from the corresponding SMC turns logic one. So do all the SDC_outs below. Tab. 2 shows the measured results.

Tab. 1 Measured results on equalization mechanism V

Battery number	Measured battery voltage			
	Step 1	Step 2	Step 3	Step 4
VB_1	3.894	3.994	4.092	4.191
VB_2	3.883	3.980	4.078	4.176
VB_3	3.874	3.972	4.071	4.171
VB_4	3.876	3.974	4.073	4.171
VB_5	3.925	4.026	4.128	4.228

Tab. 2 Measured discharge termination voltage V

Battery number	Measured discharge termination voltage
VB_1	2.749
VB_2	2.744
VB_3	2.742
VB_4	2.752
VB_5	2.765

Seen from the testing results in Tab. 1 and Tab. 2, the built-in references in SMC have a variation of 1%. The accuracy of the built-in references can be improved by trimming.

In the sleep mode, the nethermost /SDN_in is floated. Only the circuits transferring /SDN are working. And the measured power dissipation of the system is less than 10 μA.

3 Conclusion

This paper proposes a new BMS, which employs a master-slave control mode. The whole system is composed of a master processor and a string of identical SMCs. Each battery cell corresponds to an SMC. The SMC in the proposed system communicates with the adjacent counterparts to transfer the battery information as well as the commands from the master processor. The nethermost SMC directly communicates with the master processor. This method is simple to apply. And it allows the battery management chips to be implemented in a standard CMOS process at low costs. On the other hand, as the cell numbers increase, more SMCs are needed, which increases the costs of the system. Nevertheless, taking the practical cell numbers of the battery packs now in use into consideration, the cost of the system is affirmatively less than that implemented in a high voltage process. Furthermore, the SMCs and the master processor can be encapsulated in the same package. In this way, the communication between the SMCs and that between the SMC and the master processor can be completed inside one chip.

References

[1] Chern T L, Pan P L. The research of smart li-ion battery management system [C]//*Proc of the Second IEEE Conference on Industrial Electronics and Applications*. Harbin, China, 2007: 2273 – 2277.

[2] Qiang Jiaxi, Yang Lin, Ao Guoqiang, et al. Battery management system for electric vehicle application [C]//*Proc IEEE International Conference on Vehicular Electronics and Safety*. Shanghai, China, 2006: 134 – 138.

[3] Chatzakis J, Kalaitzakis K. Designing a new generalized battery management system [J]. *IEEE Trans Industrial Electronics*, 2003, **50**(5): 990 – 999.

[4] Niu Liyong, Jiang Jiuchun, Zhang Xin. A study on battery management system of Ni-MH battery packs for hybrid electric vehicle applications [C]//*Proc of the First International Power and Energy Conference*. Putrajaya, Malaysia, 2006: 30 – 33.

[5] Asumadu J, Haque M, Vogel H, et al. Precision battery management system [C]//*Instrumentation and Measurement Technology Conference*. Ottawa, Canada, 2005: 1317 – 1320.

[6] Jwo Wu-Shun, Chien Wei-Liang. Design and implementation of a charge equalization using positive/negative pulse charger [C]//*Industry Applications Conference*. New Orleans, LA, USA, 2007: 1076 – 1081.

一种新型多节锂离子电池包管理系统

陈 琛 金 津 何乐年

(浙江大学超大规模集成电路设计研究所,杭州 310027)

摘要: 为多节锂离子电池包提出了一种新型的基于主从式控制的管理系统. 该电池包管理系统适用于任意节锂离子电池包. 整个系统由一个主控制器和一组子管理芯片组成. 电池包的每节电池对应一个子管理芯片. 与现有的电池管理系统不同,所提出的方案具有独特的通信方式,并能简单直接地采集电池状态信息. 每个子管理芯片和与其相邻的子芯片通讯,传递电池信息并接受来自主控制器的命令. 该方法能够使电池包管理芯片系统在标准的 CMOS 工艺平台上实现. 一块基于 CSMC 0.5μm 5V N 阱 CMOS 工艺的测试芯片经过流片并测试,验证了所提出的信号通讯方式和电池包管理芯片系统能完成对多节锂离子电池包的保护与管理.

关键词: 电池管理系统;CMOS 集成电路;主从式控制

中图分类号: TN401