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Step memory polynomial predistorter for power amplifiers with memory

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Abstract: To reduce the number of digital predistortion coefficients, a step memory polynomial (SMP) predistorter is presented. The number of predistortion coefficients is decreased by adjusting the maximum nonlinear order for different memory orders in the traditional memory polynomial (MP) predistorter. The proposed SMP predistorter is identified by an offline learning structure on which the coefficients can be extracted directly from the sampled input and output of a PA. Simulation results show that the SMP predistorter is not tied to a particular PA model and is, therefore, robust. The effectiveness of the SMP predistorter is demonstrated by simulations and experiments on an MP model, a parallel Wiener model, a Wiener-Hammerstein model, a sparse-delay memory polynomial model and a real PA which is fabricated based on the Freescale LDMOSFET MRF21030. Compared with the traditional MP predistorter, the SMP predistorter can reduce the number of coefficients by 60%.

Key words: power amplifier; predistortion; memory effects; memory polynomial

One of the challenges in designing RF power amplifiers (PAs) is the linearity requirement. As more and more non-constant envelope signals are transmitted to utilize the limited frequency resources efficiently, higher peak-to-average power ratio (PAPR) results lead to stronger linearity requirements of RF PAs. Memory effects also become significant in high-efficiency PAs operating with wideband signals and need to be considered for these PAs' linearization[1]. Of all linearization techniques, predistortion is among the most effective and popular ones. A predistorter is a functional block that precedes the PA. It generally creates an expanding nonlinearity since the PA has a compressing characteristic. Ideally, it is hoped that the output of a PA is a scalar multiple of the input of the predistorter-PA chain[2].

In the past, several behavioral models of PAs were proposed to model the memory effects, such as the Volterra model[3-4], the Wiener model[5-6], the parallel-Wiener model[7], the Wiener-Hammerstein model[8] and the memory polynomial (MP) model[2]. It is difficult to judge which PA model is the best, since it depends on the type of the PA and the data format being transmitted etc. In applications, predistortion linearization is the ultimate objective. Our goal here is to find a good model to approximate the inverse of the nonlinearity PA with memory, in the sense that parameter extraction and system implementation are straightforward and the predistorter model is robust. The memory polynomial model[2, 9-10] is shown to be a good model for predistorters and it is robust. But when long-term memory effects[11] are considered, the memory polynomial model requires a large number of coefficients, and shows a slow convergence of root mean square (rms) error between measured output and predicted output by adding delay taps. These disadvantages can be minimized by adopting sparse delay taps in modeling PAs[10]. Yet a memory polynomial model with sparse delay taps (MPMSD) introduced by Hyunchul et al. is unsuitable for a predistorter due to high computational complexity and relatively slow convergence.

To solve this problem, a step memory polynomial (SMP) predistorter is proposed. Instead of a constant maximum nonlinear order in a memory polynomial predistorter, the proposed SMP predistorter has a non-constant maximum nonlinear order. Compared with the traditional memory polynomial predistorter, the SMP predistorter can efficiently decrease the number of coefficients, especially when long-term memory effects are considered. The corresponding offline learning structure[12] and the identification algorithm are also detailed. Owing to the offline learning structure, the coefficients of the proposed predistorter can be directly extracted from the sampled input and output of a PA through a simple offline process. The linearization performance of the SMP predistorter is validated by simulations and experiments. The results show that the SMP predistorter can work as well as the traditional MP predistorter with fewer coefficients.

1 Step Memory Polynomial Model for Predistorter

Let us consider a traditional memory polynomial predistorter with the input $x(n)$ and output $y(n)$,

$$y(n) = \sum_{k=1}^{K} \sum_{q=0}^{Q} a_{kq} x(n-q) \mid x(n-q) \mid^{k-1} \qquad (1)$$

where K is the maximum nonlinearity order and Q represents the maximum memory order. In Eq. (1), a K-th order polynomial of $x(n-q)$ ($q = 0, 2, \ldots, Q$) is used to represent its contribution to the output $y(n)$. In other words, the maximum nonlinear order is constant for every input. Since the effects of nonlinear dynamics tend to fade with increasing order in many real PAs[4], we can try to adjust the maximum nonlinear order of the past input to decrease the number of coefficients and keep the linearity of the predistorter-PA chain.

Let $K = K_q$, then Eq. (1) becomes

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$$y(n) = \sum_{q=0}^{Q} \sum_{k=1}^{K_q} a_{kq} x(n-q) \mid x(n-q) \mid^{k-1} \quad (2)$$

where K_q is the maximum nonlinearity order, and it is nonconstant and varies with memory order q. Eq. (2) is referred to as a step memory polynomial model. In practical applications, in a predistorter, K_0 is usually the maximum of all K_q ($q = 0, 1, \ldots, Q$).

2 System Identification

The coefficients of the proposed predistorter are extracted based on an offline learning structure[12], whose configuration is shown in Fig. 1. Instead of modeling a PA's behavioral model and then building a corresponding predistorter, we extract the coefficients of the predistorter directly from the input and output data of a PA. This structure eliminates the real-time closed-loop adaptation requirement, and allows us to extract the parameters through a simple offline process.

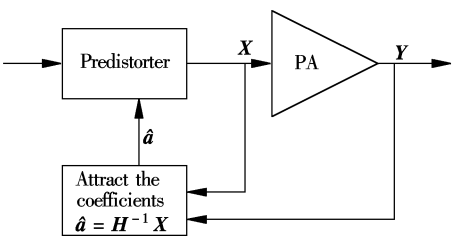

Fig. 1 Offline learning structure

As we know, the characteristic of a predistorter and the characteristic of a PA are inverse. In Ref. [3], it is shown that if one has a p-th-order post-inverse of a general Volterra system, then the p-th-order pre-inverse is identical. The memory polynomial model is a special case of the Volterra model[2]. Thus, for an arbitrary order of approximation, predistortion is equivalent to postdistortion in our application. If the input and the output data of a PA are represented by $\boldsymbol{X}$ and $\boldsymbol{Y}$ (scaled) respectively, then the characteristic of the corresponding predistorter can be extracted from $\boldsymbol{X}$ and $\boldsymbol{Y}$. This means that $\boldsymbol{X}$ is expected to be the output of the predistorter while $\boldsymbol{Y}$ is assumed to be the input of the predistorter.

Now the output $\boldsymbol{X}$ and the input $\boldsymbol{Y}$ of the predistorter are given. In order to extract the coefficients of the step memory polynomial model, the step memory polynomial function is represented by a matrix equation. From the given input data $\boldsymbol{Y}$ and the output data $\boldsymbol{X}$ in the time domain, we can define

$$\boldsymbol{X} = [x(l) \quad x(l+1) \quad \ldots \quad x(l+N-1)]^{\mathrm{T}} \quad (3)$$

and

$$\boldsymbol{H} = [\boldsymbol{H}_0 \quad \ldots \quad \boldsymbol{H}_q \quad \ldots \quad \boldsymbol{H}_Q] \quad (4)$$

where

$$\boldsymbol{H}_q = \begin{bmatrix} h_{1,q}(l) & h_{2,q}(l) & \ldots & h_{K_q,q}(l) \\ h_{1,q}(l+1) & h_{2,q}(l+1) & \ldots & h_{K_q,q}(l+1) \\ \vdots & \vdots & & \vdots \\ h_{1,q}(l+N-1) & h_{2,q}(l+N-1) & \ldots & h_{K_q,q}(l+N-1) \end{bmatrix} \quad (5)$$

$$h_{k,q}(l) = \mid y(l-q) \mid^{k-1} y(l-q) \quad (6)$$

Let the complex coefficients be represented as follows:

$$\boldsymbol{a} = [\boldsymbol{a}_0 \quad \ldots \quad \boldsymbol{a}_q \quad \ldots \quad \boldsymbol{a}_Q]^{\mathrm{T}} \quad (7)$$

where

$$\boldsymbol{a}_q = [a_{1,q} \quad a_{2,q} \quad \ldots \quad a_{K_q,q}] \quad (8)$$

Eq. (2) with N consecutive time-domain data points can be represented with a matrix equation such as

$$\boldsymbol{X} = \boldsymbol{H}\boldsymbol{a} \quad (9)$$

where $\boldsymbol{X}$ is an $N \times 1$ vector; $\boldsymbol{H}$ is an $N \times \sum_{q=0}^{Q} K_q$ matrix; and $\boldsymbol{a}$ is a $\sum_{q=0}^{Q} K_q \times 1$ vector. The expected coefficients can be acquired using the following equation:

$$\hat{\boldsymbol{a}} = \boldsymbol{H}^{-1}\boldsymbol{X} \quad (10)$$

where $\boldsymbol{H}^{-1}$ denotes the pseudo-inverse matrix of $\boldsymbol{H}$ and $\hat{\boldsymbol{a}}$ is the least-square solution of Eq. (9). Then

$$\hat{\boldsymbol{X}} = \boldsymbol{H}\hat{\boldsymbol{a}} \quad (11)$$

To give a quantitive measure of the linearization accuracy, a normalized mean square error (NMSE)[13] can be acquired as

$$e_{\mathrm{NMSE}} = 10\log_{10}\left[\frac{\sum_{l=0}^{N-1} \mid x(l) - \hat{x}(l) \mid^2}{\sum_{l=0}^{N-1} \mid x(l) \mid^2}\right] \quad (12)$$

where $x(l)$ is the desired PA output and $\hat{x}(l)$ is the PA output with predistortion.

3 Simulations

In this section, we illustrate the performance of the SMP predistorter identified by the offline learning structure. We will show that the SMP predistorter can be used to linearize several different nonlinear models with memory, which demonstrates the robustness of the SMP predistorter. The PA is assumed to follow an odd-order-only memory polynomial model, a three-branch parallel Wiener model, a Wiener-Hammerstein model and a sparse-delay memory polynomial model, respectively. The coefficients of the first three models are cited from Ref. [2]. In the following simulations, the baseband input is a WCDMA downlink signal with a data rate of 3.84 MHz and a center frequency of 2.14 GHz.

3.1 Example of memory polynomial model

We assume that the PA obeys an odd-order-only memory polynomial model,

$$y(n) = \sum_{\substack{k=1 \\ k\ \mathrm{odd}}}^{K} \sum_{q=0}^{Q} c_{kq} x(n-q) \mid x(n-q) \mid^{k-1} \quad (13)$$

The coefficients are as follows:

$$c_{10} = 1.051\,3 + 0.090\,4\mathrm{i}, \quad c_{30} = -0.054\,2 - 0.290\,0\mathrm{i}$$
$$c_{50} = -0.965\,7 - 0.708\,2\mathrm{i}, \quad c_{11} = -0.068\,0 - 0.002\,3\mathrm{i}$$
$$c_{31} = 0.223\,4 + 0.231\,7\mathrm{i}, \quad c_{51} = -0.245\,1 - 0.373\,5\mathrm{i}$$

$$c_{12} = 0.028\ 9 - 0.005\ 4\mathrm{i},\ c_{32} = -0.062\ 1 - 0.093\ 2\mathrm{i}$$
$$c_{52} = 0.122\ 9 + 0.150\ 8\mathrm{i}$$

The nonlinearity and the memory order of the proposed SMP predistorter is assumed to be

$$\left.\begin{aligned} &Q = 3 \\ &K_0 = 7,\ K_1 = 5,\ K_2 = 3,\ K_3 = 1 \end{aligned}\right\} \tag{14}$$

In the traditional MP predistorter, the maximum nonlinearity order $K = 7$ and the maximum memory order $Q = 3$. Fig. 2 shows the power spectrum density(PSD) when different predistorters are applied. The adjacent channel power ratio(ACPR), the NMSE and the number of coefficients used in different predistorters are listed in Tab. 1. We can see that both the proposed SMP predistorter and the traditional MP predistorter work well. ACPR@ ±5 MHz is improved by 14 dB and 16 dB, respectively. The NMSE of both predistorters are better than −45 dB. Compared with the MP predistorter, the number of coefficients of the SMP predistorter is decreased by 37.5%.

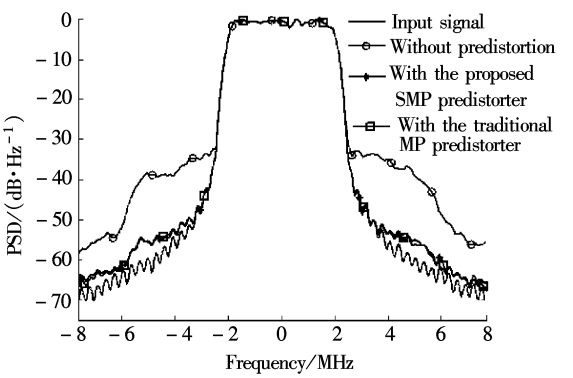

Fig. 2 Simulated power spectrum density for the MP model

Tab. 1 Comparison of linearization performance for the MP model

Predistorter type	ACLR@ ±5 MHz/dBc	e_{NMSE}/dB	Number of coefficients
Without predistorter	−35.38/−33.88		
MP predistorter	−49.82/−49.92	−45.85	16
SMP predistorter	−50.01/−50.16	−45.48	10

3.2 Example of parallel Wiener model

The PA is assumed to follow a three-branch parallel Wiener model(see Fig. 3). The linear time-invariant(LTI) blocks in the model are defined as

$$H_1(z) = 1 \tag{15}$$

$$H_2(z) = \frac{1 + 0.3z^{-1}}{1 - 0.1z^{-1}} \tag{16}$$

$$H_3(z) = \frac{1 - 0.2z^{-1}}{1 - 0.4z^{-1}} \tag{17}$$

The memoryless nonlinearity in the i-th branch has input/output relationship,

$$y_i(n) = \sum_{\substack{k=1 \\ k\ \mathrm{odd}}}^{K} d_{ki} v_i(n) \mid v_i(n) \mid^{k-1} \tag{18}$$

where $v_i(n)$ and $y_i(n)$ are the input and output of the i-th nonlinearity block $F_i(v)$, respectively. The d_{ki} coefficients used are

$$d_{11} = 1.010\ 8 + 0.085\ 8\mathrm{i},\ d_{31} = 0.087\ 9 - 0.158\ 3\mathrm{i}$$
$$d_{51} = -1.099\ 2 - 0.889\ 1\mathrm{i},\ d_{12} = 0.117\ 9 + 0.000\ 4\mathrm{i}$$
$$d_{32} = -0.181\ 8 + 0.039\ 1\mathrm{i},\ d_{52} = 0.168\ 4 + 0.003\ 4\mathrm{i}$$
$$d_{13} = 0.047\ 3 - 0.005\ 8\mathrm{i},\ d_{33} = 0.039\ 5 + 0.028\ 3\mathrm{i}$$
$$d_{53} = -0.101\ 5 - 0.019\ 6\mathrm{i}$$

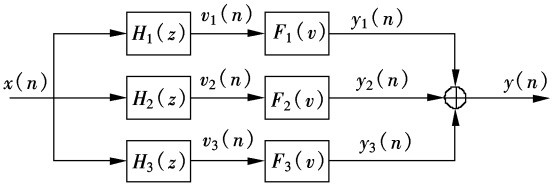

Fig. 3 A three-branch parallel Wiener model

The nonlinearity and the memory order of the SMP predistorter are assumed to be

$$\left.\begin{aligned} &Q = 2 \\ &K_0 = 7,\ K_1 = 5,\ K_2 = 3 \end{aligned}\right\} \tag{19}$$

In the traditional MP predistorter, the maximum nonlinearity order $K = 7$ and the maximum memory order $Q = 2$. Fig. 4 and Tab. 2 show the results. The same conclusion can be drawn that the SMP predistorter performs as well as the memory polynomial predistorter with fewer coefficients. Both predistorters can improve ACPR@ ±5 MHz 14 dB.

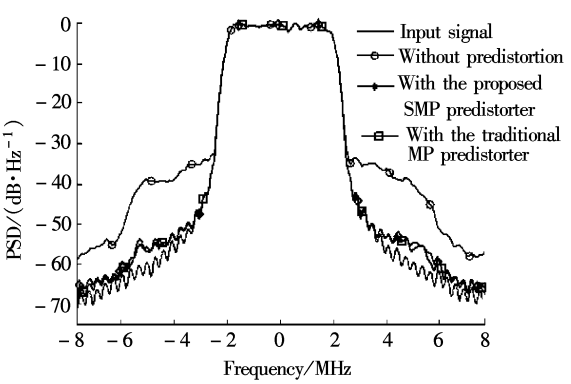

Fig. 4 Simulated power spectrum density for the parallel Wiener model

Tab. 2 Comparison of linearization performance for the parallel Wiener model

Predistorter type	ACPR@ ±5 MHz/dBc	e_{NMSE}/dB	Number of coefficients
Without predistorter	−35.81/−35.34		
MP predistorter	−50.19/−50.06	−46.69	12
SMP predistorter	−50.10/−49.81	−46.94	9

3.3 Example of Wiener-Hammerstein model

The PA is assumed to follow a Wiener-Hammerstein model(see Fig. 5).

$H(z)$ and $G(z)$ are assumed to be

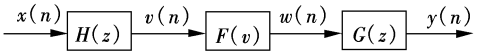

Fig. 5 Wiener-Hammerstein model

$$H(z) = \frac{1 + 0.5z^{-2}}{1 - 0.2z^{-1}} \tag{20}$$

$$G(z) = \frac{1 - 0.1z^{-2}}{1 - 0.4z^{-1}} \tag{21}$$

$v(n)$ and $w(n)$ are the input and output of the memoryless nonlinear block $F(v)$,

$$w(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^{K} b_k v(n) \mid v(n) \mid^{k-1} \tag{22}$$

where $b_1 = 1.010\,8 + 0.085\,8\mathrm{i}$, $b_3 = 0.087\,9 - 0.158\,3\mathrm{i}$, $b_5 = -1.099\,2 - 0.889\,1\mathrm{i}$.

In this example, the maximum nonlinearity order and the memory order of the traditional MP predistorter are assumed to be $K = 11$, $Q = 7$. To obtain better performance, we increase the maximum memory order of the SMP predistorter to $Q = 9$. The corresponding nonlinearity order is assumed to be

$$\left.\begin{aligned} &K_0 = 11,\ K_1 = 9,\ K_2 = 7,\ K_3 = 5,\ K_4 = 3 \\ &K_5 = K_6 = K_7 = K_8 = K_9 = 1 \end{aligned}\right\} \tag{23}$$

Fig. 6 and Tab. 3 show the simulation results when the PA is modeled by the Wiener-Hammerstein model. The results show that both the SMP predistorter and the MP predistorter can improve ACPR@ ±5 MHz 18 dB; the NMSE of both predistorters are better than −44 dB. Compared with the traditional MP predistorter, the proposed SMP predistorter reduces the number of coefficients by 50%.

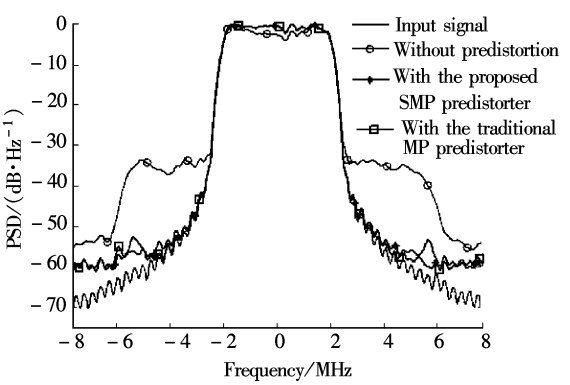

Fig. 6 Simulated power spectrum density for the Wiener-Hammerstein model

Tab. 3 Comparison of linearization performance for the Wiener-Hammerstein model

Predistorter type	ACPR@ ±5 MHz/dBc	e_{NMSE}/dB	Number of coefficients
Without predistorter	−31.76/−31.84		
MP predistorter	−50.23/−49.78	−44.50	48
SMP predistorter	−50.71/−49.88	−44.73	24

3.4 Example of sparse-delay memory polynomial model

The PA is assumed to follow a sparse-delay memory polynomial model[10] that has a transfer function with the form described in Eq. (5) with $K = 3$ and $Q = 3$,

$$y(n) = \sum_{q=0}^{Q} \sum_{k=1}^{K} a_{2k-1,\,q} \mid x(n - d_q) \mid^{2(k-1)} x(n - d_q) \tag{24}$$

The parameters of the given system are as follows:

$$\begin{aligned} &a_{1,0} = 0.98 - 0.3\mathrm{i},\ a_{3,0} = -0.3 + 0.42\mathrm{i},\ d_0 = 0 \\ &a_{1,1} = 0.06 + 0.03\mathrm{i},\ a_{3,1} = -0.02 + 0.05\mathrm{i},\ d_1 = 10 \\ &a_{1,2} = 0.02 + 0.08\mathrm{i},\ a_{3,2} = -0.01 - 0.08\mathrm{i},\ d_2 = 100 \\ &a_{1,3} = -0.01 + 0.02\mathrm{i},\ a_{3,3} = 0.02 - 0.01\mathrm{i},\ d_3 = 50 \end{aligned}$$

In this example, the maximum nonlinearity order and the memory order of the traditional MP predistorter are assumed to be $K = 7$, $Q = 14$. To obtain better performance, we increase the maximum memory order of the SMP predistorter to $Q = 16$. The corresponding nonlinearity order is assumed to be

$$\left.\begin{aligned} &K_0 = 7,\ K_1 = 5,\ K_2 = 3 \\ &K_3 = K_4 = \ldots = K_{16} = 1 \end{aligned}\right\} \tag{25}$$

Fig. 7 and Tab. 4 show the simulation results. Both the SMP predistorter and the MP predistorter can improve ACPR@ ±5 MHz 17dB. However, the NMSE of the SMP predistorter is better than that of the MP predistorter; about 5 dB improvement can be achieved. Compared with the traditional MP predistorter, the proposed SMP predistorter achieves better performance with fewer coefficients. The number of coefficients is reduced by 61.6%.

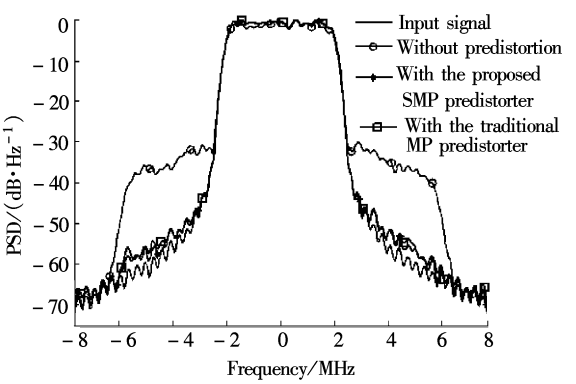

Fig. 7 Simulation power spectrum density for the sparse-delay memory polynomial model

Tab. 4 Comparison of linearization performance for the sparse-delay memory polynomial model

Predistorter type	ACPR@ ±5 MHz/dBc	e_{NMSE}/dB	Number of coefficients
Without predistorter	−32.53/−32.45		
MP predistorter	−49.95/−49.20	−32.24	60
SMP predistorter	−50.25/−49.69	−37.15	23

3.5 Analysis

There are some interesting links between the proposed step memory polynomial model and the memory polynomial model.

For the step memory polynomial model, let $K_i = K_j = K$ $(i, j = 0, 1, \ldots, Q)$, and then the step memory polynomial model becomes the traditional memory polynomial model. In other words, the memory polynomial model is a special case

of the step memory polynomial model.

Compared with the memory polynomial model, the step memory polynomial model divides the input $x(n-q)$ ($q=0,1,\ldots,Q$) into several portions and makes a difference among different portions. By decreasing the maximum nonlinearity order of some portions, the SMP predistorter can efficiently reduce the number of coefficients. When long-term memory effects are considered, the advantages of the SMP predistorter become more evident. Also the good performance on different PA models demonstrates that the SMP predistorter is not tied to a particular PA model and is therefore robust.

4 Measurement Results

Fig. 8 shows a block diagram of the experimental test set-up. The predistortion algorithm is carried out on a PC. The Anritsu signal analyzer MS2691A(including a signal generator and a signal analyzer) is used to generate the predistorted signal and collect the PA response through networking with the PC. The power amplifier under test is fabricated based on the freescale LDMOSFET MRF21030. Experimental steps are as follows:

1) Set the bias voltage of the PA under test, $V_{GS}=3.5$ V, $V_{DD}=28$ V.

2) Generate a pre-defined downlink WCDMA signal and up-convert it to RF at 2.14 GHz by a signal generator.

3) Collect the input(connect the input of PA to signal analyzer through channel A) and output(connect the output of PA to signal analyzer through channel B) of PA without predistortion by a signal analyzer.

4) Compute the predistortion coefficients.

5) Predistort the pre-defined downlink WCDMA signal, and then record the results.

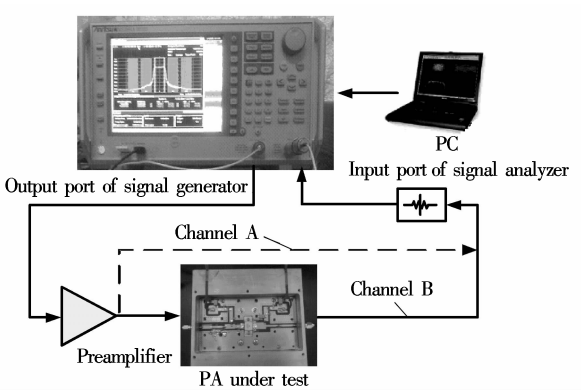

Fig. 8 The measured set-up diagram

Both the traditional memory polynomial predistorter and the proposed SMP predistorter are tested. Fig. 9 shows the output spectrum of the signal when different predistorters are applied. Trace (a) is the power spectrum of the input signal. Trace (b) shows the spectral regrowth of the PA output without predistorter and is seen to be as high as -35 dB relative to the in-band level. Trace (c) shows the output spectrum with the traditional memory polynomial predistorter with nonlinearity order $K=9$ and memory order $Q=5$ delay taps, and trace (d) shows the output spectrum with the proposed SMP predistorter using nonlinearity and memory orders as follows:

$$\left.\begin{array}{l} Q=5 \\ K_0=9,\ K_1=7,\ K_2=5,\ K_3=3,\ K_4=1,\ K_5=1 \end{array}\right\} \quad (26)$$

The measured results as well as the number of coefficients are listed in Tab. 5. The second and third columns are the ACPR measured in the two lower and two upper adjacent channel slots, which are spaced at contiguous 5 MHz intervals. The last column shows the number of coefficients. As can be seen from Fig. 9 and Tab. 5, the proposed SMP predistorter improves the ACPR more than 13 dB as well as the traditional memory polynomial predistorter. The SMP predistorter reduces the number of coefficients by 46%.

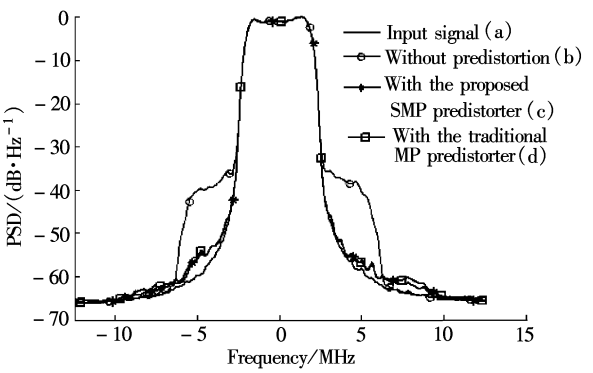

Fig. 9 Measured power spectrum density

Tab. 5 Comparison of linearization performance for real PA

Predistorter type	ACPR/dBc		Number of coefficients
	±5 MHz	±10 MHz	
Without predistorter	−39.66/−38.99	−64.68/−63.97	
With traditional MP predistorter	−52.86/−53.13	−63.87/−62.74	30
With proposed SMP predistorter	−52.83/−53.05	−64.13/−63.15	16

5 Conclusion

In this paper, a step memory polynomial predistorter is proposed and implemented by adopting an offline learning structure. The coefficients of the proposed predistorter can be directly extracted from the sampled input and output of a PA. Several PA models with memory including a memory polynomial model, a parallel Wiener model, a Wiener-Hammerstein model and a sparse-delay memory polynomial model are used in simulation. It is demonstrated that the proposed SMP predistorter is not tied to a particular PA model, and therefore is robust. The effectiveness of the SMP predistorter is validated by not only simulation on different PA models, but also by experiments on a real PA which is fabricated based on the freescale LDMOSFET MRF21030. Simulation and experimental results show that the SMP predistorter can effectively improve the linearization performance. Compared with the traditional memory polynomial predistorter, the SMP predistorter can reduce the number of coefficients by more than 60%.

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用于功率放大器的阶梯记忆多项式预失真器

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摘要: 为了减少数字预失真系数的数量, 提出了阶梯记忆多项式(SMP)预失真器. 该预失真器通过改变传统记忆多项式预失真器中不同记忆深度对应的最大非线性阶数以降低系数数量. SMP 预失真器系数的提取采用离线学习结构, 直接通过功率放大器(PA)的输入、输出采样数据计算预失真系数. 仿真结果表明了 SMP 预失真器的鲁棒性, 它并不局限于某一特定 PA 模型. SMP 预失真器的有效性分别在记忆多项式模型、并行 Wiener 模型、Wiener-Hammerstein 模型、非单位延时记忆多项式模型和基于 Freescale LDMOSFET MRF21030 制作的实际 PA 上, 通过仿真和实验的方式进行了验证. 与传统 MP 预失真器相比, SMP 预失真器可减少系数数量 60% 以上.

关键词: 功率放大器; 预失真; 记忆效应; 记忆多项式
中图分类号: TN72