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A 10 Gb/s laser diode driver in 0.35 μm SiGe BiCMOS technology

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Abstract: This paper discusses the design of a 10 Gb/s laser diode driver implemented in SiGe BiCMOS technology. The laser diode driver is composed of an input buffer, a predriver circuit and an output current switch stage. With the current mode logic (CML) structure, the input buffer and the predriver circuit have the capability of transmission and amplification of high speed data. By employing MOS-HBT cascode structure as the output stage, the laser diode driver exhibits very high speed and efficiency working at the 10 Gb/s data rate. The core circuit is operated under a 3.3 V supply, while the output stage is operated under 5.5 V for sufficient headroom across the laser diode. The chip occupies a die area of 600 μm × 800 μm. Measurements on chip show clear electrical eye diagrams over 10 Gb/s, which can well meet the specifications defined by SDH STM64/SONET OC192 and a 10 Gb/s Ethernet eye mask. Under a 5.5 V supply voltage, the maximum output swing is 3.0 V with a 50 Ω load (the corresponding modulation current is 60 mA), and the total power dissipation is 660 mW.

Key words: laser diode driver; MOS-HBT cascode; SiGe BiCMOS technology

The rapidly growing volume of data exchange in telecommunication networks has recently drawn considerable attention to the design of ultra high speed circuits for optical communications. The laser diode driver circuit as a key part of optical communications has become a hot research topic. Recently, some research on the 10 Gb/s laser diode driver in SiGe BiCMOS technology has exhibited high performance and power efficiency[1-2]; however, having self-owned intellectual rights for ultra-high speed laser diode drivers of optical communications will accelerate the construction of optical fiber networks and the development of information highways in China.

The design of a high performance laser diode driver is very challenging, mainly due to its requirements of high speed and large output current[3]. Meanwhile, large output current means that large transistors and large driving signals should be necessary. Moreover, a large output current across a resistor brings high voltage, which indicates that we need high breakdown voltage transistors; unfortunately, high breakdown voltage transistors usually have a lower cut-off frequency[4], which also makes our design more difficult.

The laser diode driver architecture is shown in Fig. 1. It consists of two parts, a very high speed laser diode driver circuit providing modulation current and a bias network including devices for AC coupling and a DC bias current. The laser diode driver circuit is composed of an input buffer, a two stage predriver circuit and an MOS-HBT cascode output switch stage. The core part of the circuit is operated under a 3.3 V (V_{DD}) supply, while the output stage works at a 5.5 V (V_{CC}) supply for a sufficient swing voltage across the laser diode. In this design, cascade stages using differential pair amplifiers with degenerated resistors are implemented for the predriver to provide a high speed signal. To reduce the huge input capacitance of the output transistor and maximize the speed, we use the MOS-HBT cascode structure[5] as the output switch stage. There is also a PTAT bias circuit to compensate the temperature variation.

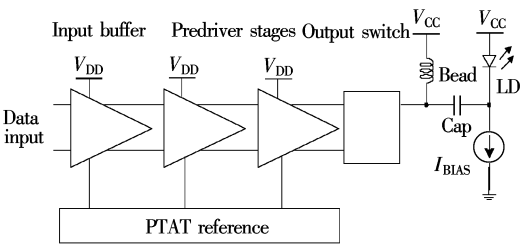

Fig. 1 Laser diode driver architecture

1 Circuit Implementation

1.1 Predriver

Fig. 2 shows the predriver circuit. Two stages are cascaded for high speed driver capability. Each stage is composed of a differential pair amplifier and an emitter follower buffer. The local feedback (emitter degeneration) is employed in a differential pair amplifier. Small signal analysis shows that the equivalent capacitance seen from the input port of the differential amplifier is reduced by $1 + g_m R_E$ but at the expense of gain reduction. The buffer exhibits small output impedance to enhance high speed capability.

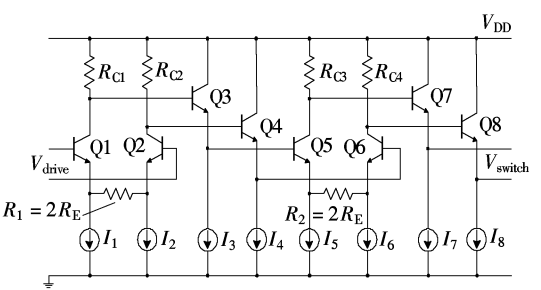

Fig. 2 Predriver stages

To keep minimum overshoot and switching times, the output swing of the predriver should be kept constant to drive the output stage. Therefore, the second differential pair amplifier works as a limited amplifier.

The voltage swing at the input of the second differential

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pair amplifier is determined by the tail current of the first stage circuit and load resistors. An optimum trade-off between rise/fall time and overshoot/undershoot is achieved using a driving voltage amplitude of $V_s = (4 \sim 5)\, V_T + 2I_{tail}\, R_E$, where V_T is the thermal voltage and it is about 26 mV at room temperature, I_{tail} is the bias current, and R_E is the emitter resistor. PTAT DC current reference is provided for all current sources in Fig. 2 which can alleviate rise/fall time variations over temperature.

1.2 MOS-HBT cascode structure

The high modulation current(up to 60 mA) requires large devices for output stages, resulting in a huge capacitance. This capacitance is multiplied by the Miller effect, which loads the predriver heavily and also increases the rise/fall time. In order to reduce the huge capacitance caused by the Miller effect, cascode topology is usually used to alleviate the Miller effect. There exist four cascode configurations: MOS-MOS, MOS-HBT, HBT-MOS, and HBT-HBT available in a SiGe BiCMOS technology. The MOS-MOS and HBT-HBT cascodes are perhaps the most widely used, but the MOS-HBT cascode can show better performance in high speed design. The MOS-HBT cascode of Fig. 3 employs an NMOS common-source amplifier followed by an HBT in the common base configuration. This configuration has been used previously in lower frequency analog circuits[6]. Recently, its high frequency application has been explored, showing very high performance characteristics[5].

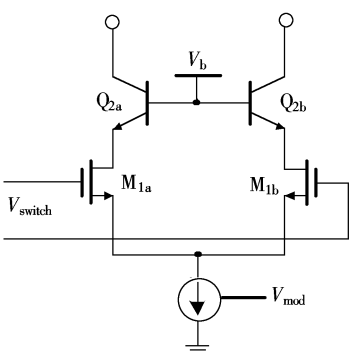

Fig. 3 MOS-HBT cascode

The -3 dB bandwidth of cascode structure estimated by the open circuit time constant is

$$\frac{1}{2\pi f_{-3\mathrm{dB,\,cascode}}} \approx (R_s + R_{g/b}) \left[C_{1gs/be} + \left(1 + \frac{g_{m2}}{g_{m1}}\right) C_{1gd/cb} \right] + R_L (C_{2gb/bc} + C_{j2}) + \frac{1}{g_{m2}} C_{2gs/be}$$

where R_s is the source resistance, and C_{j2} is the junction capacitance at the output. The first term of the formula accounts for the input node time constant. The second and third terms represent the output and intermediate time constants, respectively. The NMOS gate resistance R_g can be made negligible by connecting multiple fingers in parallel. Moreover, this does not affect C_{gs} to be a first-order analysis, since the total gate area remains unchanged. In contrast, increasing the emitter length of the SiGe HBT can reduce the base resistance R_b, but at the expense of increased base-to-emitter capacitance. The output time constant is lower due to the HBT being the common base output stage[7]. The intermediate time constant is mainly determined by the top transistor, indicating that the use of a SiGe HBT as a common base stage is preferable.

1.3 PTAT reference

Fig. 4 shows the detail schematic of PTAT current reference. It gives a self-biased, supply-independent current with the well known equation $I_o = V_T/R\ln(n)$. Obviously, thermal voltage V_T is proportional to temperature and so is the output current. Besides, to reduce the effects of interconnect resistance and make the current mirror more robust, the reference current is distributed in the current domain rather than in the voltage domain.

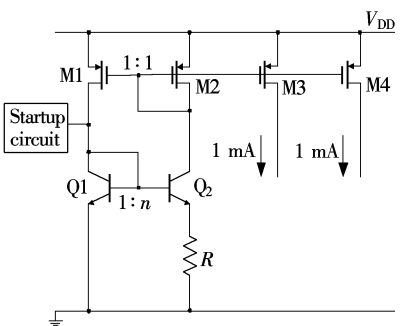

Fig. 4 PTAT reference

2 Fabrication and Experimental Results

This chip is fabricated in Jazz 0.35 μm SiGe BiCMOS technology. The chip photograph is shown in Fig. 5. The chip dimension is 600 μm × 800 μm which is very area-efficient. To reduce mismatch, symmetric layout is necessary. For high frequency design, the layout parasitic affects the performance significantly. The high frequency signals interconnection between adjacent blocks are designed as close as possible and put on the top layer metal when long interconnection is unavoidable. For the connections between output switch stage and its driving emitter follower buffers, the transistors are always of a large size in order to offer high driving ability. The NMOS transistor for the MOS-HBT is implemented in as many figures as possible to reduce gate resistance significantly but the width of NMOS should be larger than 2 μm to keep its high frequency performance; otherwise, its f_T will deteriorate[8]. For the last stage emitter follower buffer, its output resistor is very small owing to its

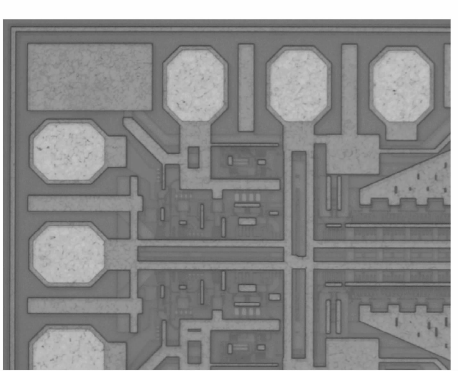

Fig. 5 Chip photograph of LDD driver

large current. Therefore, the main parasitic is due to the inductance parasitic[9]. To reduce the overshoot, the interconnection between the last emitter follower and the output switch stage should be designed wide and short to lower parasitic inductance.

This driver is tested on-wafer in the setup shown in Fig. 6. Owing to the open collector structure of the laser diode driver, two bias-tees are employed to provide DC bias to the output stage. The laser diode is simulated by a 50 Ω resistor, which is the input resistor of the oscilloscope.

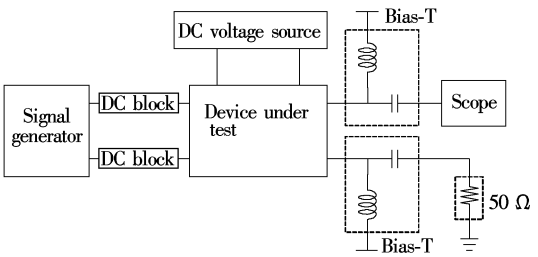

Fig. 6 On-wafer experimental setup

Fig. 7 is the resulting measured eye diagram. The input signal is a $2^{31}-1$ bit PRBS NRZ signal at 10 Gb/s with a 0.6 Vpp amplitude. The amplitude of the single-ended output is 3 Vpp at a 50 Ω load corresponding to the output current of 60 mA. The rise/fall time is about 45 ps. The deterministic jitter and rms jitter are 16.9 and 2.85 ps, respectively. The predriver costs about 100 mA current from a 3.3 V supply and the output stage drains 60 mA from a 5.5 V bias voltage. Therefore, the total power dissipation is 660 mW; however, power dissipation in Ref. [2] is 1.38 W.

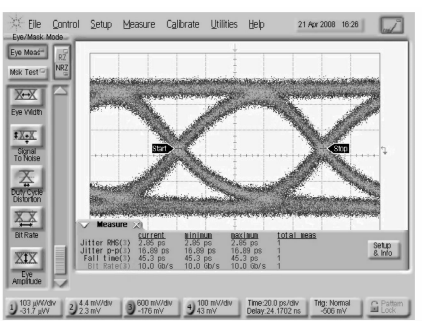

Fig. 7 Measured eye diagrams(I_{mod} = 60 mA at 10 Gb/s)

Fig. 8 and Fig. 9 show that, with 60 mA modulation current, the eye-opening meets the transition mask required by SDH STM64/SONET OC192 and 10 Gb/s Ethernet specifications.

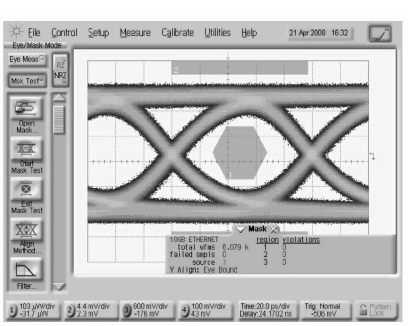

Fig. 8 Measured eye diagrams with 10 Gb/s Ethernet mask

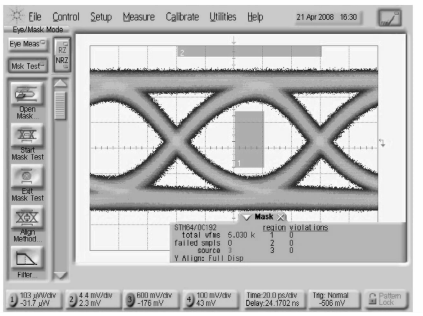

Fig. 9 Measured eye diagrams with STM64/OC192 mask

3 Conclusion

In this paper, a 10 Gb/s laser diode driver for optical communication systems is presented. The chip is fabricated in Jazz 0.35 μm SiGe BiCMOS technology and the die area is 600 μm × 800 μm. The measured eye diagrams show good characteristics at 10 Gb/s, which shows the advantage of the MOS-HBT cascode structure in BiCMOS technology.

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0.35 μm SiGe BiCMOS 10 Gb/s 激光驱动芯片设计

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摘要：讨论一款基于 SiGe BiCMOS 工艺工作速率为 10 Gb/s 激光驱动芯片的设计. 该激光驱动芯片包括输入缓冲、驱动放大电路和输出级电路 3 个部分. 输入缓冲、驱动放大电路采用电流模电路，满足高速数据传输和放大的能力，输出级电路结构采用新型的 MOS-HBT 共源共栅结构可以降低米勒效应减小输入电容，从而使激光驱动芯片工作在 10 Gb/s 时也能达到良好的性能. 主电路电源电压为 3.3 V，输出级电路供电电压为 5.5 V，确保激光器有足够的电压摆幅. 芯片总面积（包括焊盘）为 600 μm × 800 μm，，测试表明当输入 10 Gb/s 的非归零随机码，输出级电源电压为 5.5 V 时，电路总功耗为 660 mW，在 50 Ω 负载上可以提供 3 V 的驱动电压（相应的驱动电流为 60 mA）. 测试眼图清晰，可以很好地满足 SDH STM64/SONNET OC192 和 10 Gb/s 以太网的模板要求.

关键词：激光驱动芯片；MOS-HBT 结构；锗硅 BiCMOS 工艺

中图分类号：TN722