Journal of Southeast University (English Edition) Vol. 25, No. 3, pp. 367 - 371 Sept. 2009 ISSN 1003—7985

Integrated power electronics module based on chip scale packaged power devices

Wang Jiangang[1,2] Ruan Xinbo[2]

([1]College of Electrical Engineering, Yancheng Institute of Technology, Yancheng 224051, China)
([2]College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China)

Abstract: High performance can be obtained for the integrated power electronics module (IPEM) by using a three-dimensional packaging structure instead of a planar structure. A three-dimensional packaged half bridge-IPEM (HB-IPEM), consisting of two chip scale packaged MOSFETs and the corresponding gate driver and protection circuits, is fabricated at the laboratory. The reliability of the IPEM is controlled from the shape design of solder joints and the control of assembly process parameters. The parasitic parameters are extracted using Agilent 4395A impedance analyzer for building the parasitic parameter model of the HB-IPEM. A 12 V/3 A output synchronous rectifier Buck converter using the HB-IPEM is built to test the electrical performance of the HB-IPEM. Low voltage spikes on two MOSFETs illustrate that the three-dimensional package of the HB-IPEM can decrease parasitic inductance. Temperature distribution simulation results of the HB-IPEM using FLOTHERM are given. Heat dissipation of the solder joints makes the peak junction temperature of the chip drop obviously. The package realizes three-dimensional heat dissipation and has better thermal management.

Key words: integrated power electronics module; chip scale package; reliability; parasitic parameter; thermal management

To realize high power density, high efficiency, high reliability and low cost power electronics system, the power electronics system integration is considered to be the best approach[1]. In the power electronics integrated system, discrete parts are replaced by standardized units, namely integrated power electronics modules (IPEMs), which have standard power, thermal and control interfaces. Intelligent and reconfigurable IPEMs make it easy to develop multitudes of affordable, reliable, and efficient integrated systems.

The package technology is an important part of power electronics system integration, which provides mechanical support to the fragile chip, electrical interconnections, heat dissipation paths and protection from the environment and impacts on electrical, electromagnetic interference (EMI) and thermal characteristics of the module. At present, the wire-bonding interconnection technique and the two-dimensional packaging structure are commonly used in power modules due to the large installed base, available engineering resource and the maturity of the process. But wire bonds are prone to electrical overstressing, large mutual coupling effects, parasitic oscillations, and mechanical damage from the ultrasonic bonding of large-diameter wires, and the two-dimensional packaging structure has limited the heat-dissipation capability[2]. In order to improve electrical and thermal performance and reduce the package size, a complete shift in the design paradigm for packaging is expected. The Center for Power Electronics System (CPES) presents a three-dimensional packaging concept for constructing the IPEM[3]. In the IPEM, power chips and the three-dimensional structure are employed. Wire-bonding is replaced by the wire-bondless interconnection technique.

Several three-dimensional packaging approaches such as thin-film power overlay technology, metal posts interconnection technology, dimple array interconnect technology and low-temperature sintered technology for constructing the IPEM have been developed. The layouts, electrical and thermal performance of IPEMs are analyzed extensively[4-9].

The construction of the three-dimensional active IPEM based on chip scale packaged (CSP) power devices is illustrated in this paper. The reliability of the IPEM is controlled from the shape design of solder joints and the control of assembly process parameters. The electrical parasitic parameter model of the IPEM is built and electrical performance test results are included. Temperature distribution simulation results of the IPEM are given.

1 Construction of IPEM

1.1 Circuit

The phase leg composed of two active switches and a diode anti-parallel with each of them is a standard switching cell in common use. This half bridge (HB) switching leg and its corresponding driver and protection circuits are selected to illustrate the construction of the active IPEM.

The circuit diagram of the HB-IPEM is shown in Fig. 1. The HB-IPEM has three power input/output terminals: P (positive terminal of DC bus), N (negative terminal of DC bus) and O (AC terminal). C_1 is the DC bus snubber capacitor. Q_1 and Q_2 are two MOSFETs. The HIP2100 is a high frequency, 100 V HB N-channel power MOSFET driver IC with independent high and low side referenced output channels. Pin 5 and Pin 6 are the high side and low side logic input terminals, respectively. Pin 3 and Pin 8 are the high

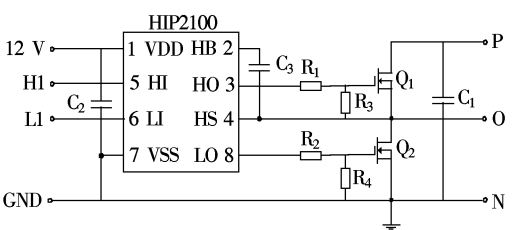

Fig. 1 Schematic circuit diagram of the HB-IPEM

Received 2008-12-30.

Biography: Wang Jiangang (1968—), female, doctor, associate professor, wangjg@ycit.cn.

Foundation items: Fok Ying Tung Education Foundation (No. 91058), the Natural Science Foundation of High Education Institutions of Jiangsu Province (No. 08KJD470004), Qing Lan Project of Jiangsu Province of 2008.

Citation: Wang Jiangang, Ruan Xinbo. Integrated power electronics module based on chip scale packaged power devices[J]. Journal of Southeast University (English Edition), 2009, 25(3): 367 - 371.

side and low side output terminals to provide gate drive signals for Q_1 and Q_2, respectively. C_2 is the logic supply snubber capacitor. C_3 and an on-chip diode are employed to form a bootstrap supply circuit for the high-side driver. R_1 to R_4 are gate driver resistors.

1.2 CSP power devices

To qualify as a chip scale, the package must have an area no greater than 1.2 times that of the die that is being packaged and it has to be a single-die, direct surface mountable package. Another criterion is that its ball pitch should be no more than 1 mm. CSP can be in many forms: flip chip, non flip chip, wire-bonded, ball grid array(BGA), leaded, etc. A CSP device is commonly referred to as a chip[10].

The two CSP MOSFETs (FDZ3547N) are employed in the HB-IPEM. FDZ3547N has a typical MOSFET BGA package. The area of the device is 5.5 mm × 5 mm and the height is 0.9 mm. The device consists of a bumped die assembled in a cavity-based carrier lead-frame, which is also bumped with the same sized solder balls. The metallic lead-frame covers the back and sides of the die. This construction allows the drain terminal of the MOSFET(which is the backside of the die) to be brought to the same plane as the gate and the source through the bumps on the lead-frame. The solder balls are eutectic solders (Sn63/Pb37) with a melting temperature of 183 ℃. The diameter of the solder balls is 0.4 mm.

1.3 Package structure

The cross section of the package structure of the HB-IPEM is illustrated in Fig. 2. The power chips(CSP MOSFETs) are sandwiched between the substrate of the high thermal conductivity(bottom layer) and the double-sided printed circuit board(PCB)(top layer). The active sides of the power chips are flip-chip bonded to the PCB using solder bumps. The back of the power chips is soldered to the bottom substrate. Underfill is used to fill the gap between the silicon chip and the substrate around the solder joints to match coefficients of thermal expansion(CTE) of the substrate and the chips. Thermally conductive encapsulation material is mainly used to improve thermal management. Driver, control and protection circuit components are built on the top of the PCB using either surface mounting or flip-chip technology.

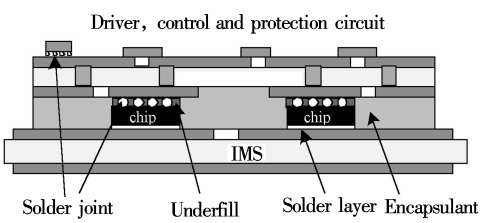

Fig. 2 Schematic structure of the HB-IPEM

An HB-IPEM consisting of two CSP MOSFETs and gate driver and protection circuits is fabricated in our lab. The materials of the HB-IPEM include: 1) CSP MOSFET (FDZ3547N, 80 V/12.5 A); 2) FR-4 substrate(top substrate); 3) Al based insulated metal substrate(IMS)(bottom substrate). Fig. 3 is the prototype HB-IPEM. The size of the bottom substrate is 50 mm × 50 mm.

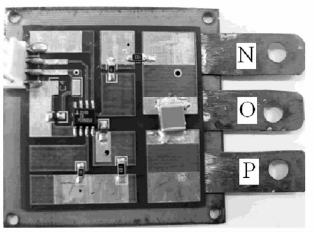

Fig. 3 The HB-IPEM based on CSP MOSFETs

2 Reliability Control of IPEM

2.1 Optimum design of solder joint

The electrical and mechanical interconnections of different materials(chips and substrates) are accomplished by solder joints in the HB-IPEM. The reliability of module depends on the ones of the solder joints to a great extent[11].

2.1.1 Impact of shape on solder joint lifetime

Thermally induced stresses are the main reliability issues for flip-chip interconnections. One of the major sources of thermal stresses is the global CTE mismatch between the silicon chip and the substrate. The other major source is the local CTE mismatch between the silicon chip, solder bump, underfill, encapsulant, and substrate. The global CTE mismatch causes high shear strain in the solder bump interconnection during thermal cycling. The distance from the solder joint to the neutral expansion point increases, the strain imposed on the solder joints increases. The shear strain Δ_γ can be estimated by the following simplified expression:

$$\Delta_\gamma = \Delta\alpha \Delta T \frac{d}{h} \tag{1}$$

where $\Delta\alpha$ is the difference in the CTE between the joined materials; ΔT is the temperature change; d is the distance from the neutral expansion point of the joined materials; and h is the height of the solder joints. The shear strain Δ_γ of the solder joints includes elastic strain and plastic strain. But the elastic strain is much smaller than the plastic strain.

The Coffin-Manson equation is a widely used relationship to predict the solder joint fatigue lifetime,

$$N_f = \theta(\Delta\gamma_p)^{-\phi} \tag{2}$$

where N_f is the number of cycles to failure; $\Delta\gamma_p$ is the plastic strain range, and θ and ϕ are material constants. For solder joints(Sn63/Pb37), $\theta = 1.292\,8$, $\phi = 1.96$.

For FDZ3547N, which is used in the HB-IPEM, d = 2.28 mm and h is about 0.23 mm. The difference in the CTE between the silicon chip and the PCB is 9.2×10^{-6}/℃. Assuming the highest module temperature is 65 ℃ and the room temperature is 35 ℃, then the temperature change is ΔT = 30 ℃ and the shear strain Δ_γ of 0.273 6% is caused. An average life of the module is about 1.364×10^5 cycles.

2.1.2 Employment of solder paste pre-overlaying on PCB solder pad

Assume that the solder bump volume of CSP chips is V_1 and the volume of solder paste which is pre-overlaid on each solder pad of the PCB is V_2, and the volume of the solder joint is $V = V_1 + V_2$ after reflowing. Keeping the radius b of the solder pad on the chip and the PCB constant, while increasing V_2, h increases, and the thermal stress caused by

the global CTE mismatch between the silicon chip and the substrate decreases.

The contact angle of the solder joint is

$$\beta = \frac{\pi}{2} - \arctan\left(\frac{h/2}{b}\right) \tag{3}$$

β decreases while the volume of the solder paste increases. High solder joints make the thermal stresses caused by local CTE mismatch decrease.

Assuming that $V_2 = V_1$, $h = 0.357$ mm, the shear strain $\Delta\gamma$ of 0.176% is caused. The average life of the module is about 3.238×10^5 cycles. The lifetime of the module is increased.

Employment of solder paste pre-overlaying on the PCB solder pad can help to optimize the shape of the solder joints and improve the reliability of the module.

2.2 Control of package assembly

2.2.1 Temperature hierarchy of solder

In the HB-IPEM package assembly, a typical manufacturing consideration is to maintain a temperature hierarchy, where processes occur in the order of decreasing process temperature. Each subsequent soldering process occurs at a lower temperature to avoid damage to previously completed solder joints. The solders used in the HB-IPEM are shown in Tab. 1. Their melting points and functions are also given.

Tab. 1 Solders and their melting points

Solder	Melting point/℃	Function
Sn95/Ag5	221	Power terminal soldering on IMS
Sn63/Pb37	183	Flip chip bonding on PCB
Sn43/Pb43/Bi14	163	Attaching PCB to IMS
Sn43/Bi57	135	Soldering components on PCB

2.2.2 Flux

In order to remove metal oxides and promote wetting of the solders when the assembly is heated above the temperature of the solder, flux is needed. No-clean flux is a preferable choice for the HB-IPEM package assembly.

2.2.3 Setting of reflow temperature profile

A reflow temperature profile must enable reflow soldering temperature changes smoothly. The PCB can be double-sided heated and the chips can be heated uniformly while they are undergoing reflow. To test the solder pads temperature in real time, SlimKIC 2000 is used. The temperature curves of the solder pads are shown in Fig. 4. The curves match the requirements of reflow soldering for the chip on the PCB well.

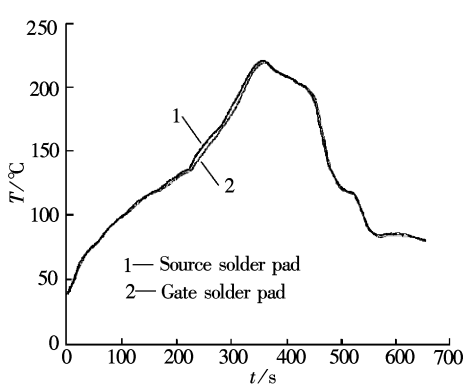

Fig. 4 Temperature curves of the solder pads in real time

3 Parasitic Parameter Model of HB-IPEM

In order to analyze the EMI and test the electrical performances of the HB-IPEM, a synchronous rectifier Buck converter using the HB-IPEM is built. The parameters of the converter are: $V_{in} = 42$ V; $V_o = 12$ V; $I_o = 3$ A; switching frequency $f_s = 105$ kHz. L_f and C_f are the inductor and the capacitor of the output filter, respectively.

3.1 EMI path

Because of fast switching, EMIs generate in IPEMs. EMI issue has become a very challenging design task for IPEMs.

The EMI paths of a synchronous rectifier Buck converter using HB-IPEM are shown in Fig. 5. LISN is a device to create known impedance on power lines of electrical equipment during EMI testing. As far as the HB-IPEM is concerned, the parasitic inductances of the traces will affect the differential-mode(DM) noise, and the parasitic capacitances C_O between the Cu trace connected with the O output terminal and the Al layer of IMS will account for the common-mode(CM) noise[12].

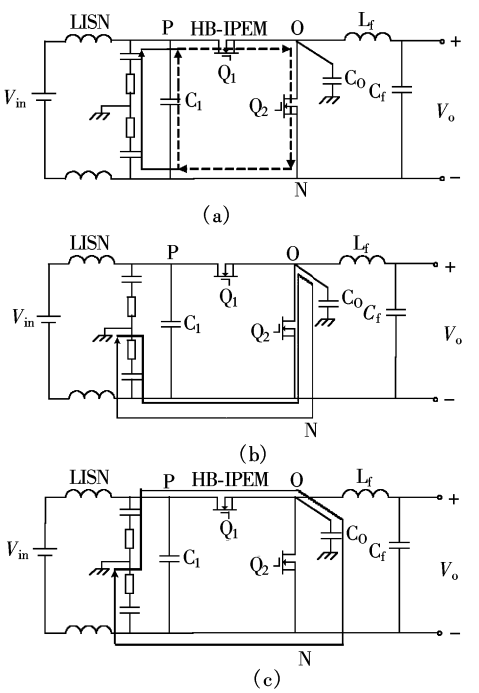

Fig. 5 EMI paths of synchronous rectifier Buck converter using the HB-IPEM. (a) DM EMI path; (b) CM EMI path 1; (c) CM EMI path 2

3.2 Parasitic parameter model

The parasitic parameters of the HB-IPEM are extracted using the Agilent 4395A Network/Spectrum/Impedance analyzer. Impedance measurement is simple and straightforward. For a better illustration of the characterization process, the HB-IPEM under measurement is the case where the gate driver is not incorporated. The parasitic parameter model of the HB-IPEM is shown in Fig. 6.

The parasitic inductance values for the HB-IPEM are less than the order of 10 nH, and they are closer to those of the TO-247 packaged devices. The thin dielectric layer of Al based insulated metal substrate brings about great parasitic

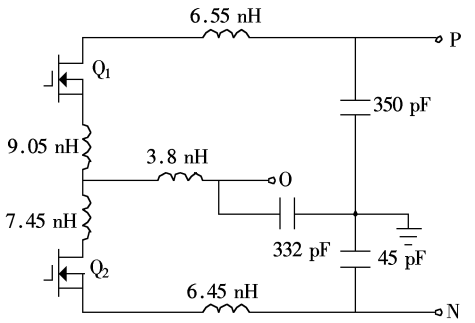

Fig. 6 Parasitic parameter model of the HB-IPEM

capacitances. The CM noises occur when the HB-IPEM operates. EMI filters or anti-phase techniques can be employed to suppress the CM noises.

3.3 Electrical testing results

Fig. 7 shows the experimental results at full load. Fig. 7 shows the voltage across the drain and source of Q_1 and Q_2, respectively, and the output filter inductance current i_{Lf}. From Fig. 7, we can see that the synchronous rectifier Buck converter using HB-IPEM works well. Low voltage spikes on Q_1 and Q_2 illustrate that the three-dimensional package of the HB-IPEM can decrease parasitic inductance.

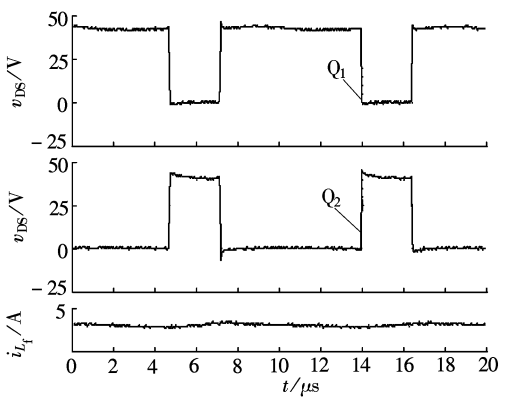

Fig. 7 Experimental results at full load

4 Thermal Management of IPEM

Tightened IPEM brings about a prominent issue: heat dissipation. Thermal management should be set out from: 1) Reducing the loss of the devices; 2) Reducing the thermal resistance of the heat transfer path. Employing appropriate topology and devices can reduce the loss of the IPEM. Once they are determined, the main work of thermal management is to select the materials and design the heat transfer path.

4.1 Selection of materials

The HB-IPEM contains several materials with different properties. Superior thermal management requires the availability of materials with high thermal conductivity and thermal capacitance.

Heat from the module is mainly dissipated by the bottom substrate. The important factors in the selection of substrate are thermal conductivity and CTE. The bottom substrate usually uses IMS or direct bonded copper substrate. The commonly used IMS is Al based. Underfill is used to relax the thermal stress over the surface of the chip. The CTE of the underfill must match that of the solder as closely as possible. The cure temperature must be lower than the melting point of the solder joints. Thermally conductive encapsulation material fills the gap between IMS and the PCB to improve thermal management. Encapsulation material must be of high thermal conductivity and definite mechanical intension.

4.2 Heat transfer path of IPEM

The primary heat transfer path is stated as follows. Heat which is generated from the active side (ball) of the chip flows from the silicon chip through the solder paste to IMS by conduction. Heat is then removed by natural air convection or radiation. A secondary heat flow path exists by conduction in parallel, through the solder joints and underfill to the PCB, and heat is then removed by natural air convection or radiation. Additionally, thermally conductive encapsulation material is used.

4.3 Thermal analysis of IPEM

In order to evaluate the thermal performance of the HB-IPEM, loss distribution of power chips must be evaluated. Q_2 can realize ZVS when the synchronous rectifier Buck converter using the HB-IPEM operates in continuous current mode. The two chips dissipate a total power of 1.157 W at full load: 0.658 W for Q_1 and 0.499 W for Q_2.

Temperature distribution of the HB-IPEM is simulated using FLOTHERM. The simulation conditions are listed as follows: 1) The room temperature is 35 ℃; 2) The HB-IPEM is cooled by natural air convection and with no heat sink; 3) Solder voids are ignored. The three-dimensional thermal model is built and temperature distribution simulation results are shown in Fig. 8. The peak junction temperature of the chip is 59.719 ℃. The junction temperature can drop 3.5 ℃ through the solder joints from which heat is extracted to the PCB. This indicates that the three-dimensional package can improve the thermal performance of the HB-IPEM.

Al based IMS is a key material which impacts on the thermal performance of the HB-IPEM. For the Al layer of IMS, with an increase in thickness from 0.5 to 2 mm, the junction temperature of Q_1 drops by 2.569 ℃. For the insulator layer of IMS, with an increase in thermal conductivity from 0.5 to 4.0 W/mK, the junction temperature of Q_1 drops by 0.771 ℃ and with an increase in thickness from 0.5 to 1.5 mm, the junction temperature of Q_1 drops by 0.499 ℃. The growing trends become weaker as the thermal conductivity

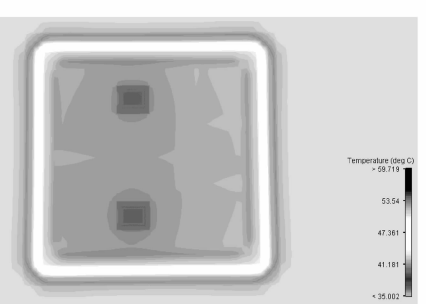

Fig. 8 Temperature distribution simulation map of the HB-IPEM

and the thickness of the insulator layer increase. The area of the Cu layer which connects to power output terminals "O" increases from 36 to 740 mm^2; the junction temperature of Q_2 drops by 0.226 ℃. The junction temperature of Q_2 increases slightly when the area exceeds 250 mm^2. The analyses above provide the design strategies that optimize the thermal performance of the HB-IPEM.

5 Conclusion

CSP power devices have the same or somewhat larger areas than those of the dies, and they have short and thick solder bumps. They enable the construction of a high power density, high efficiency and high reliability IPEM. An HB-IPEM consisting of two CSP MOSFETs and gate driver & protection circuits is fabricated by the flip-chip technology at the laboratory. In the HB-IPEM, the CSP chips are bonded to the substrate by solder bumps. The traditional wire bonding interconnection is eliminated completely. Chips are encapsulated to form a robust package. The reliability of the HB-IPEM is controlled from: 1) The method of solder paste pre-overlaying on the PCB solder pad is applied to raise the fatigue lifetime of the solder joints; 2) Assembly process parameters are elaborately controlled to raise the soldering quality. The parasitic parameters are extracted for building the parasitic parameter model of the IPEM, and excellent electrical performance is proved by the experimental results of a synchronous rectifier Buck converter using the HB-IPEM. Temperature distribution simulation results of the HB-IPEM using FLOTHERM show that the three-dimensional package offers better thermal management.

References

[1] Van Wyk J D, Lee Fred C. Power electronics technology at the dawn of the new millennium — status and future [C]// *IEEE Power Electronics Specialists Conference*. Charleston, South Carolina, USA, 1999: 3 - 12.

[2] Xing Kun, Lee Fred C, Borojevic Dushan. Extraction of parasitics within wire-bond IGBT modules [C]//*IEEE Applied Power Electronics Conference*. Anaheim, California, USA, 1998: 497 - 503.

[3] Lu Guo-Quan, Liu Xingsheng. Application of solderable devices for assembling three-dimensional power electronics modules [C]//*IEEE Power Electronics Specialists Conference*. Galway, Ireland, 2000: 1261 - 1266.

[4] Haque Shatil, Xing Kun, Lin Ray-Lee, et al. An innovative technique for packaging power electronic building blocks using metal posts interconnected parallel plate structures [J]. *IEEE Transactions on Advanced Packaging*, 1999, **22**(2): 136 - 144.

[5] Bai John G, Lu Guo-Quan, Liu Xingsheng. Flip-chip on flex integrated power electronics modules for high-density power integration [J]. *IEEE Transactions on Advanced Packaging*, 2003, **26**(1): 54 - 59.

[6] Wen Simon S, Huff Daniel, Lu Guo-Quan. Dimple-array interconnect technique for packaging power semiconductor devices and modules [C]//*IEEE International Symposium on Power Semiconductor Devices & ICs*. Osaka, Japan, 2001: 69 - 74.

[7] Bai John G, Zhang Zhiye, Calata Jesus N, et al. Low-temperature sintered nanoscale silver as a novel semiconductor device-metalized substrate interconnect material [J]. *IEEE Transactions on Component Packaging Technology*, 2006, **29**(3): 589 - 593.

[8] Chen Qiaoliang, Yang Xu, Wang Zhaoan, et al. Thermal design considerations for integrated power electronics modules based on temperature distribution cases study [C]// *IEEE Power Electronics Specialists Conference*. Orlando, Florida, USA, 2007: 1029 - 1035.

[9] Yin Jian. High temperature SiC embedded chip module (ECM) with double-sided metallization structure [D]. Blacksburg, USA: Virginia Polytechnic Institute and State University, 2005.

[10] Fairchildsemi Corporation. Advanced packaging product [EB/OL]. (2004-04-30)[2008-08-18]. http: //www. fairchildsemi. com/products/discrete/adv_pkg. html.

[11] Liu Xingsheng, Haque Shatil, Lu Guo-Quan. Three-dimensional flip-chip on flex packaging for power electronics applications [J]. *IEEE Transactions on Advanced Packaging*, 2001, **24**(1): 1 - 9.

[12] Lu Bing, Lu Zhiguo, Yang Liyu, et al. IPEM based high frequency PFC [C]//*IEEE Applied Power Electronic Conference*. Anaheim, California, USA, 2004: 1200 - 1205.

基于芯片尺寸封装功率器件的集成电力电子模块

王建冈[1,2]　　阮新波[2]

([1] 盐城工学院电气工程学院, 盐城 224051)

([2] 南京航空航天大学自动化学院, 南京 210016)

摘要: 采用三维封装结构取代传统的平面封装结构可获得高性能集成电力电子模块. 在实验室完成由 2 只芯片尺寸封装 MOSFET 和驱动、保护等电路构成的三维封装半桥 IPEM. 从互连焊点形状的优化和封装工艺过程参数的控制出发,进行 IPEM 的可靠性控制. 采用阻抗分析仪 Agilent 4395A 测量 IPEM 的寄生参数,建立了半桥 IPEM 的寄生参数模型;采用半桥 IPEM 构成 12V/3A 输出的同步整流 Buck 变换器,2 只 MOSFET 的漏源极尖峰电压小,说明 HB-IPEM 的三维封装结构有效减小了寄生电感. 运用 Flotherm 软件对半桥 IPEM 进行了热分析,给出了温度分布仿真结果. 焊料凸点传热使芯片的最高结温明显降低,三维封装结构实现了良好的热设计.

关键词: 集成电力电子模块; 芯片尺寸封装; 可靠性; 寄生参数; 热设计

中图分类号: TM461