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A 5-GHz frequency synthesizer with constant bandwidth for low IF ZigBee transceiver applications

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Abstract: A fully integrated integer-N frequency synthesizer is implemented. The synthesizer is designed for low intermediate frequency (IF) ZigBee transceiver applications. Techniques used to make the loop bandwidth constant across the whole output frequency range of the voltage controlled oscillator (VCO) are adopted to maintain phase noise optimization and loop stability. In-phase and quadrature (IQ) signals are generated by a 1/2 frequency divider at the output of the VCO. The synthesizer is fabricated in 0.18 μm radio frequency(RF) complementary metal oxide semiconductor transistor (CMOS) technology. The chip area is 1.7 mm^2. The synthesizer is measured on wafer. It consumes totally 28.8 mW excluding output buffers from a supply voltage of 1.8 V. The measured phase noise is −110 and −122 dBc/Hz at the offset of 1 and 3 MHz from a 2.405 GHz carrier, respectively. The measured reference spur at a 2 MHz offset from a 2.405 GHz carrier is −48.2 dBc. The measured setting time of the synthesizer is about 160 μs.

Key words: phase-locked loop; phase noise; auto frequency calibration; ZigBee; voltage controlled oscillator

ZigBee is an industry standard for short range, low cost, low power and low bit rate wireless applications. It defines 16 channels within the 2.4 GHz unlicensed ISM band (from 2 400 to 2 483.5 MHz with a 5 MHz channel spacing)[1].

In this paper, a low-cost fully integrated CMOS quadrature frequency synthesizer for a 2.4 GHz ZigBee low IF(2 MHz) transceiver is introduced. Compared with IEEE 802.11 series, the ZigBee standard requires a relatively relaxed image rejection requirement. Therefore, the low IF architecture is adopted as the ZigBee receiver to avoid the drawbacks of the direct conversion architecture. With respect to the transmitter, the direct conversion architecture is adopted because it is free from DC offset noise and is simpler in architecture[2]. The block diagram of the transceiver for the 2.4 GHz ZigBee standard is depicted in Fig. 1.

1 Frequency Synthesizer Architecture

Fig. 2 shows the simplified block diagram of the phase locked loop (PLL)-based quadrature frequency synthesizer. The synthesizer consists of a phase-frequency detector (PFD), a charge pump (CP), a voltage control oscillator (VCO), a loop filter(LPF), an integer-N frequency divider, an auto frequency calibration (AFC), and a divide-by-two frequency divider generating I and Q local oscillator (LO) signals.

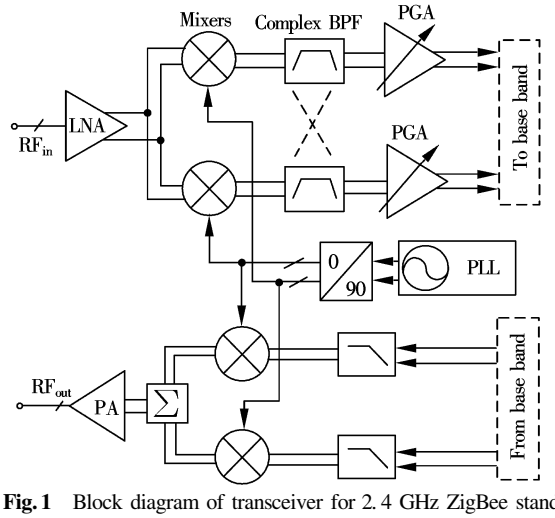

Fig. 1 Block diagram of transceiver for 2.4 GHz ZigBee standard

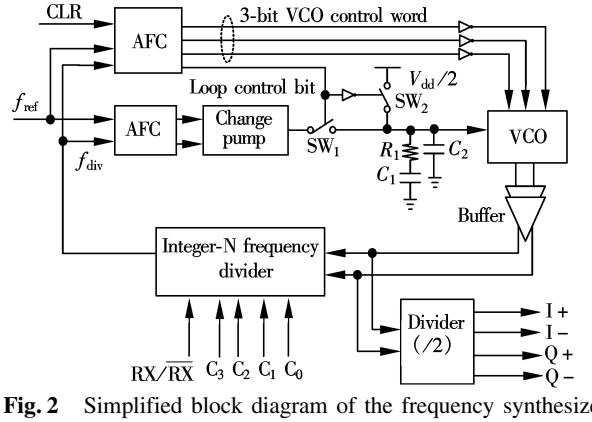

Fig. 2 Simplified block diagram of the frequency synthesizer

The LO frequency is set by programming the 4-bit channel control word(C_3, C_2, C_1, C_0) and the work mode. In receive(RX) mode, the LO frequency is 2 403 + 5C[3:0] MHz since a 2-MHz IF is used. Direct conversion is used for transmission, so here the LO frequency equals 2 405 + 5C[3:0] MHz.

The VCO operates in the frequency range from 4.8 to 4.96 GHz, and the frequency is divided by two when split into I and Q signals. Because the operation frequency of the VCO is different from the channel frequency, the pulling effect of the VCO is avoided. The AFC circuit is adopted to control the frequency drifting problem of the VCO caused by variations in the technology process and the temperature.

The design parameters of the individual blocks are determined not only by loop parameters, but also by the system level performance specifications[3]. Each parameter of the

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PLL has to be optimally chosen in order to achieve short lock time, low phase noise, low power consumption and full integration of the second order passive loop filter.

According to the operation frequency range of the VCO and the effective tuning voltage (from 0.4 to 1.4 V), the conversion gain K_{VCO} of the designed VCO must be larger than 160 MHz/V. In fact, K_{VCO} must be larger than 320 MHz/V because the variation of K_{VCO} may be more than a factor of 2 due to the variations in the technology process[4]. However, a large K_{VCO} will not only degrade the phase noise performance but also increase the capacitance of the LPF which will greatly increase the chip area. Therefore, a VCO conversion gain of 400 MHz/V is selected as a trade-off.

The maximal bandwidth of the PLL is limited by the reference frequency f_{ref} (in this case f_{ref} = 2 MHz), and the minimal bandwidth is limited by the specifics of lock time. In addition, the bandwidth of the PLL affects the parameters of the LPF directly. Thus a bandwidth of 100 kHz with a phase margin of 61° is adopted as a trade-off among settling time, phase noise and stability.

A large I_{CP} can improve the match performance, and thus reduce the spurs of the PLL. However, a large I_{CP} usually requires a large total capacitance of the LPF, which makes the integration of on-chip LPF difficult. As a trade-off, the charge pump current used is 100 μA. According to conventional PLL theory[4], the parameters of the LPF can be computed as R_1 = 33.5 kΩ, C_1 = 237.2 pF, C_2 = 15.8 pF.

2 PLL Building Blocks

2.1 PFD/CP

The PFD in Fig. 2 is a conventional NAND-based scheme. Several techniques and circuit topologies have been reported to improve the performance of the CP[5-7]. The designed charge pump circuit scheme is depicted in Fig. 3. A rail-to-rail error operational amplifier with reference circuit and self-biasing cascade current mirror enables the charge pump current to be well matched in a wide output voltage range.

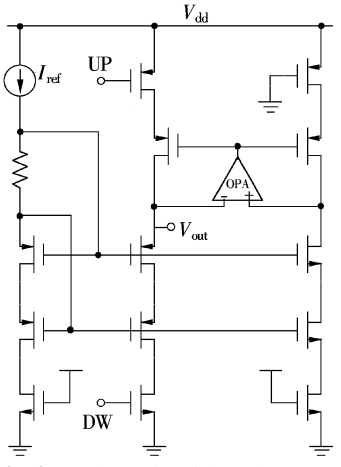

Fig. 3 Schematic of the charge pump

2.2 Voltage control oscillator

The VCOs with a switched-capacitor array bank[8-10] are usually adopted to achieve a wide operating frequency to avoid process variation and frequency drifting problems. A typical LC-VCO with a switched-capacitor array bank diagram is shown in Fig. 4, the output frequency f_o can be expressed as

$$f_o = \frac{1}{2\pi\sqrt{L_{tank}C_{total}}} \tag{1}$$

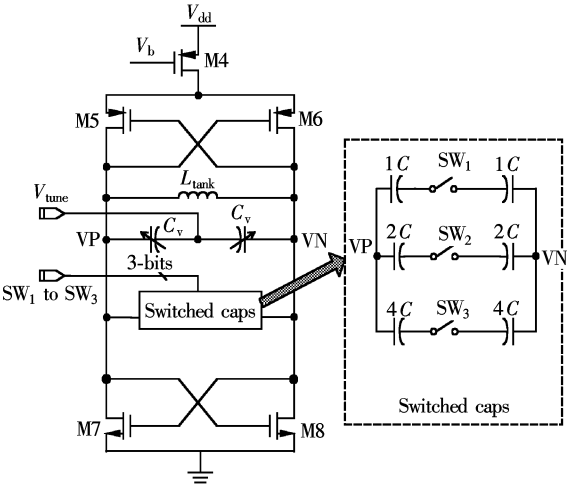

Fig. 4 Typical switched-capacitor LC-VCO

where L_{tank} is the inductance, and C_{total} is the total capacitance in the LC tank including the parasitic capacitance, the varactor and the fixed capacitances. K_{VCO} is defined by

$$K_{VCO} = \left.\frac{\partial f_o}{\partial V}\right|_{V=V_{center}} \tag{2}$$

where V represents the tuning voltage of the VCO, and V_{center} equals the center voltage of the supply. The maximum-to-minimum ratio of K_{VCO} of the conventional switched-capacitor array LC-VCO at different frequency bands is[9]

$$\frac{K_{VCO,max}}{K_{VCO,min}} = \sqrt{\left(\frac{C_{total,max}}{C_{total,min}}\right)^3} = \left(\frac{f_{o,max}}{f_{o,min}}\right)^3 \tag{3}$$

From Eq. (3), we can see that K_{VCO} suffers a large variation when the VCO tuning range ($f_{o,max} - f_{o,min}$) becomes very wide. The variation of K_{VCO} alters the PLL bandwidth, so the phase noise performance is deteriorated and the loop becomes unstable[9].

A new architecture of a switched-capacitor array to reduce the variations of K_{VCO} is proposed in Ref. [10] and it is also adopted in this paper. The proposed LC-VCO is shown in Fig. 5. Compared with the conventional switched-capacitor array, an additional switched-varactor array is added into the LC tank. The oscillator frequency can be expressed as Eq. (1). Now C_{total} in Eq. (3) can be expressed as

$$C_{total} = C_p + C_v + \sum_{i=1}^{3}[SW_i(\alpha_i C_f + \beta_i C_v) + \overline{SW_i}\beta_i C_{v,min}] \tag{4}$$

where C_p is the parasitic capacitance; C_f is the unit capacitance of the switched-capacitance array bank; $C_{v,min}$ is the minimum capacitance of the varactor; C_v is the capacitance of the varactor controlled by the tuning voltage; α_i (i = 1, 2,

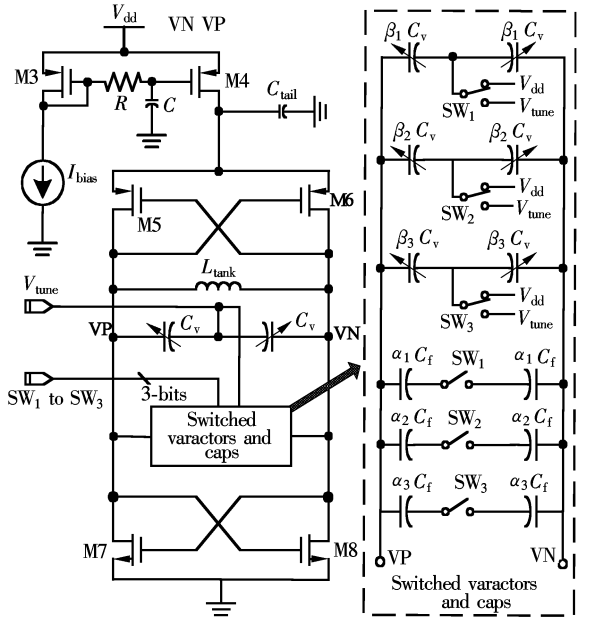

Fig. 5 Proposed LC-VCO

3) is the capacitor ratio of the switched-capacitance array and $\beta_i (i = 1, 2, 3)$ is the varactor ratio of the switched-varactor array. The value of SW$_i$ in Eq. (4) is 0 or 1, according to the 3-bit VCO control word. From Eqs. (1), (2) and (4), the maximum-to-minimum ratio of K_{VCO} can be written as

$$\frac{K_{VCO,max}}{K_{VCO,min}} = \frac{1}{\sum_{i=1}^{3}(1+\beta_i)}\sqrt{\left(\frac{C_{total,max}}{C_{total,min}}\right)^3} = \frac{1}{\sum_{i=1}^{3}(1+\beta_i)}\left(\frac{f_{o,max}}{f_{o,min}}\right)^3 \tag{5}$$

Compared with Eq. (3), we can see that the variations of K_{VCO} can be greatly reduced by properly setting the values of $\beta_i (i = 1, 2, 3)$.

As shown in Fig. 5, a top-biased complementary CMOS VCO topology is used. Using a PMOS (M3 and M4) instead of NMOS to bias the VCO helps to lower $1/f$ noise up-conversion because PMOS devices have a lower $1/f$ noise corner compared with NMOS devices. Also, the top-biased oscillator is more immune to substrate noise because the current source is placed in an n-well, rather than in the substrate. The use of the large tail capacitor in parallel with M4 can improve the phase noise behavior of the differential LC oscillator[11]. A RC low pass filter is used to compress the noise of diode-connected MOSFET M3.

2.3 Programmable frequency divider

The block diagram of the integer-N frequency divider is shown in Fig. 6. It includes a dual modulus prescaler (DMP), a program counter and a swallow counter. The frequency division modulus is $M = PN + S$, where the number $N = 32$; P can be programmed from 75 to 77, and S can be programmed from 0 to 31.

A decoder is used to reduce the bits of programmable frequency control word from 7-bit to 5-bit (4 bits for the channel selection and 1 bit for the mode selection between the transmitter mode and the receiver mode). In the transmit mode, the divider ratio is given by $f_{in}/f_{div} = 2\ 405 + 5C[3:0]$. In the receiver mode, the divider ratio is given by $f_{in}/f_{div} = 2\ 403 + 5C[3:0]$.

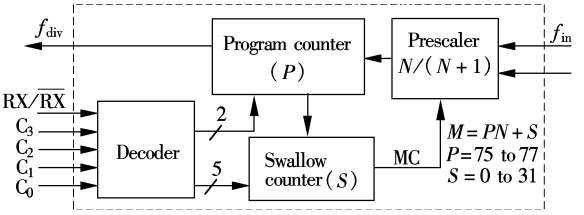

Fig. 6 Block diagram of the integer-N frequency divider

2.4 Auto frequency calibration

The block diagram of the AFC loop incorporated in this synthesizer is shown in Fig. 7, including a counter-based divider (10-bit), a digital counter(10-bit), a counter3 (2-bit) and a SAR(successive approximation register). The frequency of SAR_clock equals $f_{ref}/2^{10}$. The digital counter is reset by the negative edge of the SAR_clock, and at the same time the H signal is set to zero. The H signal tells the SAR whether the divided VCO clock signal frequency f_{div} is higher than the reference frequency f_{ref}. If H is high, the divided VCO clock signal frequency f_{div} is higher than that of the reference f_{ref}; otherwise, f_{div} is lower. The counter3 is triggered at the negative edge of SAR_clock, and it will stop counting when the number in it reduces to zero. The SAR_en keeps low when the number of counter3 is 3 or 0. The 3-bit VCO control word is set bit-by-bit (from high to low) by the SAR. The conventional binary arithmetic[12] is used in this SAR.

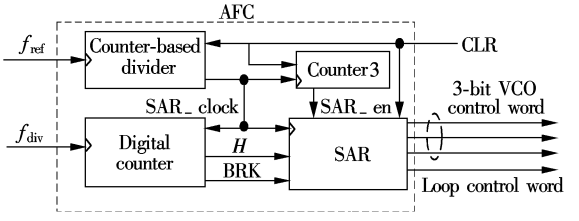

Fig. 7 The block diagram of AFC loop

The AFC flow diagram is shown in Fig. 8. Before the AFC starts to work, the frequency division ratio is set to 2 440. Then the CLR is set to zero, and now the AFC begins to be initialized. During the initiation phase of the AFC, the counter-based divider is reset to zero; the number of counter3 is reset to 3; the 3-bit VCO control word is set to 100; the PLL loop is broken and the VCO tuning voltage is connected to $V_{dd}/2$.

When the CLR becomes high, the counter-based divider and the digital counter begin to count, and at the same time the SAR_clock becomes high. Because the SAR_en is still low, the VCO control word in the SAR is not changed. After 2^9 periods of T_{ref} ($T_{ref} = 1/f_{ref}$), the SAR_clock becomes low; the digital counter is reset to zero; the number of counter3 equals 2; the SAR_en becomes high and the SAR begins to work. At the end of another 2^9 periods, the SAR_clock becomes high. The most significant bit (MSB) of the VCO control word in the SAR is changed to zero if H is high. Then the next bit of the VCO control word is set to 1. Now the 3-bit VCO control word in the SAR is 010. During the next 2^{10} periods, the second bit is changed or maintained

according to H. The last bit of the VCO control word is determined with another 2^{10} periods. The number of counter3 now is 0. The SAR_en is set to 0 by counter3, so the VCO control word is held in the SAR. After the AFC, SW1 in Fig. 2 is closed and SW2 is open.

It needs to be pointed out that the SAR may make errors when the frequency f_{div} equals or is very close to the frequency f_{ref}. To resolve this potential problem, a BRK signal in Fig. 8 is produced by the digital counter when the two frequencies are equal or very close to each other. When the BRK signal is high, the AFC finishes directly.

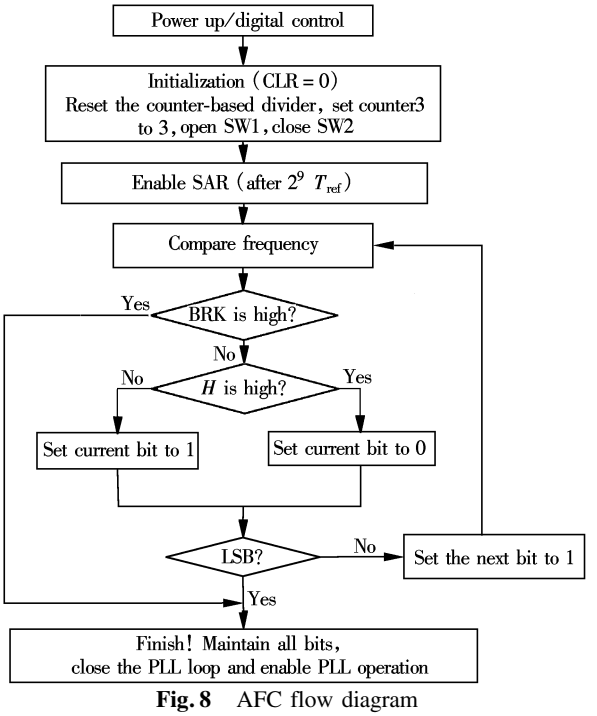

Fig. 8 AFC flow diagram

3 Experimental Results

The fully integrated synthesizer is fabricated in a 0.18 μm RF CMOS process. The microphotograph of the chip is shown in Fig. 9. The area is 1.7 mm^2. The chip is measured on a wafer.

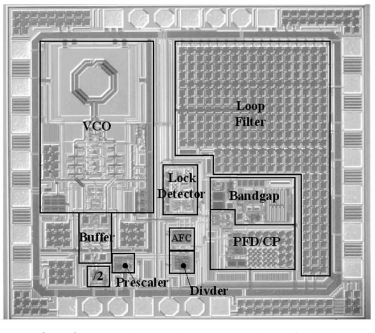

Fig. 9 Microphotograph of chip

The measured VCO tuning characteristics are shown in Fig. 10. The output spectrum for the closed loop synthesizer operating in channel 1 (2.405 GHz) is given in Fig. 11. The observed reference spur is about −48.2 dBc at 2 MHz offset from the carrier. As depicted in Fig. 12, the measured phase noise is −110 dBc/Hz at 1 MHz offset and −122 dBc/Hz at 3 MHz offset from a 2.405 GHz carrier.

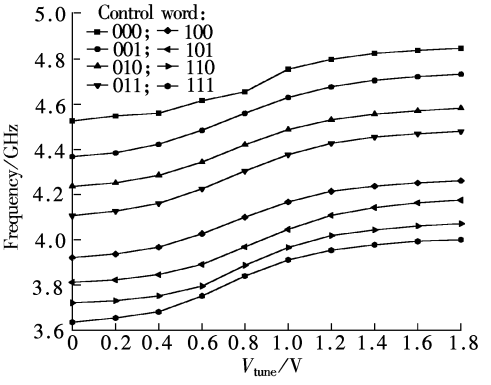

Fig. 10 Measured VCO tuning characteristics

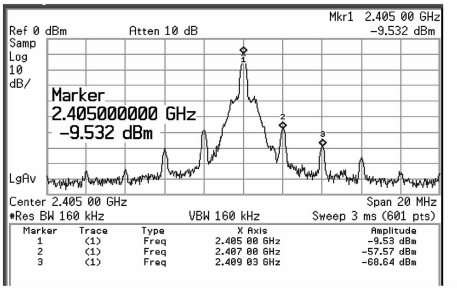

Fig. 11 Measured PLL output spectrum(channel 1)

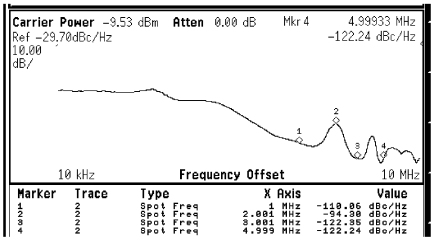

Fig. 12 Measured phase noise

The setting time is measured by watching the tuning voltage of the VCO in the process of switching periodically between channel 11 and channel 16. As shown in Fig. 13, the measured setting time is about 160 μs. However, the practical setting time must be below 160 μs because the PLL loop characteristic is greatly affected by the input impedance of the oscilloscope.

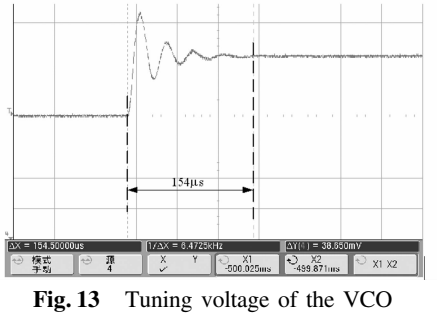

Fig. 13 Tuning voltage of the VCO

The AFC functionality is successfully verified at different frequencies of the reference signal. A summary of the measurement results of the synthesizer is given in Tab. 1 along with the recent 5-GHz synthesizers for comparison.

Tab. 1 Comparison with other published 5-GHz synthesizers

Parameter	This paper	Ref. [13]	Ref. [14] *	Ref. [15] *
Process/μm	0.18	0.18	0.18	0.09
VDD/V	1.8	1.0	1.8	1.2
Reference frequency/MHz	2	20	5	2.5
Power/mW	28.8	29.9	35.5	5.1
Phase noise/ (dBc·Hz^{-1}@1MHz)	−110	−96.3	−117	−106
Phase noise/ (dBc·Hz^{-1}@3MHz)	−122			
Spur/dBc	−48.2			
Setting time/μs	<160	about 40		
AFC	Yes	No	Yes	No
On-chip LPF	Yes	No	No	No

Note: * Only simulation results.

4 Conclusion

A fully integrated frequency synthesizer for a 2.4 GHz ZigBee(IEEE 802.15.4) transceiver is presented. The PLL with AFC is successfully implemented. The charge pump with op-amp feedback is used to reduce current mismatch. The oscillation frequency of the VCO is twice as much as the channel frequency, and I and Q signals are generated by a 1/2 frequency divider at the output of the VCO. Measurement results of the synthesizer are given in Tab. 1 to compare with the other published synthesizers operating at 5 GHz. The synthesizer operates with a 1.8V supply and consumes 28.8 mW. The measured phase noise is −110 and −122 dBc/Hz at 1 and 3 MHz offsets, respectively, from a 2.405 GHz carrier.

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应用于低中频 Zigbee 收发机的 5-GHz 恒定带宽频率综合器

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摘要:设计并实现了一个应用于 ZigBee 收发机的全集成整数 N 频率综合器. 频率综合器中采用了稳定环路带宽技术,使频率综合器的环路带宽在压控振荡器(VCO)的整个输出频率范围内恒定不变,从而维持了频率综合器的相位噪声最优值与环路稳定性. 频率综合器的同相与正交信号(IQ)由 VCO 输出端的除 2 分频器产生. 该频率综合器采用 0.18 μm RF CMOS 工艺技术制造,芯片面积约 1.7 mm^2. 频率综合器采用在晶圆测试的方式进行了测试. 在 1.8 V 电源电压下,频率综合器不包括输出缓冲所消耗的总功率为 28.8 mW. 频率综合器在 2.405 GHz 载波 1 及 3 MHz 频偏处测得相位噪声分别为 −110 和 −122 dBc/Hz. 频率综合器在 2 MHz 频偏处测得的参考杂散为 −48.2 dBc. 测得的建立时间约为 160 μs.

关键词:锁相环;相位噪声;自动频率校准;ZigBee;压控振荡器

中图分类号:TN742;TN752