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A CMOS high-IF down-conversion mixer for WLAN 802.11a applications

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Abstract: A low noise, high conversion gain down-conversion mixer for WLAN 802.11a applications, which adopts the high intermediate frequency (IF) topology, is presented. The input radio frequency (RF) band, local oscillator (LO) frequency band and output IF are 5.15 to 5.35, 4.15 to 4.35 and 1 GHz, respectively. Source resistive degeneration technique and pseudo-differential Gilbert topology are used to achieve high linearity, and, current bleeding technique and LC resonant loads are used to acquire a low noise figure. In addition, the mixer adopts a common-source transistor pair cross-stacked with a source follow pair (CSSF) circuit as an output buffer to enhance the mixer's conversion gain but not deteriorate the other performances. The mixer is implemented in 0.18 μm RF CMOS (complementary metal oxide semiconductor transistor) technology and the chip area of the mixer including all bonding pads is 580 μm × 1 185 μm. The measured results show that under a 1.8 V supply, the conversion gain is 10.1 dB; the input 1 dB compression point and the input-referred third-order intercept point are – 3.5 and 5.3 dBm, respectively; the single side band (SSB) noise figure (NF) is 8.65 dB, and the core current consumption is 3.8 mA.

Key words: high intermediate frequency; mixer; high linearity; WLAN 802.11a; buffer; complementary metal oxide semiconductor transistor (CMOS)

Portable consumer electronics embedded with WLAN chipsets have become more and more popular. The IEEE 802.11a standard, which is based on orthogonal frequency division multiplexing (OFDM) modulation, provides a high data rate and a large system capacity. In recent years, the direct conversion architecture and the low IF architecture have been increasingly used in RF-CMOS transceivers to reduce the costs and save the power consumptions[1-2]. But they have some drawbacks, such as the DC offset, the low image reject ratio and so on. In order to avoid these problems, the RF transceiver described in this paper uses a dual-conversion architecture with a sliding IF of 1 GHz[3] as shown in Fig. 1. The RF signal after the variable gain low-noise amplifier (VG-LNA) first is down-converted to a fixed 1 GHz-IF by the RF-mixer, and then the 1 GHz-IF signal is directly down-converted to I/Q baseband signals by the I/Q-demodulator. In this structure, the second LO signal is generated from the first LO signal using a divide-by-four divider, eliminating the need for two synthesizers. The divide-by-four divider can inherently provide very precise quadrature LO signals at 1 GHz, thereby improving the receiver's image rejection.

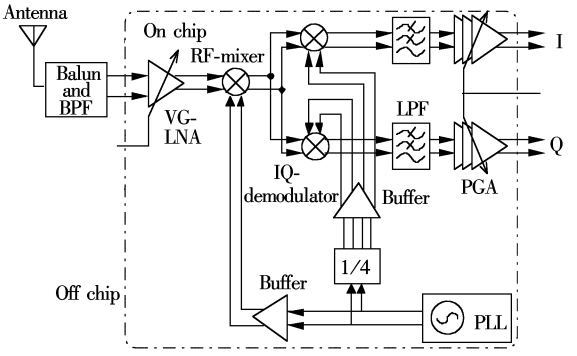

Fig. 1 Dual-conversion sliding-IF WLAN receiver architecture

The mixer is one of the most important building blocks in a communication system. The purpose of the mixer is to convert a signal from one frequency to another. In a receiver, the conversion is from RF to IF. As a part of RF front-end circuits, its performance directly impacts the whole system's performance, such as dynamic range, isolations, noise figure and so on. One of the most important impacts is that the mixer limits the linearity of the whole receiver. So, it must have a large enough linearity to handle the large signals from the LNA. On the other hand, as the second active block in the receiving chain, it must have a low noise figure and a high enough voltage gain to suppress the noise contribution from the next block.

1 Circuit Topology and Considerations

1.1 Pseudo-differential topology

The CMOS Gilbert active mixer becomes more and more popular in the modern receivers, because of its reasonable conversion gain, moderate linearity, low noise figure and high port-to-port isolations. But, as the CMOS technology is scaling down, the supply voltage becomes lower and lower, and the voltage headroom becomes very critical. The conventional Gilbert topology shown in Fig. 2(a) is not suitable for the modern design. In order to acquire high performances, some new techniques are used in the mixer design. The Gilbert mixer with source degeneration and current bleeding is shown in Fig. 2(b). Compared with the conventional Gilbert mixer, the proposed mixer eliminates the tail current source to enhance the linearity of the transconductor stage. Fig. 3(a) shows the transconductor stage of the conventional Gilbert mixer, which is a source-coupled differential pair. Fig. 3(b) shows the pseudo-differential topology.

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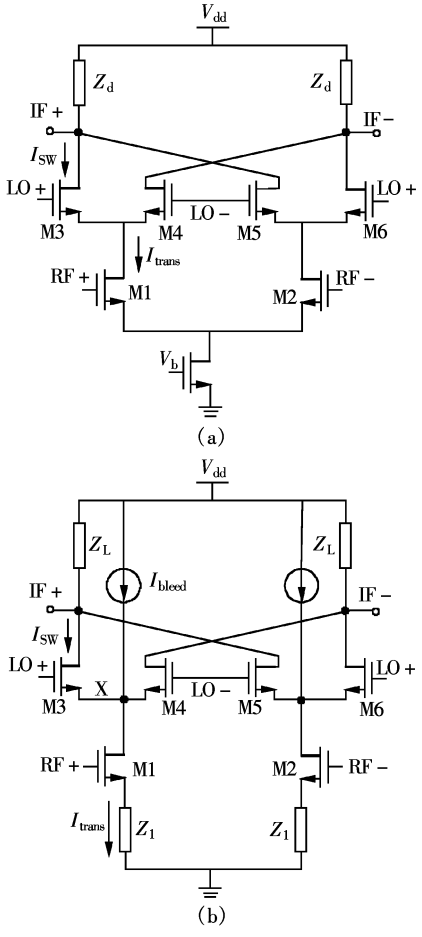

Fig. 2 Two topologies of down-conversion mixers. (a) Conventional Gilbert mixer; (b) Gilbert mixer with source degeneration and current bleeding

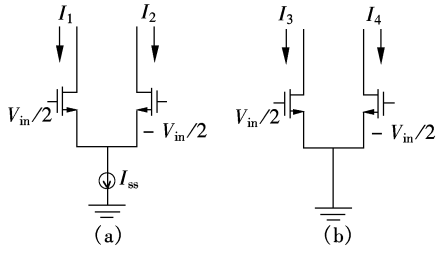

Fig. 3 Transconductor stages. (a) With tail current; (b) Without tail current

MOSFET can be expressed as[4]

$$I_D = K\frac{(V_{GS}-V_T)^2}{1+\theta(V_{GS}-V_T)} \tag{1}$$

where I_D is the drain current; K depends on the technology and the device size, which is proportional to the channel width; $V_{GS}-V_T$ is the overdrive voltage; V_T is the threshold voltage of the MOSFET. The parameter θ models the first order of the source series resistance, the mobility degradation due to the vertical field, and the velocity saturation due to the lateral field in short channel devices. θ is a constant around 0.001 to 0.1 V, which depends on the channel length and is independent on the body effect. For a short channel device, ignoring the third and the higher order terms of θ, the output current of the transconductor stage can be expressed as

$$\Delta I_{1,2} = I_1 - I_2 \approx \frac{1}{2}KV_{in}\left(\sqrt{\frac{4I_{SS}}{K}-V_{in}^2}-\theta\left(\frac{2I_{SS}}{K}-V_{in}^2\right)\right) \tag{2}$$

$$\Delta I_{3,4} = I_3 - I_4 \approx -KV_{in}V_T(1+\theta V_T^2) \tag{3}$$

According to Eq. (2) and Eq. (3), it can be seen that, at the short channel length, the differential pair without the tail current is obviously more linear than the pair with the current source.

1.2 Source resistive degeneration

Linearity is the most important requirement of the mixer. There are many methods to improve the mixer's linearity. One of the most common and effective methods is to use source degeneration. Theoretically, there are three types of source degeneration. Inductive degeneration has no thermal noise to degrade the noise figure, and it does not consume voltage headroom. The inductor occupies a lot of chip area. The capacitive degeneration may cause instability problems and need an additional DC path. So, in this paper, the resistive degeneration is adopted to achieve a small area and a broad bandwidth. But the degeneration resistor may consume the voltage headroom. The limitation for voltage headroom is an important reason for output compression. The available voltage headroom is related to the bias conditions and the source resistance. The available headroom can be expressed as

$$V_{AV} = V_{dd} - V_{DS,\,min} - V_{X,\,min} \tag{4}$$

$$V_{DS,\,min} = (V_{GS}-V_T)_{SW},\quad V_{X,\,min} = (V_{GS}-V_T)_{Trans} + I_{Trans}R_1 \tag{5}$$

where V_{dd} is the supply voltage; V_X is the DC voltage at node X in Fig. 2(b); I_{Trans} is the DC current of the transconductor stage, and R_1 is the resistance of Z_1. For the long channel MOSFET, $(V_{GS}-V_T)^2 \propto I_D$; and for a short channel MOSFET, $(V_{GS}-V_T) \propto I_D$. So, decreasing the bias current can acquire a large voltage headroom. Great R_1 may increase the linearity of the transconductor stage, but great R_1 may also cause a low available voltage headroom, which will decrease the mixer's linearity. So, the choice of the R_1 value must be traded off.

1.3 Current bleeding

Because the IF frequency is very high, the $1/f$ noise can be ignored. The white noise of the switching core dominates the mixer's noise figure. The thermal noise generated in the switching core has periodically time-varying statistics. The switching core FETs (M3 to M6) operate among the triode, the cutoff and the saturation region. The thermal noise appears at the output when switch core FETs are in the saturation region. When switch core FETs are off, the thermal noise does not contribute to the noise output. So, when one switch pair is conducting, we want the other pair to be completely off. If two pairs are conducting current at the same time, it will generate maximum noise. The output noise current produced by a single MOSFET in the switching core is given by[5]

$$\overline{i_{o,\,SW}^2} = 4kT\gamma\frac{I_{SW}}{\pi V_{LO}} \tag{6}$$

where I_{SW} is the DC current through the switching MOSFET (M3 to M6). In order to reduce the noise of the switching core, I_{SW} must be reduced. In the conventional Gilbert mixer, we have $I_{trans} = 2I_{sw}$. So, reducing the bias current will decrease the transconductor stage's linearity and voltage gain. If adopting the current bleeding technique, the current flow through the transconductor stage and the switching core can be optimized separately[6]. But, if I_{SW} is too small, the current flow through the load will be compressed. Furthermore, the bleeding current source will increase the parasitic capacitances at node X, which will increase the noise figure. So, there must be a tradeoff between the bleeding current and the switching core current. The input 1 dB compression point and noise figure (NF) as a function of the bleeding current are illustrated in Fig. 4. Usually, setting the bleeding current to be three-quarters of the transconductor stage current appears to be a good compromise.

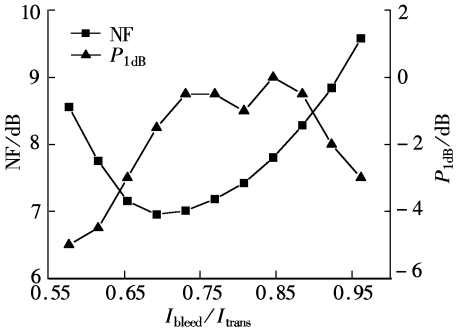

Fig. 4 Linearity and NF vs. the bleeding current

2 Circuit Design and Optimization

Based on the above analysis, a high-IF CMOS down conversion mixer for WLAN802. 11a is designed and optimized. The schematic is shown in Fig. 5. The RF frequency is from 5. 15 to 5. 35 GHz, and the LO frequency is from 4. 15 to 4. 35 GHz. In order to maximize the voltage headroom required by the mixer for low voltage operation, the Gilbert mixer has only two stacked transistors. By using the current bleeding technique, the bias currents flow through the switch and the transconductor stage can be separately optimized to obtain a higher gain and a better noise figure.

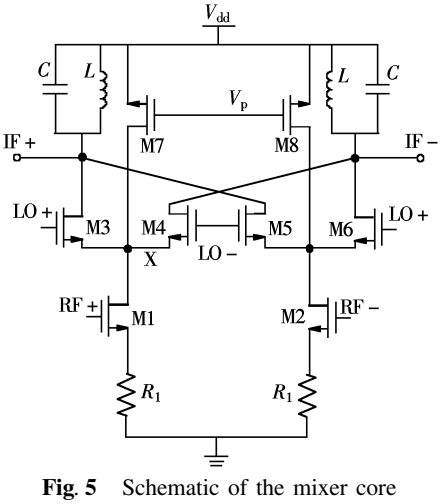

Fig. 5 Schematic of the mixer core

2. 1 Transconductor stage

The gain of this mixer with the source degeneration in Fig. 5 can be written as

$$V_{Gain} = \frac{2}{\pi} G_m Z_L \tag{7}$$

$$G_m = \frac{g_m}{1 + g_m R_1} \tag{8}$$

where g_m is the transconductance of the input device M1 (M2); R_1 is the source degeneration resistor and Z_L is the load impedance. From Eq. (7), the voltage gain of the mixer is dominated by the transconductor stage and the load impedance when the switch is perfect.

In the Gilbert mixers, the linearity is mainly limited by the transconductor stage. The input-referred third-order intercept point (P_{IIP3}) is defined from the transconductor stage as[7]

$$P_{IIP3} = \frac{8}{3}\frac{V_{sat}L}{\mu_1 R_S}(V_{GS} - V_T)_{Trans}\left(1 + \frac{\mu_1 (V_{GS} - V_T)_{Trans}}{4V_{sat}L}\right) \cdot \left(1 + \frac{\mu_1 (V_{GS} - V_T)_{Trans}}{2V_{sat}L}\right)^2 \tag{9}$$

$$\mu_1 = \mu_0 + 2\theta V_{sat} L \tag{10}$$

where V_{sat} is the saturation velocity; L is the channel length; R_S is the source resistance, and μ_0 is the electronic mobility. From Eqs. (7) and (9), it can be seen that great overdrive voltage can increase the linearity and voltage gain, and great R_1 can also increase the linearity. But the large overdrive voltage will decrease the voltage headroom and increase power consumption, and great R_1 may reduce the voltage headroom and voltage gain. So, the value of R_1 must be properly chosen to acquire high linearity and high gain.

2. 2 Switching core

A perfect switching core must have small switch delay[4, 8]. The transition time of the switching core can be expressed as[9]

$$T_{tr} = \sqrt{\frac{2I_{SW}}{K}}\frac{1}{V_{LO}\omega_{LO}} = \frac{\sqrt{2}(V_{GS} - V_T)_{SW}}{V_{LO}\omega_{LO}} \tag{11}$$

where ω_{LO} is the frequency of the LO; V_{LO} is the amplitude of the LO. According to Eq. (11), a large LO amplitude and a small over drive voltage of the switching core can reduce the transition time. However, when the LO becomes too large, it leads to spikes in the signals, reducing the switching speed and increasing the LO feed-through. The spikes can also cause transistors to leave the saturation region. On the other hand, the overdrive voltage cannot be too small. Low overdrive voltage means a large transistor size which will increase the parasitic capacitance at node X. Fig. 6 shows the variation of both the conversion gain and the noise figure for different values of the LO power. From Fig. 6, the LO power can be selected by considering the gain and the NF. So, the design procedure of the switching core is shown as follows. First, the current through the switching core I_{SW} can be determined according to the cur-

rent of the transconductor stage. Then, the overdrive voltage and the device size are chosen according to I_{SW}. Finally, an appropriate LO power is selected from Fig. 6.

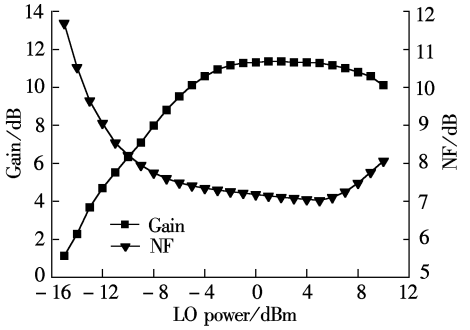

Fig. 6 Gain and NF vs. the LO power

2.3 Load stage

There are three types of load for mixer design: resistor, MOSFET and inductor. Usually, no inductor is used in a low IF down conversion mixer, because the Q value of the inductor is very small at a low frequency and the value of the inductor is very large which is unrealistic. In this design, the IF is 1 GHz. The load can adopt an LC resonate network. The inductance and the Q-factor of the load inductor are about 15 nH and 8 at 1 GHz, respectively. Compared with the resistor and the MOSFET loads, the LC load has some significant advantages. First, it can acquire a high conversion gain to suppress the next block's noise. Secondly, the ideal LC resonate network is noiseless. Thirdly, the LC network does not occupy the voltage headroom, thus improving the mixer's linearity. Finally, the LC resonant load is a frequency selective network, so it can improve the mixer's isolations and suppress other harmonics at the IF output port.

2.4 Buffer design

Because the impedance of the LC load is very high, a buffer is required to drive the test equipment. This buffer must not decrease the mixer's performance. So, it should have high linearity, unity gain and low power consumption. Usually the source follower is used as a buffer shown in Fig. 7(a), but this structure has large power consumption and low voltage gain. A new structure is adopted which is composed of a common-source transistor pair cross-stacked with a source follower pair[10] shown in Fig. 7(b). The

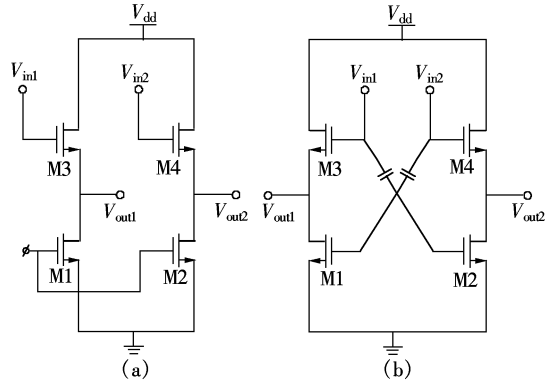

Fig. 7 Two topologies of buffers. (a) SF buffer; (b) Proposed CSSF buffer

compensation via M1 tends to keep the current constant in the follower transistor M3, thus improving the linearity. The IIP3 is higher than the conventional source follower. The gain of the buffer is given by

$$V_{\text{Gain, CSSF}} = \frac{g_{m1} + g_{m3}}{g_{m1} + g_{mb1} + 1/r_{01} + 1/r_{03}} \tag{12}$$

$$V_{\text{Gain, SF}} = \frac{g_{m1}}{g_{m1} + g_{mb1} + 1/r_{01} + 1/r_{03}} \tag{13}$$

where g_{mb} is the body transconductance. Comparing Eq. (12) with Eq. (13), the gain of the CSSF buffer is obviously greater than that of the SF buffer. The gain of the CSSF buffer is greater than 1 when

$$g_{m3} > g_{mb1} + \frac{1}{r_{01}} + \frac{1}{r_{03}} \tag{14}$$

Fig. 8 shows the input 1dB compression point of the two circuits at the same bias current(The half circuit bias current is 2.2 mA). It can be seen that the gain and the linearity of the CSSF are obviously higher than that of the SF circuit.

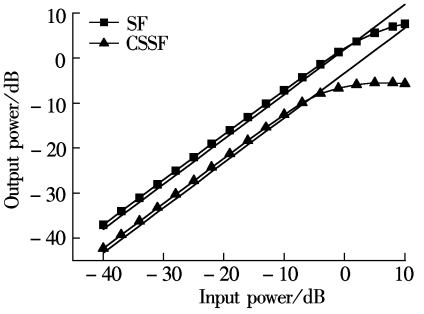

Fig. 8 P_{1dB} of the SF and CSSF circuit

3 Implement and Measurement Results

The mixer is fabricated with the SMIC 0.18 μm 1P6M RF CMOS technology. The microphotograph of the mixer is shown in Fig. 9. Each MOSFET is surrounded by a deep n-well(DNW) to reduce the noise and to avoid the body effect. The inductors add N + and P + guard rings to isolate the substrate noise. The octagon pads of the top metal(M6) are used for the signal pads to reduce the pad's parasitic capacitance. In order to attain good matching, the layouts of the resistors are common centroid. All the components are fully symmetrical. The chip area of the mixer with the IF buffer including all bonding pads is 580 μm × 1 185 μm. The testing instruments include a spectrum analyzer E4440A, a vector network analyzer E5071B, a noise figure analyzer N8975A, and RF signal generators E4438C and SMP04.

Fig. 10 shows the input 1 dB compression point at the center frequency of 5.25 GHz. The input 1 dB compression

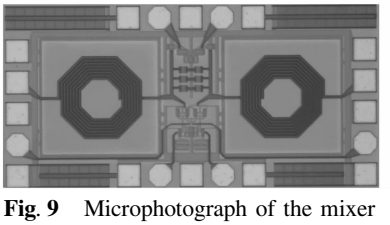

Fig. 9 Microphotograph of the mixer

point is about −3. 5 dBm. Fig. 11 shows the noise figure curve of the mixer. It can be seen that the noise figure is about 8. 65 dB at 1 GHz. The minimum noise figure is about 7. 9 dB at 1. 01 GHz. The frequencies of RF, LO and IF are 5. 25, 4. 25 and 1 GHz, respectively. Fig. 12 is the output spectrum of two tone tests. The frequency space is 5 MHz. The IIP3 of the mixer is about 5. 3 dBm.

The measurement results are summarized and compared with some recently published mixers in Tab. 1.

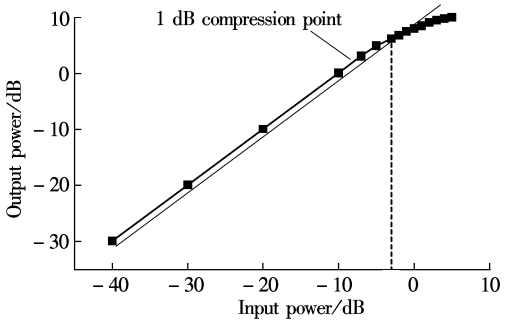

Fig. 10 Input 1dB compression point

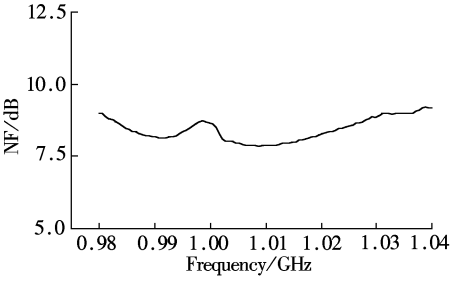

Fig. 11 Noise figure

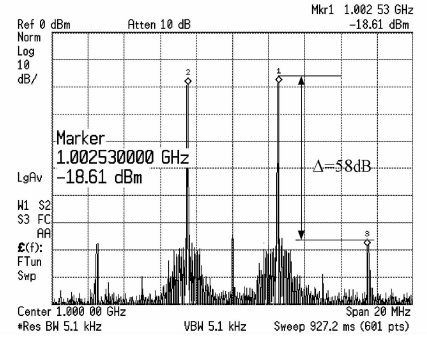

Fig. 12 Output spectrum

Tab. 1 Performance summary and comparison

Reference	Frequency/GHz	V_{Gain}/dB	($P_{1\ dB}$/P_{IIP3})/dBm	SSB NF/dB	Current/mA	Process
Ref. [11]	2. 4	15. 7	NA/1	12. 9	4. 5	0. 18 μm CMOS
Ref. [12]	0. 9	4	NA/ −5. 6	11. 2	4	0. 35 μm CMOS
Ref. [13]	2. 4	−4. 5	1/NA	18	10/40 *	0. 18 μm CMOS
Ref. [14]	0. 915	12. 5	NA/10	17. 6	3	0. 18 μm CMOS
This paper	5. 25	10. 1	−3. 5/5. 3	8. 65	3. 8/5 *	0. 18 μm CMOS

Note: * Output buffer current.

4 Conclusion

A 5 GHz mixer with the source degeneration and the current bleeding techniques is analyzed and designed for the WLAN 802. 11a system. Compared with the other mixer circuits reported in Tab. 1, some key parameters are better. The measurement results indicate that the designed mixer has good performance and meets the requirements of the WLAN 802. 11a system.

References

[1] Brandolini M, Sosio M, Svelto F. A 750 mV fully integrated direct conversion receiver front-end for GSM in 90-nm CMOS [J]. *IEEE Journal of Solid-State Circuits*, 2007, **42**(6): 1310 − 1317.

[2] Chen T M, Chiu Y M, Wang C C, et al. A low-power fullband 802. 11a/b/g WLAN transceiver with on-chip PA [J]. *IEEE Journal of Solid-State Circuits*, 2007, **42**(2): 983 − 991.

[3] Zargari M, Su D K, Yue C P, et al. A 5-GHz CMOS Transceiver for IEEE 802. 11a WLAN Systems [J]. *IEEE Journal of Solid-State Circuits*, 2002, **37**(12): 1688 − 1694.

[4] Terrovitis M T, Meyer R G. Intermodulation distortion in current-commutating CMOS mixers [J]. *IEEE Journal of Solid-State Circuits*, 2000, **34**(6): 1461 − 1473.

[5] Darabi H, Abidi A A. Noise in RF-CMOS mixers: a simple physical model [J]. *IEEE Transactions on Solid-State Circuits*, 2000, **35**(1): 15 − 25.

[6] MacEachern L A, Manku T. A charge-injection method for Gilbert cell biasing [C]//*IEEE Canadian Conf Electrical and Computer Engineering*. Toronto, Canada, 1998: 365 − 368.

[7] Soorapanth T, Lee T H. RF linearity of short-channel MOSFETs [C]//*Proceedings of the First International Workshop on Design of Mixed-Mode Integrated Circuits and Applications*. Cancun, Mexico, 1997: 81 − 84.

[8] Terrovitis M T, Meyer R G. Noise in current-commutating CMOS mixers [J]. *IEEE Journal of Solid-State Circuits*, 1999, **34**(6): 772 − 783.

[9] Hossain M, Frank B M, Antar Y M. A low voltage highly linear 24 GHz down conversion mixer in 0. 18-μm CMOS [J]. *Microwave and Optical Technology Letter*, 2007, **49**(10): 2547 − 2552.

[10] Gharpurey R. A broadband low-noise front-end amplifier for ultra wideband in 0. 13-μm CMOS [J]. *IEEE Journal of Solid-State Circuits*, 2005, **40**(9): 1983 − 1986.

[11] Vidojkovic V, Tang J, Leeuwenburgh A, et al. A low-voltage folded-switching mixer in 0. 18-μm CMOS [J]. *IEEE Journal of Solid-State Circuits*, 2005, **40**(6): 1259 − 1264.

[12] Lee S G, Choi J K. Current-reuse bleeding mixer [J]. *Electronics Letters*, 2000, **36**(8): 696 − 697.

[13] Chi Baoyong, Shi Bingxue. CMOS mixers for 2. 4 GHz WLAN transceivers [J]. *Chinese Journal of Semiconductors*, 2003, **24**(5): 472 − 475.

[14] Ni Ronghua, Tan Xi, Tang Zhangwen. Analysis and design of a quadrature down-conversion mixer for UHF RFID readers [J]. *Chinese Journal of Semiconductors*, 2008, **29**(6): 1128 − 1135.

应用于无线局域网 802.11a 高中频下变频器的设计

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摘要：给出了一个应用于无线局域网 WLAN802.11a 的中低噪声、高增益的下变频器. 该下变频器采用高中频的结构，输入的射频频率(RF)、本振(LO)频率和输出的中频频率(IF)分别为 5.15～5.35，4.15～4.35 和 1 GHz. 为了提高混频器的线性度，电路采用了伪差分的吉尔伯特结构和源极电阻负反馈技术；为了获得低的噪声系数，混频器采用电流源注入技术和 LC 谐振电路作为负载. 此外，采用了一种改进的源极跟随器输出缓冲电路，在不恶化其他性能的情况下混频器可以达到较高的增益. 该芯片采用 0.18 μm RF CMOS 工艺制作，包含所有焊盘在内的芯片尺寸为 580 μm×1 185 μm. 测试结果表明：在 1.8 V 电源电压下，消耗电流为 3.8 mA，转换增益为 10.1 dB，输入 1 dB 压缩点为 −3.5 dBm，输入三阶截点为 5.3 dBm，单边带(SSB)噪声系数(NF)为 8.65 dB.

关键词：高中频；混频器；高线性度；无线局域网 802.11a；缓冲；金属氧化物半导体

中图分类号：TN402；TN432