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Analysis of hot-carrier degradation in N-LDMOS transistor with step gate oxide

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Abstract: In order to minimize the hot-carrier effect (HCE) and maintain on-state performance in the high voltage N-type lateral double diffused MOS (N-LDMOS), an optimized device structure with step gate oxide is proposed. Compared with the conventional configuration, the electric field under the gate along the Si-SiO_2 interface in the presented N-LDMOS can be greatly reduced, which favors reducing the hot-carrier degradation. The step gate oxide can be achieved by double gate oxide growth, which is commonly used in some smart power ICs. The differences in hot-carrier degradations between the novel structure and the conventional structure are investigated and analyzed by 2D technology computer-aided design (TCAD) numerical simulations, and the optimal length of the thick gate oxide part in the novel N-LDMOS device can also be acquired on the basis of maintaining the characteristic parameters of the conventional device. Finally, the practical degradation measurements of some characteristic parameters can also be carried out. It is found that the hot-carrier degradation of the novel N-LDMOS device can be improved greatly.

Key words: hot-carrier; degradation; step gate oxide; N-type lateral double diffused MOS (N-LDMOS)

In order to fulfill the trend of lower cost and smaller chip size in recent specific high-voltage products, high-voltage devices are integrated into advanced CMOS and BiCMOS technologies[1-3]. Typically, the lateral double diffused MOS (LDMOS) are the devices of choice to accomplish this task as they are compatible with standard CMOS processing and can be easily integrated by the addition of some extra process layers. The LDMOS devices usually work under high temperature, high voltage and high power conditions. Consequently, they suffer seriously from hot-carrier effects and the hot-carrier degradation of LDMOS devices has become an important reliability issue of power integrated circuits[4-6]. It is well known that the R_{on} (on-resistance) of the device has a strong dependence on the gate oxide thickness at the same gate voltage condition, which needs to be thinner to gain a lower R_{on} value. However, the LDMOS devices with a thinner gate oxide thickness also undergo hot-carrier effects more seriously. Nowadays, hot-carrier degradation studies of LDMOS transistors are mainly focused on the explanations of various degradation phenomena under static or dynamic stress[7-8]. Very little information is available on how to alleviate the hot-carrier effects of LDMOS devices.

A kind of N-LDMOS transistor with step gate oxide is presented, which is used to effectively restrain the hot-carrier effects of the high voltage devices. The novel structure of step gate oxide is illustrated in section 1. The TCAD simulations show that the perpendicular electric field under the gate and the quantity of the hot-carrier injecting into the gate oxide in the improved N-LDMOS is much smaller than the one in the conventional N-LDMOS, which indicates the melioration of the hot-carrier degradation in the novel N-LDMOS device. At the same time, according to the simulation results, it is found that the threshold voltage and the breakdown voltage of the N-LDMOS with step gate oxide are basically equal to the ones of the conventional N-LDMOS. Finally, the practical degradation measurements of some characteristic parameters are used to support the numerical simulation results.

1 Device Structure

The device studied in this paper is the N-type lateral double diffused MOS transistor with step gate oxide, which is implemented in 0.5 μm CMOS technology using bulk silicon. The step gate oxide can be achieved by double gate oxide growth, which is commonly used in double gates process of some smart power ICs. Consequently, the fabrication of the step gate oxide is easily achievable. The cross-sections of the conventional N-LDMOS device and the ana-

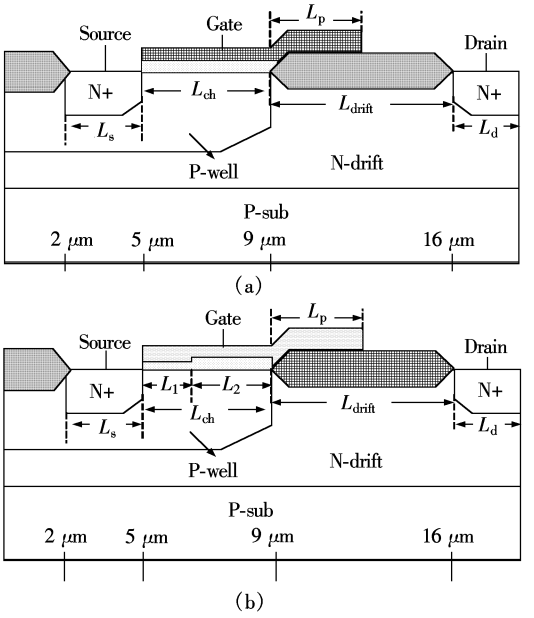

Fig. 1 Schematic cross-sections and components of two N-LDMOS devices. (a) Conventional N-LDMOS device; (b) N-LDMOS device studied in this paper

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lyzed device in this paper are illustrated in Fig. 1, and the main geometrical and technological parameters of the proposed N-LDMOS are listed in Tab. 1. As we can see from Fig. 1, compared with the conventional N-LDMOS, the only difference in the suggested N-LDMOS is the gate oxide, which is with a step, and other parts of the device are the same.

Tab. 1 Main parameters of proposed N-LDMOS μm

Parameter	Value
Channel length L_{ch}	4
Gate oxide length $L_1 + L_2$	4
Thin gate oxide length L_1	Variable
Thin gate oxide thickness	12.5×10^{-3}
Thick gate oxide length L_2	Variable
Thick gate oxide thickness	25×10^{-3}
Effective drift region length L_{drift}	7
Poly overlap field oxide L_p	5
Source and drain length L_s, L_d	3

2 Simulation and Discussion

The hot-carrier effect has been closely connected with electric field intensity under the gate of the high voltage device. Fig. 2 shows the variations in the perpendicular electric field and the total electric field along the Si-SiO_2 interface of the N-LDMOS devices with different lengths of L_2 at $V_{gs} = 10$ V and $V_{ds} = 100$ V, which is the worst stress condition for the studied N-LDMOS device. As shown in Fig. 2, the positions of the peak value of the total electric field of the conventional N-LDMOS are at $x = 7$ μm and $x = 14$ μm, where hot carriers can be easily generated. However, the position at $x = 7$ μm belongs to the channel region under the gate, where the generating hot carrier can be easily injected and trapped into the gate oxide and the hot-carrier degradation of the device becomes very serious. Nevertheless, it can also be seen from Fig. 2 that the perpendicular electric field and the total electric field under the gate are obviously reduced for the presented N-LDMOS, which is caused by the modulation of the thick gate oxide part. The longer the thick gate oxide length L_2 is, the more the perpendicular electric field and the total electric field under the gate can be reduced. Thereby, it is believed that the hot-carrier degradation of the improved N-LDMOS can also be decreased.

Fig. 3 shows the relationship between the impact ionization generations (IIG) along the Si-SiO_2 interface and the transverse position of the N-LDMOS devices with different lengths of L_2 at $V_{gs} = 10$ V and $V_{ds} = 100$ V. As can be observed in Fig. 3, the impact ionization generations under the gate are smaller for the proposed N-LDMOS than the ones for the conventional N-LDMOS, and the impact ionization generations under the gate decrease when L_2 increases. But it is very interesting that the most obvious decrease in the impact ionization generations, which is decreased by about 4 orders of magnitude, occurs at $x = 7$ μm with $L_2 = 2$ μm. It is due to the fact that the total electric field under the gate of N-LDMOS with $L_2 = 2$ μm is the lowest at $x = 7$ μm, and it can be seen in Fig. 2.

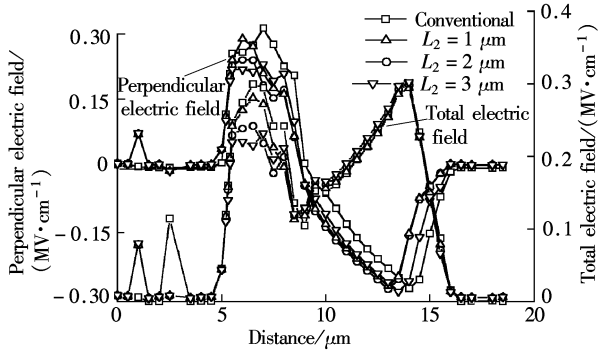

Fig. 2 Perpendicular and total electric field along Si-SiO_2 interface of N-LDMOS devices with different lengths of L_2 at $V_{gs} = 10$ V and $V_{ds} = 100$ V

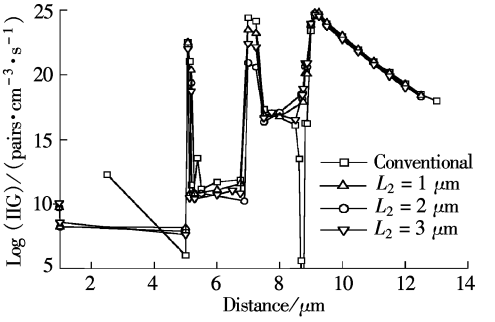

Fig. 3 Impact ionization distribution along Si-SiO2 interface of N-LDMOS devices

Fig. 4 shows the electron temperature and the hole temperature under the gate dependency as a function of the transverse distance of the conventional N-LDMOS. It is very clear that the hole temperature in the depletion region, which is more than 1 000 K, is much greater than the electron temperature in the channel. In this way, very few electrons can be injected into the gate oxide due to the low energy; however, hot holes with high energy can do it though the perpendicular electric field along the Si-SiO_2 interface is positive (pointing to the substrate). So the threshold voltage of the device will decrease as the working hours increase. The difference between the hole temperature and the electron temperature can be explained as follows: The electrons in the channel can be swiftly and orderly drawn into the drift region due to the transverse electric field, but the hole in the depletion region cannot be drawn out and has to be easily accelerated due to the transverse electric field. As a result, the temperature difference appears.

Consequently, the simulation results demonstrate that the

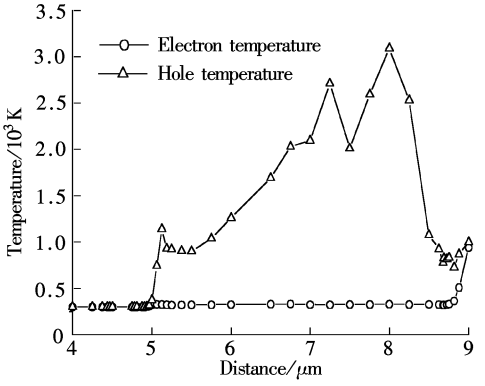

Fig. 4 Carrier temperature along Si-SiO2 interface of conventional N-LDMOS devices

step gate oxide in the high voltage N-LDMOS is very useful for reducing the hot-carrier degradation, and there is hot hole injection into the gate oxide in the channel. However, the length of the thick oxide L_2 must be proper in order to maintain the basic characteristic parameters of the N-LDMOS.

The basic characteristic parameters of the presented N-LDMOS with different lengths of L_2 are listed in Tab. 2, which are simulated by means of MEDICI. We can see from Tab. 2 that the threshold voltage increases by 0.9 V when $L_2 = 3$ μm, but the ones under other conditions remain constant. The lateral distributions of the threshold voltage in the channel region are nonuniform, and the maximum point of the threshold voltage is usually located at the middle of the channel[9]. Consequently, if the thick gate oxide part cannot cover the position of the maximum threshold voltage, the threshold voltage of the device is invariable. However, once the position is covered by the thick gate oxide part, the threshold voltage of the device will change immediately. This is because the inductive charge at the position will be obviously decreased due to the covering of the thick gate oxide, and the inversion layer cannot form, just as what happens at $L_2 = 3$ μm. At the same time, from Tab. 2, it can be seen that the breakdown voltages of different N-LDMOS devices are the same. Nevertheless, the on-resistances ($V_{gs} = 5$ V, $V_{ds} = 1$ V) of the devices increase a little as L_2 increases. The reason is that the channel inductive charge under the thick gate oxide is reduced.

Tab. 2 Basic characteristic parameters of the proposed N-LDMOS with different lengths of L_2

L_2/μm	Threshold voltage/V	Breakdown voltage/V	On-resistance/ ($m\Omega \cdot cm^{-2}$)
0	1.8	129	16.17
1	1.8	132	17.27
2	1.8	134	19.00
3	2.7	134	25.33

According to the above simulations and discussions, the proper length of L_2 is 2 μm, where the thick gate oxide just covers the position of the maximum threshold voltage. At this time, the structure of step gate oxide not only effectively restrains the hot-carrier degradation but also maintains the threshold voltage and breakdown voltage of the N-LDMOS, and the on-resistance is also within an acceptable range.

3 Measurement and Discussion

Fig. 5 is the threshold voltage V_{th} shift as a function of stress time for the conventional and the presented N-LDMOS with $L_2 = 2$ μm under $V_{gs} = 10$ V and $V_{ds} = 100$ V stressed condition. It is clear that the V_{th} degradation of the new LDMOS with step gate oxide is much smaller than the one of the conventional N-LDMOS. V_{th} decreases when the stress time increases, which is in agreement with the above simulation. The saturated drain current I_{dsat} shift measured at the conventional and the proposed N-LDMOS with $L_2 = 2$ μm as a function of stress time is illustrated in Fig. 6, and the stress condition is also $V_{gs} = 10$ V and $V_{ds} = 100$ V. The reason for the increase of I_{dsat} is that more electrons are induced under the gate due to the hole injection into the gate oxide, which reduces the on-resistance of the device. It is noted that the degradation of I_{dsat} in the novel N-LDMOS device is much smaller, so as to have a longer device lifetime.

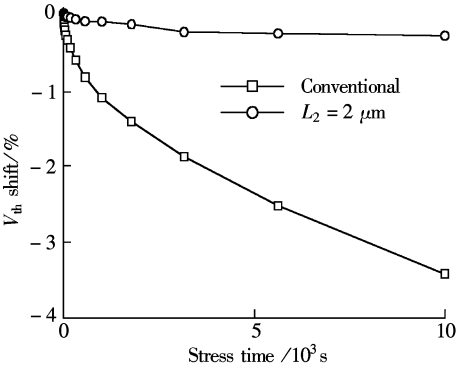

Fig. 5 V_{th} shift as a function of stress time for the LDMOS device

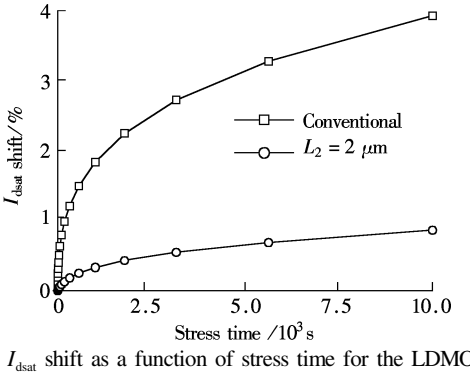

Fig. 6 I_{dsat} shift as a function of stress time for the LDMOS device

4 Conclusion

In this paper, a kind of new N-LDMOS with step gate oxide is presented. The simulation results demonstrate that the novel structure can restrain the hot-carrier effect effectively, and it is found that the hot hole injection into the gate oxide dominates the channel degradation. At the same time, in order to maintain the basic characteristic parameters of the N-LDMOS, an optimal length of the thick oxide part is selected through TCAD simulations. Finally, the threshold voltage and the saturated drain current are chosen as the indicator so as to measure the performance of the device. The measurement results show that the adoption of step gate oxide in the novel N-LDMOS can result in a longer device lifetime.

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带阶梯栅氧的 N-LDMOS 晶体管热载流子退化分析

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摘要： 为了减小高压 N-LDMOS 器件的热载流子效应并维持其开态特性，提出了一种带有阶梯栅氧的新型 N-LDMOS 器件结构. 与传统的 N-LDMOS 器件相比，其栅极下方 Si-SiO_2 界面处的电场强度明显减弱，因而可以有效地减少器件的热载流子效应，而该阶梯栅氧结构可以通过功率集成电路工艺中普遍采用的栅氧生长方法进行 2 次栅氧生长来获得. 采用 TCAD 仿真技术对传统的 N-LDMOS 器件和所提出的新型 N-LDMOS 器件的热载流子退化现象进行了对比和分析，并在维持原有器件特性参数的基础上得出了新型 N-LDMOS 器件中厚栅氧部分的最优长度. 最后，通过选取某些特性参数进行了实际的器件退化测试，结果表明该新型 N-LDMOS 器件的热载流子退化现象得到了很大的改善.

关键词： 热载流子；退化；阶梯栅氧；N 型横向双扩散金属氧化物半导体管
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