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Application study of dynamic voltage scaling policies

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Abstract: Based on the fundamental relationship among the circuit power, the circuit delay and the supply voltage, four theorems associated with the application of dynamic voltage scaling (DVS) policies are proposed and proved. First, the existence characteristics of the optimal supply voltage for a single task are proved, which suggests that the optimal supply voltage for the single task should be selected only within a one-dimensional term, and the corresponding task end time by the optimal supply voltage should be identical with its deadline. Then, it is pointed out that the minimum energy consumption that the DVS policy can obtain when completing a single task is certainly lower than that of the dynamic power management (DPM) policy or the combined DVS + DPM policy under the same conditions. Finally, the theorem of energy consumption minimization for a multi-task group is proposed, which declares that it is necessary to keep the processor in the execution state during the whole task period to obtain the minimum energy consumption, while satisfying the deadline constraints of any task.

Key words: dynamic voltage scaling; dynamic power management; circuit power; circuit delay

The minimization of power consumption is one of the most critical and challenging problems in embedded and portable systems. Nowadays, the DPM and the DVS have emerged as popular solutions to minimize the power consumption during the system design. The DPM is a design methodology that dynamically determines the power state of power manageable components according to the variations in workloads. As a subject of intense study in the past decade, many DPM polices have been presented, such as timeout-based[1-2], predictive[3-4], and stochastic[5-6]. On the other hand, with the impressive development in power supply technology along with chips that have the ability to reliably operate over a wide range of working voltages, the supply voltage for processor cores can be continuously adjusted at run time based on processing load variations[7]. The DVS is inherently a technique to dynamically scale the supply voltage according to the deadline of tasks with the purpose of balancing real-time responsiveness with low-energy task execution.

There are a number of DVS policies proposed in the literature[8-9], and the experiments demonstrate that the energy-saving performance of the DVS outperforms that of the DPM. However, the superiority of DVS policies cannot be validated by theoretical proof. Four theorems are presented altogether by strict theorem proving, which are helpful for future theoretical study and application development.

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1 Theoretical Background

1.1 Circuit power

The power consumption in the CMOS circuit consists of the static power and the dynamic power. The former is due to the leakage current, while the latter is caused by the energy transferred from supply nodes to the capacitive load connected to the output of the gate. The static power is negligible with respect to the dynamic power. This is why most research groups have devoted themselves to reducing the dynamic power. The dynamic power can be presented by

$$p = aC_1V_d^2 f \tag{1}$$

where p, a, C_1, V_d, f are the dynamic power, the switching activity, the workload capacitance, the supply voltage and the clock frequency, respectively. The power of a device is the sum of each CMOS circuit power.

1.2 Circuit delay

Reducing the supply voltage will increase the circuit delay. To be more accurate, the relationship between the circuit delay T_{cd} and the supply voltage can be represented as

$$T_{cd} = k\frac{V_d}{(V_d - V_t)^2} \tag{2}$$

where k is a constant, and V_t is the threshold voltage. So, T_{cd} will increase when decreasing V_d, which means that the clock speed of the processor will be reduced.

According to Eqs. (1) and (2), it is obvious that the power consumption of a processor is proportional to $V_d(V_d - V_t)^2$, which can be formulated as $P(V_d) = KV_d(V_d - V_t)^2$, where $P(V_d)$ is the power consumption by V_d, and K is a simplified constant.

Moreover, the following formula can be deduced from Eq. (2):

$$E(V_1) = \frac{(V_2 - V_t)^2}{V_2}\frac{V_1}{(V_1 - V_t)^2}E(V_2)$$

where $V_i\,(i = 1, 2)$ represents various supply voltages, and $E(V_i)\,(i = 1, 2)$ corresponds to the task completion time at V_i.

For the sake of simplicity, $V_d \gg V_t$ is assumed, which is a reasonable approximation for V_d in the voltage range [3.3 V, 5 V]. Hence, $P(V_d)$ and $E(V_1)$ can be approximated by

$$P(V_d) = KV_d^3 \tag{3}$$

$$E(V_1) = \frac{V_2}{V_1}E(V_2) \tag{4}$$

Eqs. (3) and (4) will be applied in the following proof of

theorems.

2 Proof of Theorems

Four theorems are presented based on the fundamental relationship among the circuit power, the circuit delay and the supply voltage. The assumptions related to the task and processor are as follows: 1) The task has arrival time S and deadline D. The task in this context means the independent software which can be scheduled by the operating system; 2) The supply voltage range for the processor is $[V_{\min}, W_{\max}]$, in which the voltage or clock speed variation is instantaneous without loss of energy. Moreover, the task can be completed by D in the whole voltage range of $[V_{\min}, W_{\max}]$; 3) The processor supports the sleep mode S_{sp}, as well as the normal active state S_{act}. The power consumption in the sleep mode is denoted as P_{sp}; 4) The switching energy W_{tran} and the switching time T_{tran} between S_{act} and S_{sp} are nonnegligible.

Theorem 1 On the premise that the task can be completed by its deadline D, and the corresponding optimal voltage V_{opt} should follow Eq. (5) when the minimum energy is expected.

$$S + E(V_{opt}) = D \tag{5}$$

The detailed proof is omitted due to the space limitation.

In fact, theorem 1, including most existing DVS policies, has made an implicit assumption that any task is only executed at the one-dimensional supply voltage during the whole execution period. Now the question whether theorem 1 is still true when the task is executed at multiple supply voltages should be answered.

Theorem 2 Assuming that the task is completed during a time interval $[S', D']$ ($[S', D'] \subseteq [S, D]$), the energy consumption at the one-dimensional supply voltage is less than the corresponding energy consumption at random multi-dimensional supply voltages.

Proof Theorem 2 can be proved by the inductive method. The one-dimensional supply voltage and the corresponding completion time are denoted as V_d and E_d, i. e., $E_d = D' - S'$.

First, a two-dimensional supply voltage set where the task will be executed is discussed.

Assume that there exists a two-dimensional voltage set $V = \{V_1, V_2\}$, at which the minimum energy the processor can obtain during $[S', D']$ would be less than the corresponding energy at V_d. Obviously, $V_1 \neq V_2$ and $V_1 > 0$, $V_2 > 0$. The result whether the voltage set V exists will be judged.

Suppose that the corresponding execution time period at V_i is $E_i (i = 1, 2)$, as shown in Fig. 1. Here, $V_1 < V_d < V_2$ is assumed.

Obviously, the following equality is certainly true:

$$E_1 + E_2 = E_d \tag{6}$$

As far as the code-executing amount is concerned, the code amount executed by the processor during E_1 is $E_1 / E(V_1)$ when the whole code amount of task is normalized to one. Similarly, the code amount executed by the processor during E_2 is $E_2 / E(V_2)$. Because the task is completed during $[S', D']$, $E_1 / E(V_1) + E_2 / E(V_2) = 1$. Substituting

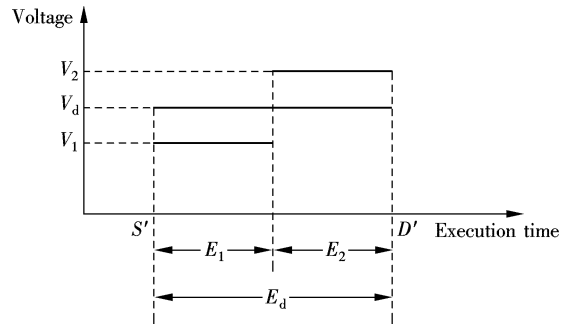

Fig. 1 Example of the two-dimensional supply voltage set

$V_d E_d / V_1$ into $E(V_1)$, and $V_d E_d / V_2$ into $E(V_2)$, we obtain

$$E_1 V_1 + E_2 V_2 = E_d V_d \tag{7}$$

According to Eqs. (6) and (7), the solution to E_1 and E_2 is as follows:

$$E_1 = \frac{V_2 - V_d}{V_2 - V_1} E_d, \quad E_2 = \frac{V_d - V_1}{V_2 - V_1} E_d$$

The total energy consumption W during $[S', D']$ at voltage set V can be calculated as

$$W = KV_1^3 E_1 + KV_2^3 E_2 = KE_d \frac{V_1^3 (V_2 - V_d) + V_2^3 (V_d - V_1)}{V_2 - V_1} \tag{8}$$

The voltage set V can be found by taking the partial derivative of Eq. (8) and setting $\partial W / \partial V_1$, $\partial W / \partial V_2$ to zero, which can be presented as

$$\left.\begin{aligned} \frac{\partial W}{\partial V_1} &= (V_2 - V_d) \frac{3V_1^2 V_2 - 2V_1^3 - V_2^3}{(V_2 - V_1)^2} = 0 \\ \frac{\partial W}{\partial V_2} &= (V_d - V_1) \frac{V_1^3 + 2V_2^3 - 3V_1 V_2^2}{(V_2 - V_1)^2} = 0 \end{aligned}\right\}$$

It is obvious that the above system of equations has no solution with the condition $V_1 \neq V_2$. That is to say, we cannot find any two-dimensional voltage set V where the minimum energy consumption is less than the corresponding energy consumption at V_d. So, theorem 2 holds corresponding to a two-dimensional voltage set.

Assuming that theorem 2 is true with the $(N-1)$-dimensional voltage set. Next we will consider the case of the N-dimensional voltage set.

Denote the N-dimensional voltage set as $V = \{V_1, V_2, \ldots, V_{N-1}, V_N\}$, and the corresponding execution time set is expressed as $E = \{E_1, E_2, \ldots, E_{N-1}, E_N\}$, which satisfies $\sum_{1 \leqslant i \leqslant N} E_i = E_d$. Then the total energy consumption under the voltage set V can be calculated as

$$W = \sum_{1 \leqslant i \leqslant N} KV_i^3 E_i = \sum_{1 \leqslant i \leqslant N-1} KV_i^3 E_i + KV_N^3 E_N$$

There surely exists an equivalent voltage $\tilde{V}$, where the code-executing amount during $\sum_{1 \leqslant i \leqslant N-1} E_i$ is equal to the sum of the code amount executed at $V_i (i = 1, 2, \ldots, N-1)$ during the specified period E_i. Generalizing formula (7), the

following equality is obtained:

$$\sum_{1\leqslant i\leqslant N-1} E_i V_i = \tilde{V} \sum_{1\leqslant i\leqslant N-1} E_i = \tilde{V}\tilde{E} \qquad \tilde{E} = \sum_{1\leqslant i\leqslant N-1} E_i$$

According to the assumption corresponding to the $(N-1)$-dimensional voltage set, the following inequality holds:

$$\sum_{1\leqslant i\leqslant N-1} KV_i^3 E_i > K\tilde{V}^3 \tilde{E} \tag{9}$$

Similarly, the N-dimensional voltage set is equivalent to a two-dimensional voltage set $V = \{\tilde{V}, V_N\}$ in terms of the code-executing amount with $\tilde{E}\tilde{V} + E_N V_N = E_d V_d$. Based on the above result related to the two-dimensional voltage set, we obtain

$$K\tilde{V}^3\tilde{E} + KV_N^3 E_N > KV_d^3 E_d \tag{10}$$

According to (9) and (10), the following inequality can be deduced:

$$\sum_{1\leqslant i\leqslant N} KV_i^3 E_i = \sum_{1\leqslant i\leqslant N-1} KV_i^3 E_i + KV_N^3 E_N > K\tilde{V}^3\tilde{E} + KV_N^3 E_N > KV_d^3 E_d$$

So, theorem 2 still holds with an N-dimensional voltage set.

In the remainder of this paper, any task is assumed to be executed at a one-dimensional voltage without special declaration.

Theorem 3 Assuming that the task is completed exactly during $[S', D']$ ($[S', D'] \subseteq [S, D]$), the minimum energy consumption that the DVS policy can obtain during $[S', D']$ is lower than that of the DPM policy or the combined DVS + DPM policy. Here, all the policies are abstract.

Proof The first step is to calculate the corresponding minimum energy value that the three policies can obtain during $[S', D']$.

The minimum energy of the DVS policy, denoted as W_{min1}, can be calculated as follows.

According to Eq. (5), we can draw the conclusion that V_x should satisfy $S' + E(V_x) = D'$ for the minimum energy. Hence, W_{min1} can be easily calculated as

$$W_{min1} = KV_x^3 (D' - S') \tag{11}$$

With regard to the DPM policy, the optimal approach for executing the task during $[S', D']$ is to keep the processor at V_{max} until the task is completed and then immediately switch the processor to S_{sp}. In this scenario, the energy consumption is minimum, and it can be expressed as

$$W_{min2} = KV_{max}^3 E_0 + W_{tran} + P_{sp}(D' - S' - E_0 - T_{tran}) \qquad D' - S' - E_0 \geqslant T_{be} \tag{12}$$

where E_0 is the completion time at V_{max}, and T_{be} is the break-even time between S_{sp} and S_{act} ($T_{be} \geqslant T_{tran}$ [3]).

An intuitive approach for the combined DVS + DPM policy is that the task will be executed at an intermediate voltage V_{mid}, which is chosen from $[V_{min}, V_{max}]$ with $D' - S' - E(V_{mid}) \geqslant T_{be}$, and then immediately switch the processor to the lower energy state S_{sp} once the task is completed. More precisely, the switching time is at the moment $S' + E(V_{mid})$.

It is established that $V_{mid} \in [E^{-1}(D' - S' - T_{be}), V_{max}]$, where E^{-1} represents the reverse function. Denote the execution time at the supply voltage V_{mid} as E_{mid}. Thus, the overall energy consumption W_{all} during $[S', D']$ is given by

$$W_{all} = KV_{mid}^3 E_{mid} + W_{tran} + P_{sp}(D' - S' - E_{mid} - T_{tran})$$

Substituting $V_{max}E_0/V_{mid}$ into E_{mid}, we obtain

$$W_{all} = K V_{max} E_0 V_{mid}^2 + W_{tran} + P_{sp}\left(D' - S' - \frac{V_{max}E_0}{V_{mid}} - T_{tran}\right)$$

It indicates that W_{all} is a monotonically increasing function of V_{mid}. When $V_{mid} = E^{-1}(D' - S' - T_{be}) = V_{max}E_0/(D' - S' - T_{be})$, the minimum energy value denoted as W_{min3} is obtained, as shown in Eq. (13). It is interesting that W_{all} will reach its maximum value W_{min2} if $V_{mid} = V_{max}$. Hence, the DPM policy can be regarded as a special case of the combination policy.

$$W_{min3} = \frac{KE_0^3 V_{max}}{(D' - S' - T_{be})^2} + W_{tran} + P_{sp}(T_{be} - T_{tran}) \tag{13}$$

The second step is to make a brief comparison among the three minimum energy values. The detailed comparison is omitted due to the space limitation.

In summary, it is ture that $W_{min1} < W_{min3} \leqslant W_{min2}$. So theorem 3 holds.

The above theorems are given in the context of a single task, which is not applicable to most practical cases. The following theorem will consider the multi-task group. Denote the arrival time and the deadline of the i-th task as S_i and D_i, respectively.

Theorem 4 Given the n tasks with $D_i \geqslant S_{i+1}$ ($i = 1, 2, \ldots, N-1$), it is necessary to keep the processor in the execution state during the whole period $[S_1, D_N]$ to obtain the minimum energy consumption, where the deadline constraint of any task should be satisfied.

Proof Using theorem 3, theorem 4 can be proven by the method of reduction to absurdity.

As one possible processing case, the processor can be assumed to enter the idle state when executing the i-th task and the $(i+1)$-th task($1 \leqslant i \leqslant N-1$), as shown in Fig. 2, where the body of oblique lines represents the execution period of corresponding tasks under V_{max}. It is shown that the i-th task will be executed at V_i during $[S_i, t_0]$, and the $(i+1)$-th task will be executed at V_{i+1} during $[t_1, D_{i+1}]$, respectively. However, the processor will enter the idle state during $[t_0, t_1]$. That is to say, the process is idle during $[t_0, t_1]$.

Since $t_1 < D_i$ as shown in Fig. 2, V_i can be decreased to V_i' as far as the i-th task is concerned, which follows $S_i + E(V_i') = t_1$. According to Eqs. (3) and (4), the energy consumption at V_i' during $[S_i, t_1]$ is $K(V_i')^2 V_{max}E(V_{max})$, which is less than the energy consumption at V_i during $[S_i, t_0]$, i. e., $KV_i^2 V_{max}E(V_{max})$. Furthermore, we can deduce from theorem 3 that the energy consumption at V_i' during $[S_i, t_1]$ is surely less than the sum of energy consumption

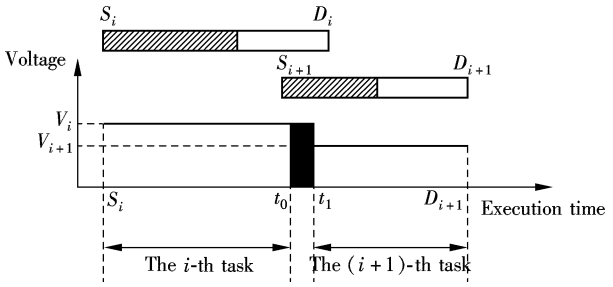

Fig. 2 The execution process of task

during $[S_i, t_0]$ and $[t_0, t_1]$, and suppose that the optimal DPM policy is applied during $[t_0, t_1]$. Although there is no mention of T_{be}, an implicit assumption $t_1 - t_0 \geqslant T_{be}$ is made. Otherwise, the processor will always stay in working state S_{act} during $[t_0, t_1]$ with more energy wasted when the DPM policy is applied.

For other possible execution processes, it can also be proved that the idle period can be occupied by a certain task for more power saving. In other words, the processor cannot enter the idle state during the whole period $[S_1, D_N]$. This completes the proof of theorem 4.

It should be noted that theorem 4 holds only when $D_i \geqslant S_{i+1}$, which means that there is no time interval between the deadline of a previous task and the arrival time of a later task.

3 Conclusion

Four theorems are presented and proven by the strict theorem proof based on the fundamental relationship among the circuit power, the circuit delay and the supply voltage. Even though great progress has been made in the DVS technique during the past decade, the design and analysis of policy optimization techniques about the power management are still open for research. For example, battery-aware DVS policies need be further investigated.

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动态电压调节策略的应用研究

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摘要:基于电路功耗、电路延迟与工作电压之间的基本关系式,提出并证明了与 DVS 策略应用相关的 4 个定理. 首先,针对单任务证明了最优工作电压的存在特性,即只需在一维电压的范畴内为单任务选择某个最优工作电压,且该电压所对应的任务结束时间必须与任务的截止期限保持一致. 然后指出在同等条件下,DVS 策略执行单任务所能达到的最小能耗必低于 DPM 策略或者 DVS 和 DPM 结合策略所对应的最小能耗. 最后,针对多任务组提出了能耗最小化定理,指出在满足所有任务截止期限的前提下,处理器能耗最小化的必要条件是处理器必须在整个任务段期间一直处于执行任务的状态.

关键词:动态电压调节; 动态电源管理; 电路功耗; 电路延迟

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