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A wideband low-phase-noise LC VCO for DRM/DAB frequency synthesizer

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Abstract: The wideband CMOS voltage-controlled oscillator (VCO) with low phase noise and low power consumption is presented for a DRM/DAB (digital radio mondiale and digital audio broadcasting) frequency synthesizer. In order to obtain a wide band and a large tuning range, a parallel switched capacitor bank is added in the LC tank. The proposed VCO is implemented in SMIC 0.18-μm RF CMOS technology and the chip area is 750 μm × 560 μm, including the test buffer circuit and the pads. Measured results show that the tuning range is 44.6%; i.e., the frequency turning range is from 2.27 to 3.57 GHz. The measured phase noise is –122.22 dBc/Hz at a 1 MHz offset from the carrier. The maximum power consumption of the core part is 6.16 mW at a 1.8 V power supply.

Key words: CMOS voltage-controlled oscillator; switched capacitor bank; MOS varactors; wideband; low phase noise; DRM/DAB frequency synthesizer

With the development of wireless communication technology, multi-standard portable terminals become a research focus. The receiver should be compatible with various wireless communication standards covering the frequency range from several hundred kHz to several GHz. Thus, the RF front-end should be compatible with various wireless communication standards and bands.

The digital radio mondiale (DRM)[1] and the digital audio broadcasting (DAB)[2] have been introduced as digital standards for radio broadcasting covering different frequency bands. The DRM covers the frequency range from 148 kHz to 27 MHz, and DRM+ added in the latest version is up to 108 MHz. The DAB covers two different bands, band Ⅲ (174 to 240 MHz) and band L (1.452 to 1.492 GHz). The DRM/DAB-based RF front-end should be compatible with DRM and DAB and cover all of their frequency bands. Thus, a broadband frequency synthesizer structure with a single VCO, a single loop filter, and a double conversion low-IF DRM/DAB radio tuner architecture are selected[3]. For such an application, the wideband voltage-controlled oscillators (VCO) in the frequency synthesizer should be of low phase noise and low power consumption throughout the entire frequency tuning range, while consuming a small chip area.

The band of a voltage-controlled oscillator (VCO) determines the frequency locking range of a frequency synthesizer. For the large frequency locking range of a frequency synthesizer, the band of the VCO should be as wide as possible. A CMOS VCO is commonly implemented using a varactor-tuned LC resonator. The ratio of the maximum to minimum capacitance of a typical varactor in CMOS technology is around 4 to 6, which in turn limits the frequency tuning range to a ratio of approximately 2 to 2.5[4]. Due to the limited tuning range of the varactors, a single LC resonator cannot produce enough frequency tuning range. To extend the frequency locking range, the LC-tank VCO can employ a parallel switched capacitor bank. Moreover, as is common with all the designs which include switch arrays, the parasitic capacitance of the switch limits the frequency tuning range. Once again, the switched parasitic capacitance and loss can degrade the tuning range and phase noise, respectively.

In this paper, a wideband VCO with low phase noise and low power consumption is designed for the DRM/DAB frequency synthesizer. Optimization of bandwidth while maintaining low phase noise and low power consumption is discussed.

1 Circuit Design

Fig. 1 shows the schematic of the proposed oscillator. It uses a double cross-coupled transconductance structure without a tail current source, which is usually preferred in low power and low phase noise applications. It consists of 4 parts, including a double cross-coupled transconductance circuit, an LC tank, two LC filter networks[3], and two isolation circuits for output nodes. The loss of the LC tank is canceled by the double cross-coupled transconductance

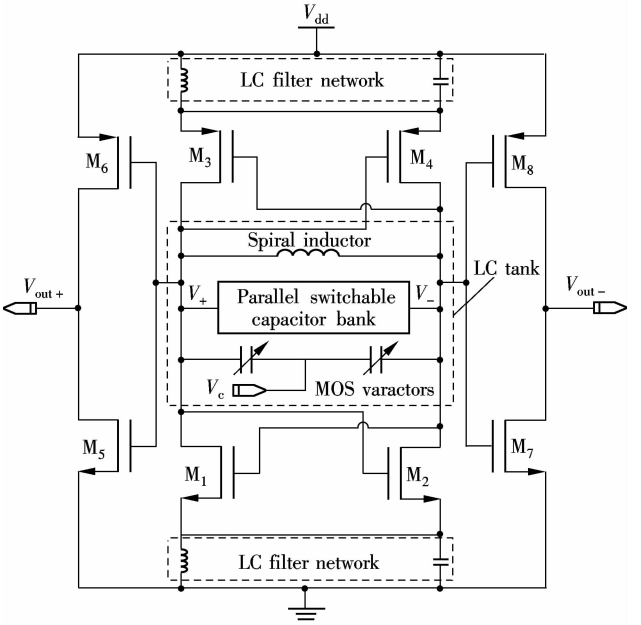

Fig. 1 Schematic of the proposed VCO

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circuit through generating a negative resistance. The LC tank consists of a spiral inductor, two MOS varactors, and a parallel switched capacitor bank. The band width of the proposed VCO is controlled by the LC tank. The parallel switched capacitor bank is used to change the control codes, and it is a 4-bit coarse tuning element. The two MOS varactors are used to change the control voltages, and they are fine-tuning elements.

The oscillation process of the proposed VCO in Fig. 1 is described as follows. Initially, both the static output voltage and the static current flowing in two sides are set by the size of the MOSFETs. The nominal output (V_+, V_-) bias point is 0.9 V and the circuit draws a static supply current of about 3.8 mA, which is enough for an oscillation. Then, when the circuit begins to oscillate, it operates in the voltage-limited region along the entire tuning range. The supply current peaks coincide with the positive and negative peaks of the output voltage and thus vary around $2\omega_0$. The average supply current is about 4.4 mA.

2 Analysis of Band Width

The bandwidth of the proposed VCO is determined by the LC tank. The equivalent circuit of the proposed LC tank is shown in Fig. 2. Its oscillation frequency is given by

$$f_{\text{osc}} = \frac{1}{2\pi \sqrt{L(C_{\text{v}}/2 + C_{\text{bank}} + C_{\text{para}})}} \tag{1}$$

where C_{v} and C_{bank} are the capacitances of the varactor and the switched capacitor bank, respectively; C_{para} is the parasitic capacitance.

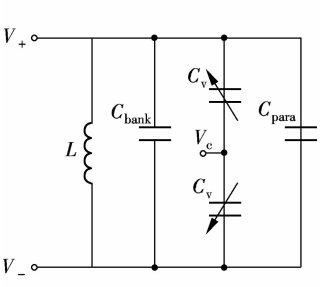

Fig. 2 Equivalent circuit of the proposed LC tank

From Eq. (1), it can be seen that the frequency range of the proposed VCO is controlled by the capacitance of the parallel switched bank and the varactors. The schematic of the parallel switched capacitor bank is shown in Fig. 3. The C_{bank} is given by

$$C_{\text{bank}} = \frac{D_0 C}{2} + D_1 C + 2D_2 C + 4D_3 C \tag{2}$$

where D_0, D_1, D_2, and D_3 are the control words of the switched capacitor bank with values of 1 or 0.

The structure of the MOS varactor is an n-type MOS.

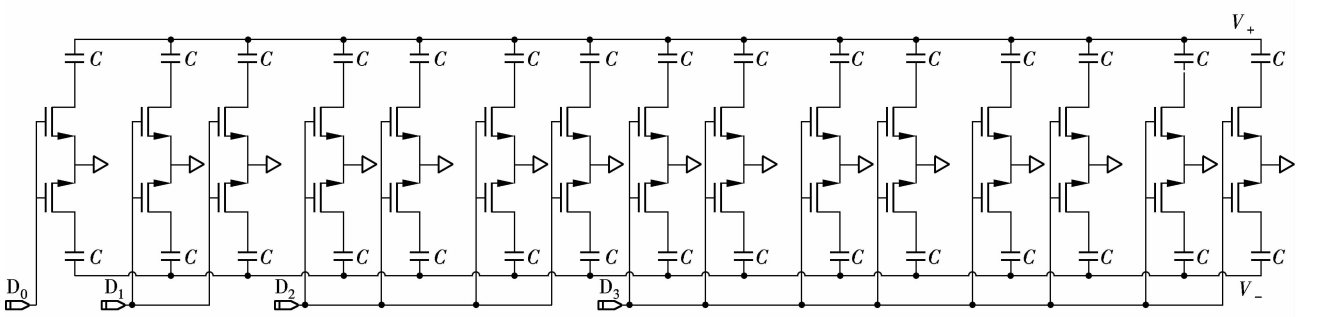

Fig. 3 Schematic of the parallel switched capacitor bank

The structure is very similar to an n-type MOSFET, except that both the channel and source/drain regions are doped with the same dopant, which is n-type in this case. The varactors have three modes of operation: accumulation, depletion, and inversion. The capacitance of the device depends on the value of V_{c}. The C_{v} curves of the proposed varactor are shown in Fig. 4. Thus, the gain of the proposed VCO is given by

$$K_{\text{VCO}} = \frac{\partial f_{\text{osc}}}{\partial V_{\text{c}}} = -\frac{1}{4\pi \sqrt{L}(C_{\text{v}}/2 + C_{\text{bank}} + C_{\text{para}})^{1.5}} \frac{\partial C_{\text{v}}}{\partial V_{\text{c}}} \tag{3}$$

According to Eq. (1), the maximum and minimum oscillation frequencies can be written as

$$f_{\text{oscmax}} \approx \frac{1}{2\pi \sqrt{L(C_{\text{vmin}}/2 + C_{\text{para}})}} \tag{4}$$

$$f_{\text{oscmin}} \approx \frac{1}{2\pi \sqrt{L(C_{\text{vmax}}/2 + 7.5C + C_{\text{para}})}} \tag{5}$$

The tuning range of the proposed oscillation is given as

$$R_{\text{T}} = 2\frac{f_{\text{oscmax}} - f_{\text{oscmin}}}{f_{\text{oscmax}} + f_{\text{oscmin}}} = 2\frac{\sqrt{C_{\text{vmax}}/2 + 7.5C + C_{\text{para}}} - \sqrt{C_{\text{vmin}}/2 + C_{\text{para}}}}{\sqrt{C_{\text{vmax}}/2 + 7.5C + C_{\text{para}}} + \sqrt{C_{\text{vmin}}/2 + C_{\text{para}}}} \tag{6}$$

According to Eqs. (4) and (6), the highest oscillation

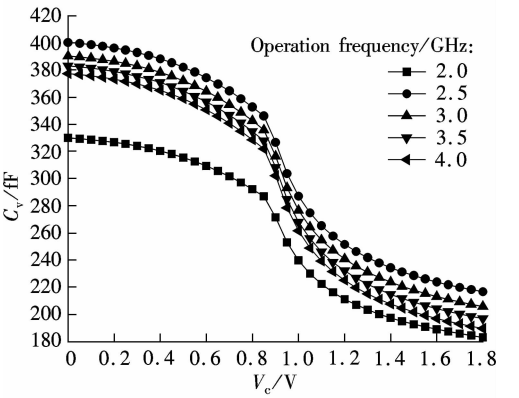

Fig. 4 C_{v} curves of the proposed varactor

frequency is mainly determined by the inductor and the MOS varactors in the LC tank. The tuning range is determined by the capacitance ratios of the MOS varactors and the parallel switched capacitor bank. Thus, the optimization of bandwidth is focused on the inductor, the MOS varactors, and the switched capacitor bank. According to the demands of DRM/DAB frequency synthesizers and SMIC 0.18-μm RF CMOS technology, the turn number and the radius of the inductor are 3 and 80 μm, respectively; the width and length of the MIM capacitor are 13 and 12 μm, respectively; the number of gate fingers of the MOS varactors is 10.

3 Optimization of Phase Noise

According to the Abidi model[5], $1/f^2$ phase noise can be written as

$$L(\Delta\omega) = \frac{8FkTR}{V_0^2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{7}$$

$$F = 1 + \frac{4RI\gamma}{\pi V_0} + \frac{4}{9}g_m R\gamma \tag{8}$$

where γ is the noise factor.

According to Eqs. (7) and (8), the structure of the proposed LC-VCO, a double cross-coupled transconductance structure without a tail current source has better performance compared with traditional structures. On the other hand, substrate noise and power noise are important sources of phase noise. In order to restrain substrate noise and power noise, one LC filter network is inserted between a PMOS cross-coupled transconductance circuit and power; the other LC filter network is inserted between an NMOS cross-coupled transconductance circuit and ground[3]. Thus, the resonant frequency of the two LC filter networks can be written as

$$f \approx 2f_o \tag{9}$$

where f_o is the average of the LC-VCO oscillation frequencies.

Based on the above analyses and the simulation results, the turn number and the radius of the inductor are 3 and 30 μm, respectively; the width and length of the MIM capacitor both are 15 μm. Fig. 5 shows the simulation results when the control voltage is 1.4 V and the control code is "0001".

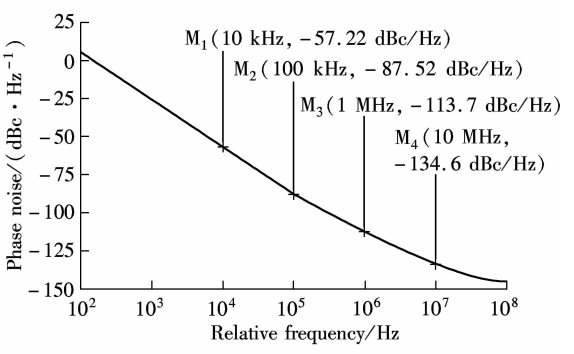

Fig. 5 Simulation results of the proposed VCO phase noise

4 Measured Results

The wideband low-phase-noise VCO is implemented in SMIC's 0.18-μm RF CMOS technology. Fig. 6 shows the microphotograph of the realized chip. The chip area is 750 μm × 560 μm, including the test buffer circuit and the pads.

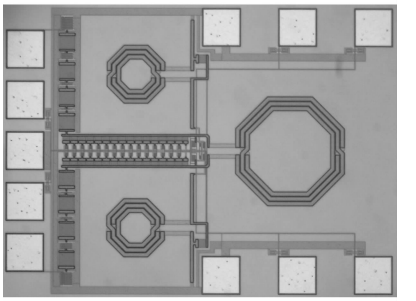

Fig. 6 Microphotograph of the proposed VCO

The f-V curve of the proposed VCO is measured as a function of the control codes of the parallel switched capacitor bank. The results are shown in Fig. 7. Compared with Fig. 4, K_{VCO} of the proposed VCO is less than the change rate of the MOS varactor because of the influence of the LC tank. It decreases with the control codes changing from "0000" to "1111". This is consistent with Eq. (3).

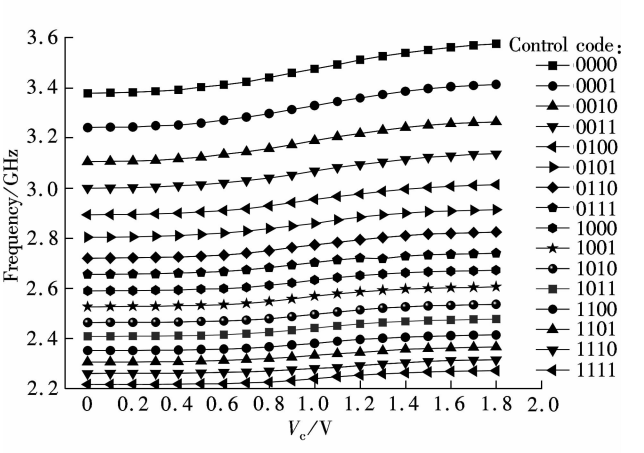

Fig. 7 Measured f-V curves of the proposed VCO

The phase noise is measured by using an Agilent E4440A spectrum analyzer. To measure the phase noise, the control voltage is 1.4 V and the control code is "0001". The oscillation frequency is 3.385 GHz. The phase noise of the output is measured to be 120.22 dBc/Hz at 1 MHz offset from the carrier as shown in Fig. 8. Compared with Fig. 5, the measured phase noise is better than the simulated one. The

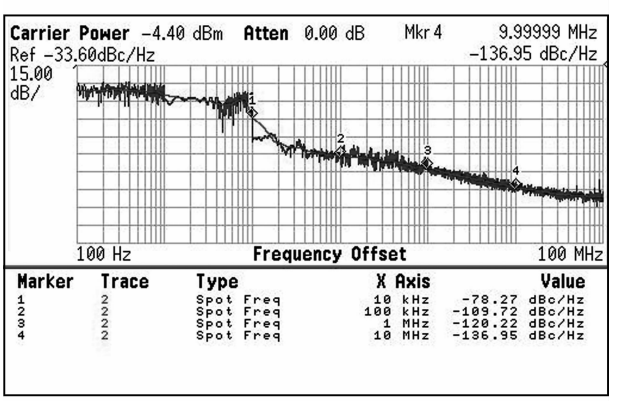

Fig. 8 Measured phase noise of the proposed VCO

reason is that the Agilent E4440A spectrum analyzer has a filter in its input port.

Measured results show that its tuning range is 44.6%; i.e., the frequency turning range is from 2.27 to 3.57 GHz. The core power consumption is 6.16 mW at a 1.8 V power supply. Comparing the proposed VCO with those in other recent papers shown in Tab. 1, it has the largest FoM[9], $\mathrm{FoM} = 10\log\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{L\{\Delta\omega\}P}\right]$.

Tab. 1 Comparison with published results

Reference	CMOS technology/μm	Oscillation frequency/GHz	Tuning range/%	Phase noise/(dBc · Hz^{-1})	Power/mW	FoM/dBc
Ref. [6]	0.13	6.0	5.1	−115.2@1 MHz	12.5	179.8
Ref. [7]	0.18	1.7	63.1	−128.0@1.25 MHz	14.0	179.2
Ref. [8]	0.18	1.8	66.7	−130.0@1.45 MHz	41.4	175.7
Ref. [9]	0.18	5.2	18.0	−113.7@1 MHz	9.7	180.0
This work	0.18	3.385	44.6	−120.22@1 MHz	6.6	182.6

5 Conclusion

Optimization of a wideband LC VCO with low phase noise and low power consumption is presented. The measured results show that the proposed VCO is of wide band, low phase noise and low power consumption. Its performance meets the requirements of DRM/DAB frequency synthesizers.

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一种应用于 DRM/DAB 频率综合器的宽带低相位噪声 LC 压控振荡器

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摘要:介绍了一种应用于 DRM/DAB 频率综合器的宽带低相位噪声低功耗的 CMOS 压控振荡器. 为了获得宽工作频带和大调谐范围,在 LC 谐振腔里并联一个开关控制的电容阵列. 所设计的压控振荡器应用中芯国际的 0.18 μm RF CMOS 工艺进行了流片实现. 包括测试驱动电路和焊盘,整个芯片面积为 750 μm×560 μm. 测试结果表明,该压控振荡器的调谐范围为 44.6%,振荡频率范围为 2.27~3.57 GHz. 其相位噪声在频偏为 1 MHz 时为 −122.22 dBc/Hz. 在 1.8V 的电源电压下,其核心的功耗为 6.16 mW.

关键词:CMOS 压控振荡器;开关电容阵列;MOS 可变电容; 宽带;低相位噪声;DRM/DAB 频率综合器

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