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Design of 0.5 V low-voltage phase and frequency detector for frequency synthesizer in wireless sensor networks

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Abstract: Based on 0.13 μm complementary metal-oxide-semiconductor (CMOS) technology, a phase and frequency detector (PFD) is designed with a low supply voltage of 0.5 V for frequency synthesizers used in wireless sensor networks (WSNs). The PFD can compare the frequency and phase differences of input signals and deliver a signal voltage proportional to the difference. Low threshold transistors are used in the circuits since a power supply of 0.5 V is adopted. A pulse latched structure is also used in the circuits in order to increase both the detection range of phase errors and the maximum operation frequency. In experiments, a phase error with a range from −358° to 358° is measured when the input signal frequency is 2 MHz. The PFD has a faster acquisition speed compared with conventional digital PFDs. When the input signals are at a frequency of 2 MHz with zero phase error, the circuits have a power consumption of 1.8 μW, and the maximum operation frequency is 1.25 GHz.

Key words: phase and frequency detector (PFD); low threshold transistor; pulse latch

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The wireless sensor network (WSN) composed of many sensor nodes is rapidly developing. It has many applications in environment science, traffic control, disaster prediction, and municipal information infrastructure. There are data sampling module, data processing and control module, communication module (including a radio transceiver), power supply module and some other functional modules in each node. Low cost and low power consumption are the basic requirements of the radio transceiver in the WSN. Supply voltage reduction can lead to significant power savings for digital circuits, and the availability of analog and RF circuits compatible with (future) digital requirements largely reduces the complexity and cost of the system chip design and tests[1] in large-scale mixed-mode systems. With CMOS process feature size scaling in the nanometer range, the maximum supply voltage has been steadily decreased. For low power and low standby-power devices, the supply voltage is forecast to decrease to 0.5 V [2-3] in the near future. To reduce power consumption, the power supply of the transceiver chip in our design is set to 0.5 V. Fig. 1 shows the block diagram of a frequency synthesizer which is a key module providing local oscillation frequencies for the transceiver. The PFD which compares the phase and frequency of the input signals plays an important role in the system. According to the requirements of the frequency synthesizer in our designed system, the frequency of the input signal of the PFD is set at 2 MHz. The specifications of the PFD together with the circuits and layout design are explained. The measurement results and the conclusion are provided.

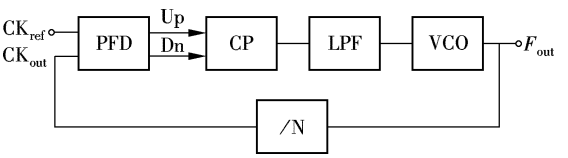

Fig. 1 Diagram of the PFD used in a frequency synthesizer

1 Technical Requirements for PFDs

There are many different structures for designing a PFD, for example, analog multiplier, exclusive-or gates, and the scheme based on reset-set (R-S) latches/two D-type flip-flops. Digital phase-frequency detectors (DPFDs) are usually used to improve the pull-in range and the pull-in time of phase-locked loop (PLL) circuits. DPFDs are especially suitable for frequency-synthesis applications with periodic inputs[4]. The pull-in range and the phase noise of a frequency synthesizer are mainly determined by the performances of the PFD including phase detection characteristics, the dead zone, frequency detection characteristics, the maximum operation frequency, phase noise and power consumption. The DPFD structure based on two D-type flip-flops and its state diagram are shown in Figs. 2(a) and (b). The ideal phase detection characteristic is shown in Fig. 3(a), where the horizontal axis $\Delta\phi$ is the phase difference of the input signals and the vertical axis V is the normalized average voltage of difference of up and down signals ($V_{\mathrm{Up}} - V_{\mathrm{Dn}}$). As shown in Fig. 3, the slope of the curve is the gain of the DPFD, and the phase detection range is from -2π to $+2\pi$. The phase detection range has effects on the lock-in range of the frequency synthesizer. However, due to the time delay of the signal in the reset path shown in Fig. 2 (a), the linear range of phase detection is less than 4π as shown in Fig. 3 (b). The best performance of the PFD is to have a zero dead zone, which is responsible for decreasing phase noise and spurious tone. When the phase error is not zero, the PFD detects a zero phase error and a dead zone occurs. A zero dead zone implies that the PFD can detect any amount of phase error [5].

Fig. 4 shows the frequency detector characteristics of the DPFD at low frequencies [4], where $b = (f_{\mathrm{CKref}} - f_{\mathrm{CKout}})/f_{\mathrm{CKout}}$ when $b > 0$, and $b = (f_{\mathrm{CKout}} - f_{\mathrm{CKref}})/f_{\mathrm{CKref}}$ when $b < 0$. As

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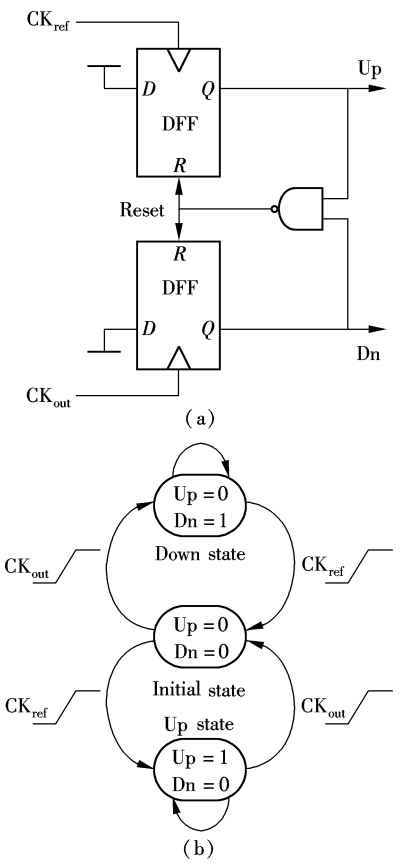

Fig. 2 Illustration of a digital phase and frequency detector. (a) Structure; (b) State diagram

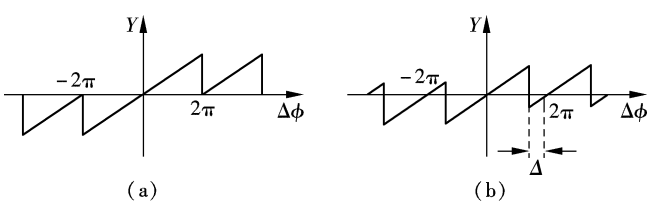

Fig. 3 Phase detection characteristic. (a) Ideal; (b) Non-ideal

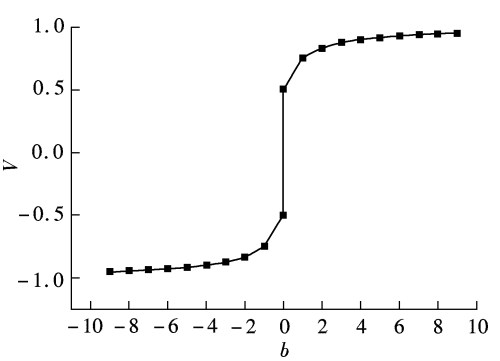

Fig. 4 Relationship of the normalized average output voltage and b at low frequencies in a frequency detector

can be seen from this figure, the DPFD circuits considered above have unlimited frequency acquisition capability when the operation frequency is low enough. However, the voltage controlled oscillator (VCO) and the other loop components in practical PLL circuits will put limits on a pull-in range which can be achieved. During acquisition, the frequency will not monotonically approach a lock-in range because errors may occur periodically in a non-ideal PFD. The acquisition slows down depending on how often the wrong information appears, which depends on $\Delta = 2\pi t_{\text{reset}}/T_{\text{CKref}}$. Note that t_{reset} is obtained from the delay of logic gates in the reset path and is not a function of the input frequency. At an input frequency with $T_{\text{CKref}} = 2t_{\text{reset}}$, which gives $\Delta = \pi$, the PFD delivers the information with errors in half the time, and thus fails to acquire frequencies locked unconditionally. The maximum operation frequency can be expressed as $f_{\text{CKref}} < 1/(2t_{\text{reset}})$. The maximum operation frequency can be found over the shortest period of time with correct up and down signals when the input signals have the same frequencies and π phase differences[6]. The PFD performance is affected by some noise, which is caused by factors such as finite reset time, dead zone and transistors. The analysis of the phase noise was reported previously[7]. Another important parameter in the PFD design is the low power because it is the system requirement of the WSN.

2 Design of Circuits and Layout

In the circuits, we use pulse latches[8] instead of flip-flops which fundamentally change the dependence on the reset time delay (see Fig. 5(a)). When the input signal CK_{ref} arrives during the reset time, the edge information in the rise time of the CK_{ref} propagates to the output as long as the amplitude of the CK_{ref} pulse ($\text{Pulse}_{\text{ref}}$ in Fig. 5(a)) is still low (level-sensitive) after the reset period ends. The PFD no longer loses the signal edge arriving during reset time and does not output a signal indicating a wrong direction. However, since the PFD output becomes active high at the end of the reset, the output pulse width is constant (at a phase error of $2\pi - \Delta$) for phase differences greater than $2\pi - \Delta$. The characteristic of the phase detector is shown in Fig. 5(b). The input clock pulse width W_{in} should be designed to be slightly smaller than t_{reset}; otherwise, the PFD will fail to lock at a zero input phase difference[9]. This PFD failure is due to the fact that the input clock pulse triggering the reset will activate the output after the reset pulse ends for $W_{\text{in}} \geqslant t_{\text{reset}}$. This design criterion results in a negative output voltage for $|\Delta\phi| \geqslant 2\pi - \delta$, where $\delta = 2\pi(t_{\text{reset}} - W_{\text{in}})/T_{\text{CKref}}$ as illustrated in Fig. 5(b).

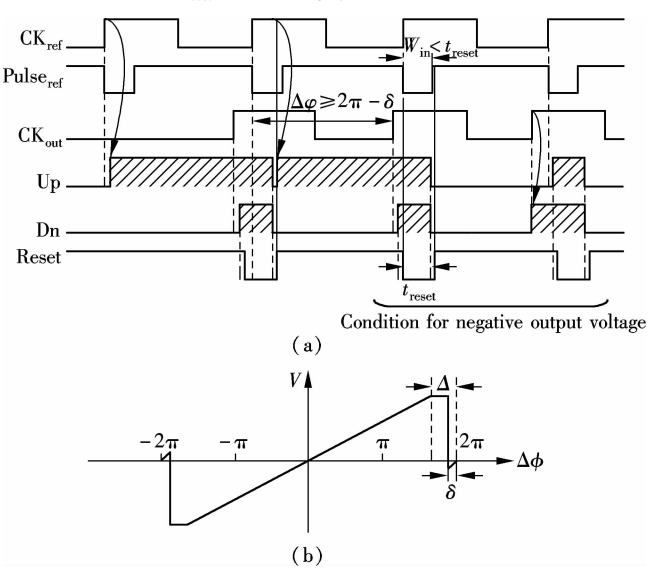

Fig. 5 Behavior of latched-based PFD. (a) Description of the non-ideal behavior; (b) Characteristic of latch-based PFD

It is noted that this PFD has a faster acquisition speed compared with the DFF-based type (with the same operating frequency) because $\delta < \Delta$ and it outputs less incorrect phase information. Also, the phase detection range is $-(2\pi - \delta)$ to $(2\pi - \delta)$ which is greater than the previous DPFD with $-(2\pi - \Delta)$ to $(2\pi - \Delta)$, and the PFD with faster acquisition has a larger lock-in range. However, the PFD has a saturated gain when the input phase difference of the signals is greater than $2\pi - \Delta$.

Fig. 6 illustrates the circuits of the latch-based PFD using glitch latches [9]. In order to operate with a 0.5 V power voltage, low threshold transistors are used in the design. The PFD core enclosed by the dashed lines is divided into two parts (parts Ⅰ and Ⅱ) by the dash-dotted line, as shown in Fig. 6. The symmetry of parts Ⅰ and Ⅱ is important for reducing the dead zone, so the NAND circuit is also divided symmetrically into two parts as shown in Fig. 7. To drive the test equipment in our measurement, body forward bias voltage [10-11] and reverse short channel effect [12] techniques are used in the test buffer circuits to improve the operation speed and reduce the power consumption. The INV_1 and INV_2 are used to latch the output, so that the output signal does not change when the input signal becomes low. The inverted delay elements which contain three inverters control the pulse width W_{in} of the clocks. As shown in Fig. 6, the reset circuit includes two inverters (INV_3) and one NAND. The reset signal also traverses the circuit twice because the reset signal should return to a high level. Therefore, the delay t_{reset} contains three inverter delays (two INV_3 and one inverter of P1 and N5) and two NAND delays. There is no dead zone when the phase difference is 0° at the designed frequency of 2 MHz for the circuits because $W_{in} < t_{reset}$, which is verified by the same narrow pulses of the simulated outputs (Up and Dn in Fig. 6) as shown in Fig. 8. The phase detection range in the simulation for operation at 2 MHz as shown in Fig. 9 (a) is from −359.5° to 359.5°. As the clock period is less than twice the pulse width, the clock pulses from N_1 (N_3) and N_2 (N_4) have no longer a constant width but reduce with the clock period. Therefore, δ is no longer constant and grows with increasing frequency. The PFD fails as the frequency approaches $1/t_{reset}$, which is potentially twice that of the previously proposed PFD for the same t_{reset} because $\delta = 2\pi(t_{reset} - W_{in})/T_{CKref} = 2\pi(t_{reset} - t_{reset}/2)/t_{reset} = \pi$. Consequently, the maximum frequency is higher than the frequency of the DFF-based designs despite the longer t_{reset}. In this circuit, $t_{reset} = 800$ ps, so the maximum operation frequency is 1.25 GHz, and the simulated phase detection range is worked out, which is from −177° to 170° and shown in Fig. 9 (b).

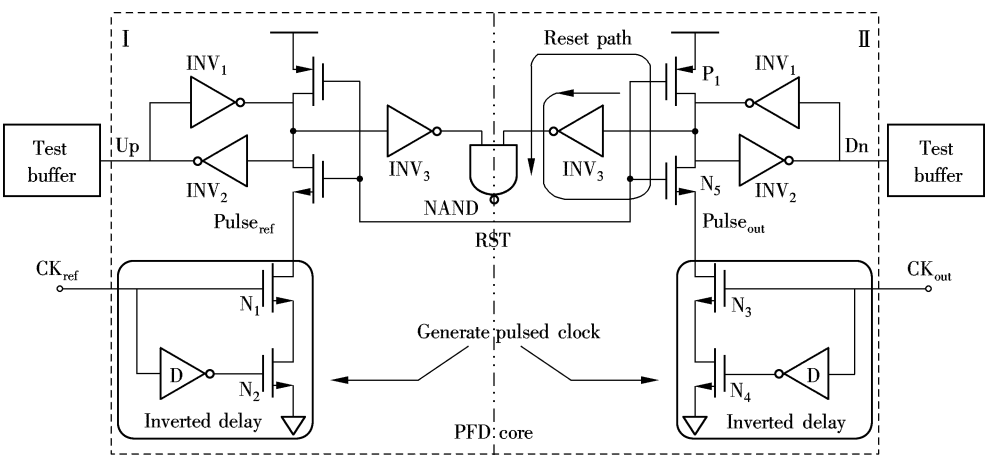

Fig. 6 Latch-based PFD structure

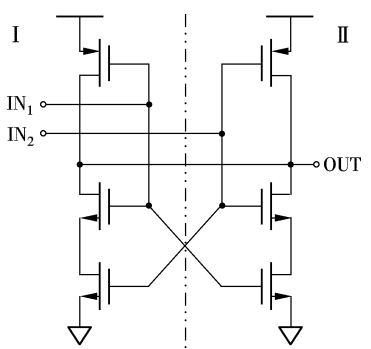

Fig. 7 NAND circuit used in the PFD core

The matching between part Ⅰ and part Ⅱ of the layout is crucial in reducing the spurious tones and the phase noise. The layouts of Part Ⅰ and Part Ⅱ must be identical and close to each other for reducing the random mismatches. The layout of the NAND gate is also divided into two equal parts. The coupling of the Up and Dn signals can increase the error transitions of switches in the charge pump circuits and affect the linearity of the phase detection, so the two signal lines must be kept away from each other. The parasitic of the reset signal has an effect on the increase of t_{reset} and the reduction of the phase detection range, so the signal routings which affect t_{reset} should be as short as possible. The PFD is fabricated in 0.13 μm CMOS process and the area of the PFD core shown in Fig. 10 is 80 μm × 90 μm.

3 Experiment and Measured Results

When the input frequency is 2 MHz, the measured phase detection range is −358° to 358° as shown in Fig. 11, which is consistent with the post simulation results. The frequency detection characteristic is measured at a reference frequency of 2 MHz as shown in Fig. 12. It can be seen that the frequency acquisition range is 0.2 to 20 MHz. The measured

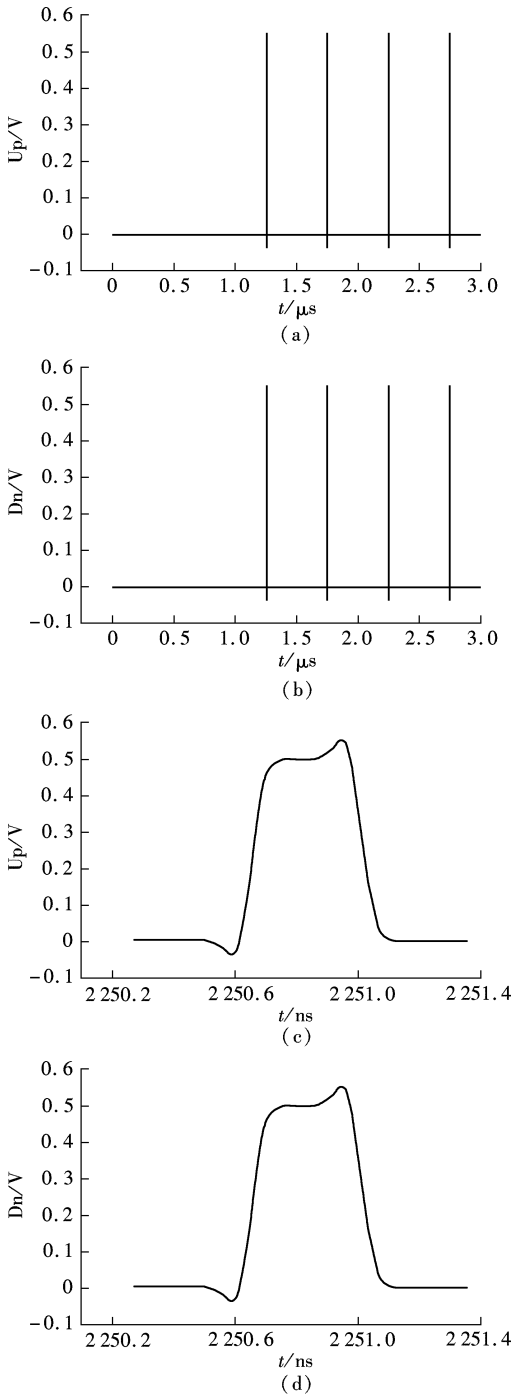

Fig. 8 Simulated output voltages with time at 2 MHz and zero phase difference. (a) Same narrow pulses for up signals; (b) Same narrow pulses for down signals; (c) Zoom-in of (a); (d) Zoom-in of (b)

current of the PFD core is 3. 5 μA when the input signals have frequencies of 2 MHz and zero phase errors.

4 Conclusion

A phase and frequency detector using low threshold transistors is designed, conducted and measured experimentally. The PFD has salient features with a low supply voltage of 0. 5 V and low power consumption. It has a faster acquisition speed and a larger lock-in range compared with the previous DPFDs, and the maximum operation frequency being double that of previous DPFDs. One problem in the PFD system is

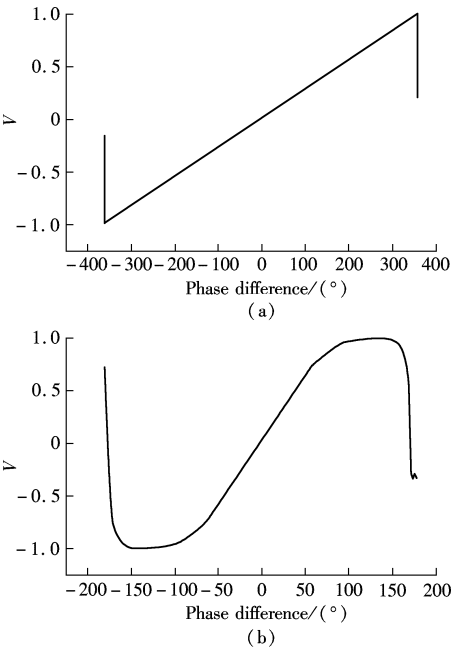

Fig. 9 Simulated phase detection characteristics. (a) At 2 MHz; (b) At 1. 25 GHz

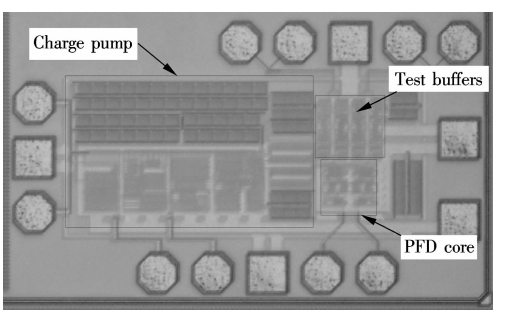

Fig. 10 Die photograph of the PFD chip fabricated by 0. 13 μm CMOS process

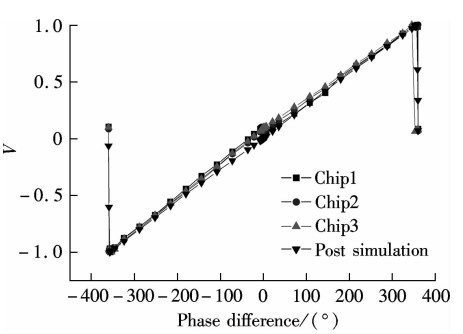

Fig. 11 Measured phase detection characteristics at 2 MHz

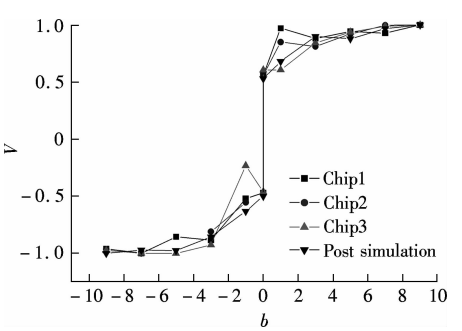

Fig. 12 Measured frequency detection characteristics at 2 MHz

that the narrow pulses of the output signal cannot be measured since the test buffer circuits cannot drive the oscilloscope at high frequencies higher than 2 GHz. Moreover, the phase noise of the circuit cannot be accurately measured because of the mismatch of the impedance between output of the test buffer circuits and the tested power spectrum analyzer. The issues will be explored in our research in the future. With the feature size of the CMOS process scaling into the nanometer range and the power supply voltage decreasing, the appropriate use of low threshold transistors in designing low voltage circuits becomes a favorable choice.

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应用于无线传感网频率合成器的0.5 V低电压鉴频鉴相器设计

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摘要:基于0.13 μm CMOS技术设计了一个应用于无线传感网频率合成器、电源电压为0.5 V的鉴频鉴相器.它的功能是比较输入信号的频率和相位差,并输出一个与该差值成比例的电压.因电源电压是0.5 V,所以该电路采用低阈值晶体管.为了增大相位误差的检测范围和提高最大工作频率,该电路采用了脉冲锁存的结构.当输入信号频率为2 MHz时,测得的相位误差检测范围为-358°~358°.与传统数字鉴频鉴相器相比,该电路具有较快的捕获速度.当输入信号的频率为2 MHz且相位误差为0°时,电路的功耗为1.8 μW,并且最大工作频率为1.25 GHz.

关键词:鉴频鉴相器;低阈值晶体管;脉冲锁存

中图分类号:TN929.5