Journal of Southeast University (English Edition) Vol. 27, No. 2, pp. 132 – 135 June 2011 ISSN 1003—7985

A monolithic InGaP/GaAs HBT power amplifier for W-CDMA applications

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Abstract: A monolithic microwave integrated circuit (MMIC) power amplifier (PA) is proposed. It adopts a new on-chip bias circuit, which not only avoids the instability of the direct current bias caused by the change in the power supply and temperature, but also compensates deviations caused by the increase in input power. The bias circuit is a current-mirror configuration, and the feedback circuit helps to maintain bias voltage at a constant level. The gain of the feedback circuit is improved by the addition of a non-inverting amplifier within the feedback circuit. A shunt capacitor at the base node of the active bias transistor enhances the linearity of the PA. The chip is fabricated in an InGaP/GaAs heterojunction bipolar transistor (HBT) process. Measured results exhibit a 26.6-dBm output compression point, 33.6% power-added efficiency (PAE) and – 40.2 dBc adjacent channel power ratio (ACPR) for wide-band code division multiple access (W-CDMA) applications.

Key words: power amplifier; wide-band code division multiple access (W-CDMA); heterojunction bipolar transistor (HBT); bias circuit; gain compression

doi: 10.3969/j.issn.1003 – 7985.2011.02.003

Wide-band code division multiple access (W-CDMA) is one of the most widely used standards of third-generation mobile communication and it employs a quadrature phase shift keying (QPSK)/hybrid phase shift keying (HPSK) modulation technique. Since QPSK and HPSK are linear modulation schemes, a stringent adjacent channel power ratio (ACPR) performance is required for the power amplifier (PA) in order to minimize the spectral regrowth and to maintain modulation accuracy.

An appropriate bias network is critical in achieving a high linear amplifier. For the design of the bias circuit of an HBT PA, there are two aspects that have to be considered: the stability of the DC bias and the adaptivity of the AC bias. Because the changes in the DC bias affect the operating point of the HBT, the DC bias has to be very stable and unaffected by the variations in the temperature and the power supply voltage. On the other hand, the significant change of the bias point owing to the input power tends to cause gain compression and phase distortion. The bias network provides adequate bias current to ensure linear or quasi-linear operation across the full range of operating power for the PA. A variety of on-chip linearization techniques have been proposed for improving PA performance[1–5].

This paper presents the design and measured performance of a monolithic linear PA for W-CDMA handset applications. A new on-chip bias circuit is demonstrated, which not only avoids the instability of the DC bias due to changes in the power supply and the temperature, but also compensates deviations caused by the increase in input power. The theory of gain expansion and gain compression is discussed. Then, the on-chip bias circuit and the whole PA circuit are presented. Finally, the measurement results of the PA are given.

1 Gain Expansion and Gain Compression

The amplifying function of an amplifier can be approximated with a polynomial:

$$V_{\text{out}} = \sum_n a_n V_{\text{in}}^n \tag{1}$$

where V_{out} is the output voltage, V_{in} is the input voltage, and a_n is a bias-dependent coefficient. If $V_{\text{in}} = A\cos \omega t$, the equations for the n-th degree output voltage can be written. In the third degree case, the output at a carrier frequency ω is

$$V_{\text{out}}|_{\omega} = \left(a_1 A + \frac{3}{4} a_3 A^3\right)\cos \omega t \tag{2}$$

where a_1A is the linear part of the PA and the other terms represent the gain deviation (i.e., expansion or compression). Gain expansion occurs for any value of A, and the signs for a_3/a_1 should be positive. Gain compression occurs for any value of A, and the signs for a_3/a_1 should be negative[6].

When a transistor PA exhibits gain expansion, the ratio of the output power to the input power increases with the increase in RF input signal power. This means that the proportionality between required bias current magnitude and input signal amplitude decreases with the increase in input signal amplitude. Gain compression represents a converse phenomenon in a transistor PA and exhibits falling or flat output power when the input signal power exceeds a certain level. Thus, beyond that level, the proportionality of the required bias current to the input signal amplitude increases. Both the gain compression and gain expansion are undesirable because of their tendency to produce a distortion in the output signal[7].

Fig. 1 shows simulated gain compression of the power amplifier. Without a compensation circuit, the amplifier tends to exhibit earlier gain compression. With a linearizing circuit, the amplifier has a constant ratio of input signal power to amplified output signal power (a flat signal gain response).

Received 2010-01-21.

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Foundation item: The National High Technology Research and Development Program of China (863 Program) (No. 2009AA01Z260).

Citation: Huang Jiwei, Wang Zhigong, Liao Yinghao, et al. A monolithic InGaP/GaAs HBT power amplifier for W-CDMA applications[J]. Journal of Southeast University (English Edition), 2011, 27(2): 132 – 135. [doi: 10.3969/j.issn.1003 – 7985.2011.02.003]

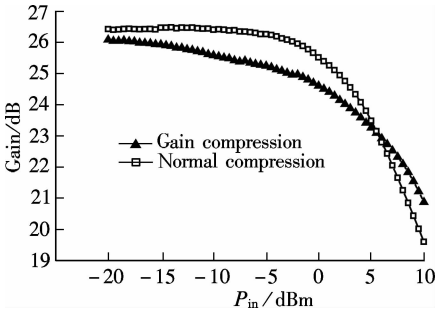

Fig. 1 Simulated gain compression of the PA

2 Bias Circuit Design

The new bias circuit proposed in this paper is shown in Fig. 2. Transistor HBT1 is the transistor that is to be biased. The bias circuit is composed of: 1) Transistor HBT2, which is matched to transistor HBT1 and is connected to transistor HBT1 in a current-mirror configuration; 2) Reference resistor R_1; 3) A non-inverting amplifier; 4) Transistor HBT3; 5) Base resistors R_2 and R_3, which control the amount of bias current supplied to transistors HBT1 and HBT2. Feedback through the non-inverting amplifier, HBT3 and R_2 stabilizes the reference current to compensate for fluctuations in reference voltage, in temperature, and in the transistor parameters, respectively.

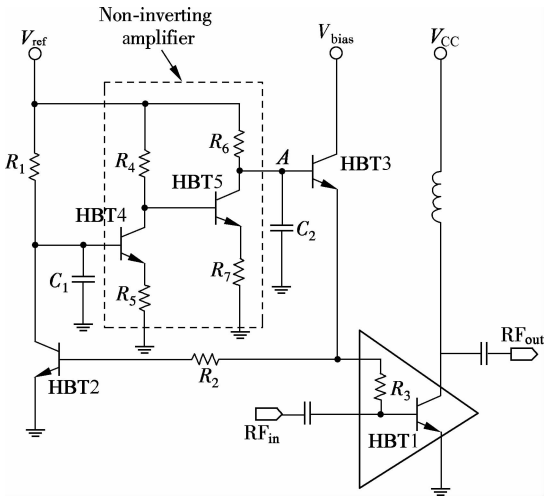

Fig. 2 Bias circuit

When reference voltage V_{ref} increases, both the voltage at the base of transistor HBT4 $V_{B,HBT4}$ and the current $I_{B,HBT4}$ increase correspondingly. The collector-emitter voltage of transistor HBT4 $V_{CE,HBT4}$ decreases, pulling down the voltage $V_{B,HBT5}$ and amplifying the fluctuation in voltage $V_{B,HBT5}$. The decreased voltage $V_{B,HBT5}$ causes the voltage $V_{CE,HBT5}$ to increase, thus pulling up the voltage $V_{B,HBT3}$. The voltage $V_{CE,HBT3}$ decreases correspondingly, thus pulling up the voltage $V_{E,HBT3}$. The current into the base of transistor HBT2 in turn increases, causing the voltage $V_{CE,HBT2}$ to decrease and thereby pulling down the voltage at its collector back to the desired quiescent value. A non-inverting amplifier within the feedback circuit improves the gain of the feedback circuit[8-9].

Fig. 3 shows the simulated V_{bias} and I_{bias} of HBT1 as a function of the reference voltage. With a non-inverting amplifier, the circuit exhibits less bias voltage variations compared with the case without a non-inverting amplifier. More-over, the gain in the feedback loop is selected sufficiently to compensate for variations in reference voltage even when the power supply voltage is as low as 2.6 V, just slightly higher than twice the base-emitter voltage of the HBT transistors in the circuit.

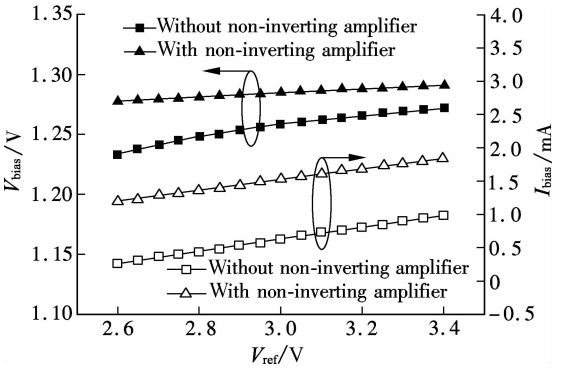

Fig. 3 Simulated V_{bias} and I_{bias} of HBT1 as a function of V_{ref}

The capacitor C_1 bypasses the power amplified by HBT2. The shunt capacitor C_2 with the base-emitter diode of the transistor HBT3 compensates for the decreased base bias voltage of HBT1 caused by the increased input power. Because the impedance of the parallel connection of other parts in the circuit is much higher than the impedance of capacitor C_2 at an RF frequency, all the RF signals at node A pass through the capacitor C_2, fixing the voltage at node A. With the increased input power, HBT1 needs more collector current, and the base-current of HBT1 must be increased. In this case, the voltage at A is fixed constantly, in a DC sense, because the collector current of HBT5 is much higher than the base current of HBT3. As a result, the entire voltage drop between the base and emitter of HBT3 compensates for the base bias drop of HBT1. Fig. 1 shows the simulated gain compression of the PA. Without the capacitor C_2, the compression point of the circuit comes earlier than the case with the capacitor[2].

3 PA Design

Fig. 4 shows the simplified schematic diagram of the power amplifier. It is a 2-stage design including inter-stage impedance matching circuits. The two stages are biased class AB to achieve the trade-off between high efficiency and good linearity. A negative on-chip RC-feedback is used in the driver stage to improve the amplifier stability and linearity as well as to increase the input resistance. The bias scheme outlined in Fig. 2 is replicated for each stage of the proposed PA. With consideration of the current collapse due to thermal effect, the selectivity of ballasting resistors is very important for PA design[10]. In this design, the base ballasting resistors are used in both the drive stage and the power stage to reduce the power loss of the ballasting resistors.

In addition to the design of active devices, the output matching network also determines the performance of the chip to a great extend. A low-pass LC network is selected to transfer the output load to be suitable to the PA for impro-

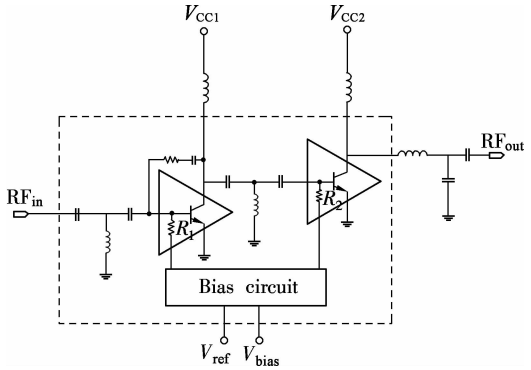

Fig. 4 Simplified block diagram of proposed PA

ving the linearity. With consideration of a high peak to an average power ratio of the modulation signal, a 31.5-dBm saturated power is designed for the 28-dBm output power, and 3 to 4 dBm power back-off is achieved. When the power voltage is 3.4 V and the designed output power is 31.5 dBm, the suitable impedance is 4 Ω for the second power stage.

4 Fabrication and Test Results

The MMIC power amplifier is fabricated in a commercial 2-μm InGaP/GaAs HBT process using multiple fingers of a unit transistor of 80 μm^2 (The emitter area is 4 800 μm^2 for the power stage and 640 μm^2 for the driver stage). The total die size of the PA is 1.1 mm × 1.1 mm. The realized PA chip is directly mounted on the measurement PCB by wire bonding. The fabricated MMIC PA and the tested board are shown in Fig. 5 and Fig. 6, respectively.

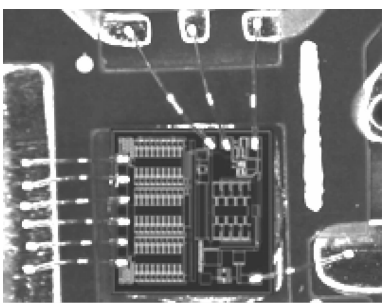

Fig. 5 Die photograph of the MMIC PA

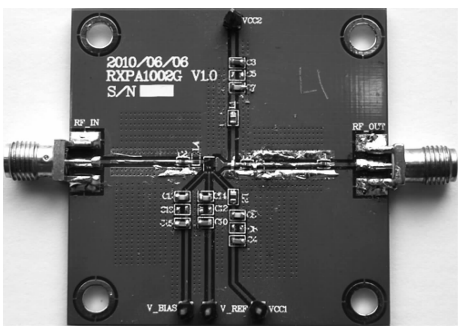

Fig. 6 PCB board for power measurement of PA

For measurement, the 3GPP uplink W-CDMA signal is used at an operating frequency of 1 950 MHz. The voltage supplies V_{ref}, V_{bias}, V_{CC1} and V_{CC2} are 3.0, 3.4, 3.4, and 3.4 V, respectively. Fig. 7 shows the single-tone performance in terms of output power, gain and PAE. The amplifier exhibits a 26.6-dBm output compression point, a 26.4-dB gain and a 29.1-dBm saturated output power along with 40.3% PAE.

ACPR measurement is achieved using a 3.84×10^6 chip/s W-CDMA modulated signal in a 5 MHz offset frequency band(see Fig. 8). The measured ACPR is −40.2 dBc at the output power of 26.6 dBm for W-CDMA applications.

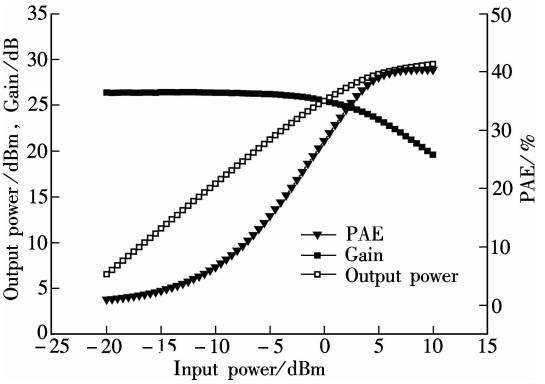

Fig. 7 Power measurement results of the PA at 1.95 GHz

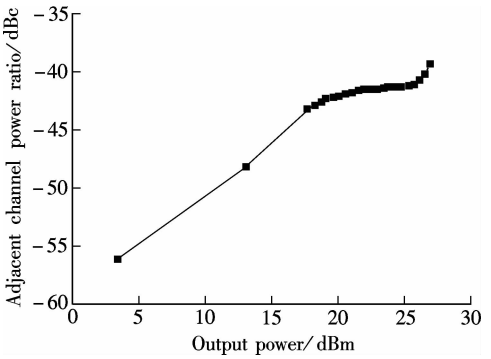

Fig. 8 Measured ACPR of the PA at 1.95 GHz

5 Conclusion

A new on-chip bias circuit composed of a current-mirror bias configuration including a feedback circuit and a linearizing capacitor is described, which not only avoids the instability of DC bias due to the change in power supply, but also compensates deviations caused by the increase of input power. Measurement results exhibit an output compression point of 26.6 dBm, PAE of 33.6%, and an ACPR of −40.2 dBc for W-CDMA applications.

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一种应用于 W-CDMA 的单片 InGaP/GaAs HBT 功率放大器

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摘要:设计了一款微波单片集成电路功率放大器. 该放大器采用了一种新颖的在片偏置电路技术,不仅避免了由于电源和温度变化导致的直流偏置点的不稳定,而且补偿了由于输入信号增大所引起的交流偏置点的偏离. 电流镜结构的偏置电路与反馈电路使偏置电压维持在一个稳定的状态,在反馈电路中引入一个非反相电路提高了电路增益. 通过在偏置管的基极并联一个电容进一步改善了功率放大器的线性. 该芯片采用 InGaP/GaAs HBT 工艺制作. 测试结果表明:该放大器具有 26.6 dBm 的输出压缩点,对于 W-CDMA 应用,放大器的效率为 33.6%,ACPR 为 –40.2 dBc.

关键词:功率放大器;宽带码分多址;异质结双极型晶体管;偏置电路;增益压缩
中图分类号:TN431