Journal of Southeast University (English Edition) Vol. 27, No. 2, pp. 136 – 139 June 2011 ISSN 1003—7985

A 5-Gbit/s monolithically-integrated low-power clock recovery circuit in 0.18-μm CMOS

Zhang Changchun[1] Wang Zhigong[1] Shi Si[1] Pan Haixian[2] Guo Yufeng[1] Huang Jiwei[1]

([1]Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

([2]State Key Laboratory of Bioelectronics, Southeast University, Nanjing 210096, China)

Abstract: In order to make a 10 Gbit/s 2∶1 half-rate multiplexer operate without external clocks, a 5 Gbit/s clock recovery (CR) circuit is needed to extract the desired clock from one input data. For the CR circuit, a 3-stage ring voltage-controlled oscillator (VCO) is employed to avoid an unreliable startup of a 2-stage VCO and a low oscillation frequency of a 4-stage VCO. A phase frequency detector (PFD) is used to expand the pull-in range to meet the wide tuning range of a VCO required by process-voltage-temperature (PVT) variation. SMIC 0.18-μm CMOS technology is adopted and the core area is 170 μm × 270 μm. Measurements show that, under a 1.8 V supply voltage, it consumes only about 90 mW, and has an input sensitivity of less than 25 mV, an output single-ended swing of above 300 mV, a phase noise of −114 dBc/Hz at 1 MHz offset and a pull-in range of 1 GHz.

Key words: clock recovery; phase frequency detector; voltage-controlled oscillator; phase noise

doi: 10.3969/j.issn.1003 – 7985.2011.02.004

With the development demands of high-volume data transmission, both high-speed long-haul serial optical communications and short-haul parallel optical interconnections have received more and more attention. In both kinds of communication systems, the clock recovery (CR) is a critical function. Owing to the diversity of application environments and demands, and the rapid development of the IC fabrication process, mainly, CMOS, the advancement of design techniques, various kinds of CR have been emerging. Unlike filter-type CR techniques[1], PLL-based CR techniques[2-6] possess many advantages, such as high integration and perfect clock-data alignment.

In this paper, a 5 Gbit/s monolithic PLL-based CR which is designed and fabricated in SMIC 0.18-μm CMOS technology is described. The 5 Gbit/s CR is used to extract a clock for a 10 Gbit/s multiplexer. The circuit design details and the measurement results are given, respectively.

1 Circuit-Level Design

Basically, the core of the CR circuit comprises a phase detector (PD), a voltage to current conversion (V/I) circuit, a loop filter (LF), and a VCO.

Owing to the unreliable and narrow pull-in range of a PLL without a frequency detector (FD), shown in Fig. 1, a frequency and phase detector (PFD) is employed, which can avoid some contradictions between loop bandwidth and pull-in range, and make the loop have a small loop bandwidth, a wide pull-in range, and operate without requiring a local reference clock and off-chip tuning.

In contrast to a CR with a PD, the required clock phase number is usually doubled for a CR with a PFD; that is, two differential clock pairs are required. Although I/Q clocks ($\pi/2$ phase separation) are an optimum choice for the operation of the PFD, I/Q clocks usually require a ring VCO of even-numbered stages. For a 0.18-μm CMOS process, if a 4-stage ring VCO is used, it is difficult to oscillate at a frequency of 5 GHz; if a 2-stage ring VCO is used, there exists a big risk that the VCO cannot oscillate because it is not easy to meet the Barkhausen criterion. Fortunately, the Pottbäcker PFD has a superior performance, which can tolerate up to a ±45° I/Q phase error[7]; so a 3-stage ring VCO can be used instead.

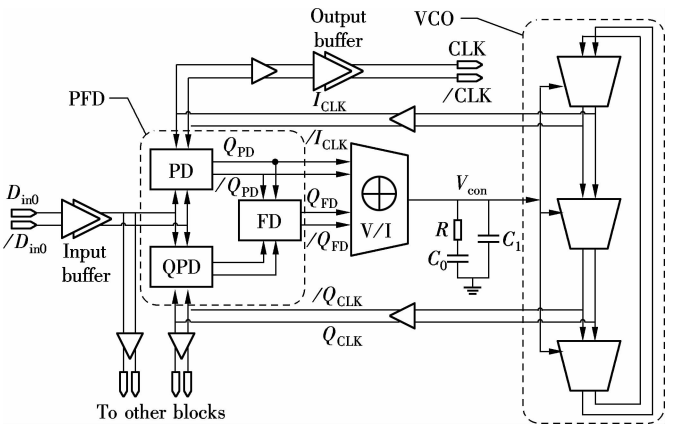


Fig. 1 Circuit block diagram of the adopted CR

First, by data sampling clocks, the input data are compared with two differential clocks and two beat notes are produced. The two beat wotes are processed by the FD to deliver a frequency error signal. Secondly, by the V/I converter and the LF, the generated frequency error signal, combined with the phase error output from the PD, drives the VCO frequency towards the data rate of the input data, relinquishing the control over the CR loop to the PD when the frequency error is sufficiently small.

1.1 Phase/frequency detector

In contrast to their linear counterparts, bang-bang PDs have many advantages, such as inherent sampling phase alignment, adaptability to multi-phase sampling structures,

Received 2010-11-22.

Biographies: Zhang Changchun (1981—), male, doctor; Wang Zhigong (corresponding author), male, doctor, professor, zgwang@seu.edu.cn.

Foundation items: The National High Technology Research and Development Program of China (863 Program) (No. 2007AA01Z2a5), the National Natural Science Foundation of China (No. 60806027, 61076073), Specialized Research Fund for the Doctoral Program of Higher Education (No. 20090092120012).

Citation: Zhang Changchun, Wang Zhigong, Shi Si, et al. A 5-Gbit/s monolithically-integrated low-power clock recovery circuit in 0.18-μm CMOS[J]. Journal of Southeast University (English Edition), 2011, 27(2): 136 – 139. [doi: 10.3969/j.issn.1003 – 7985.2011.02.004]

and operating at higher speeds, etc. Thus, a bang-bang PD is employed. According to the sampling relationship between clock and data, bang-bang PDs can be classified into two types: One produces phase error by clock sampling data, for example, Alexander PD; the other operates by data sampling clock, for example, the Pottbäcker PD. The latter usually has a simpler architecture, so it is adopted.

The Pottbäcker PFD is composed of PD, QPD and FD. As shown in Fig. 2(a), the PD, identical with the QPD, is a double-edge-triggered flip-flop (DETFF), which consists of two CML latches and a selector. The DETFF is chosen over a conventional single-edge-triggered DFF, because it can make use of both edges of the input data to offer more phase error correction information and then improve the performance of the loop. The only difference of the FD from the PD is the used selector, shown in Fig. 2(b), which is a modified version of the conventional one used in the PD and can produce a ternary output.

When the frequency acquisition is completed, the FD remains on a third state, that is, both the outputs from it remain high. By this means, the control of the FD over the loop is handed over to the PD, and then the track stage starts to work.

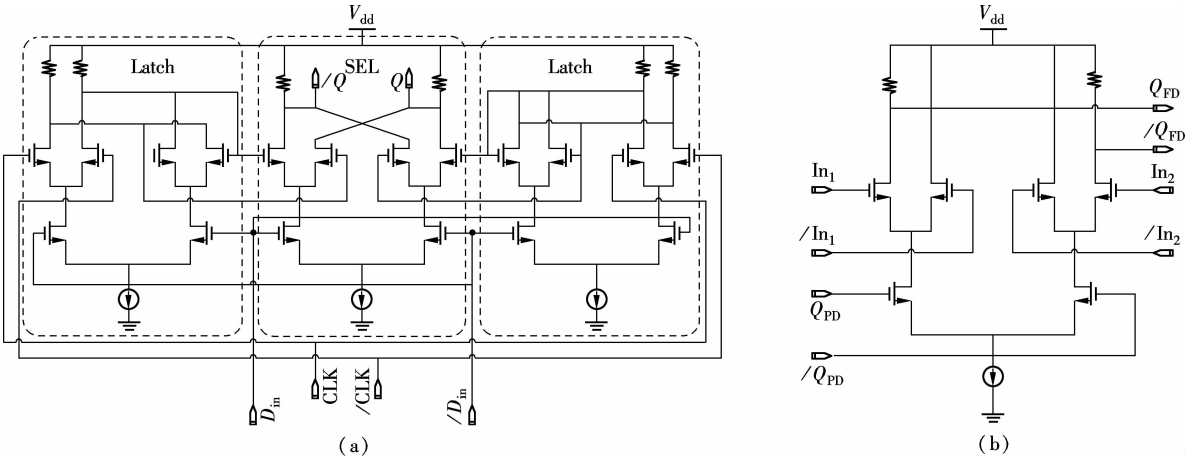


Fig. 2 Circuit diagram. (a) PD; (b) Tri-state selector

1.2 VCO

As shown in Fig. 3, a three-stage inductorless ring VCO is employed to generate the desired clocks. Due to the wide loop bandwidth of the bang-bang CR, the inferior phase noise performance inherent in the ring VCO can be tolerated. Furthermore, its inherent wide tuning bandwidth is desired by the bang-bang CR [8-9].

The VCO cell can be found in Fig. 3, in which a current-folding technique is used to alleviate the conflict between the voltage headroom and the sensitivity of the VCO[10]. The frequency of the VCO is tuned by changing the relative strength between the currents flowing through the differential pair (M_1 and M_2) and the cross-coupled transistor pair (M_3 and M_4). Two current sources (I_1 and I_2) are added to prohibit ceasing of the oscillation and improve the linearity of the VCO characteristics, respectively. Due to the differential tuning from terminals V_{c1} and V_{c2}, the total current through loads (M_7 and M_8) remains almost constant, and then the output voltage swing suffers from less variation across the tuning range, which can improve the phase noise performance of the VCO.

Compared with the pseudo-differential delay cell, the delay cell consisting of a true-differential pair and a cross-

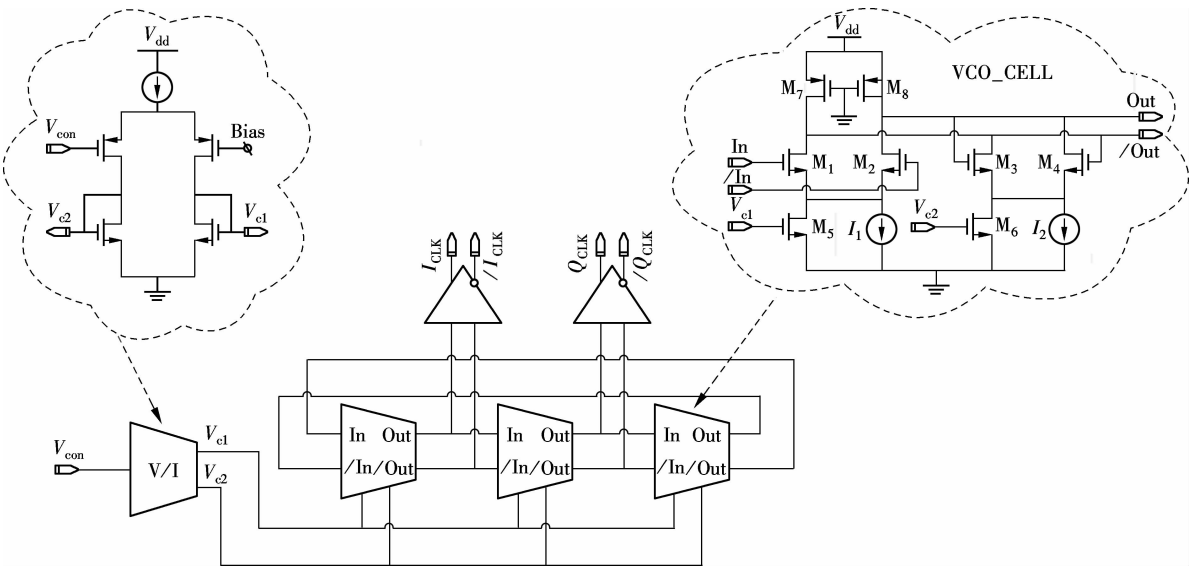


Fig. 3 Circuit diagrams of the VCO and its cell

coupled pair is easy to oscillate and has a better differential operation. The differential topology has another advantage over a single-ended one, that is, a better duty cycle, which has a critical effect on the performance of the CR.

1.3 V/I converter and loop filter

Fig. 4 shows the circuit schematic of the V/I converter and the loop filter. Actually, the V/I converter is an adder with a single-ended high-impedance output, where both phase error signal and frequency error signal from the PD and the FD are applied to two input ports, respectively, and an output signal is generated to tune the VCO by the loop filter. The V/I converter with the loop filter produces an ideal integrator to the loop. The integrator with another integrator from the VCO makes the CR loop become a type Ⅱ PLL. The type Ⅱ PLL has many advantages over a type Ⅰ loop, such as low static phase error between data and clock. As for the type II CR, the loop filter can be entirely passive, consisting only of resistors and capacitors.

In order to reduce the channel-length modulation effects of M_8 and M_{10}, the channel lengths and widths of the transistors are increased.

Due to the low capacitance density(less than 1 fF/μm^2) of the MIM capacitor, NMOS transistors (about 8 fF/μm^2) are used as a capacitor, especially for the large capacitor C (see Fig. 4).

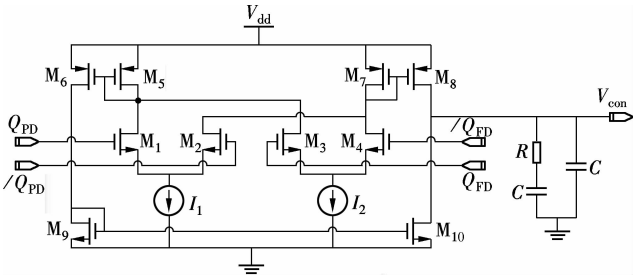


Fig. 4 Circuit diagram of V/I converter and loop filter

2 Experimental Results

The chip is designed and fabricated in SMIC 0.18-μm CMOS technology. As shown in Fig. 5, the whole IC occupies an area of 670 $\mu m \times 760$ μm with a CR core area of 170 $\mu m \times 270$ μm.

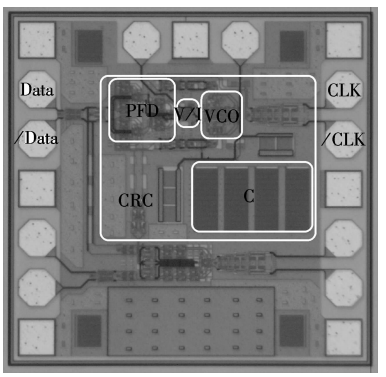


Fig. 5 Chip photograph of the whole IC

The performance of the CR was evaluated on-wafer by a Cascade probe station. Mainly, an Advantest D3186 pulse pattern generator, an Agilent 86100A Infinium DCA wide-bandwidth oscilloscope, and an E4440a digital spectrum analyzer were employed.

Fig. 6 depicts the measured VCO tuning characteristic curve. The VCO achieves a tuning range of above 1 GHz (>20%).

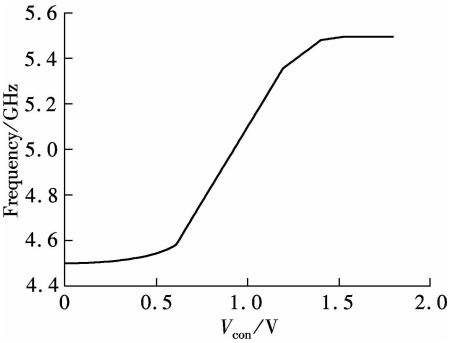
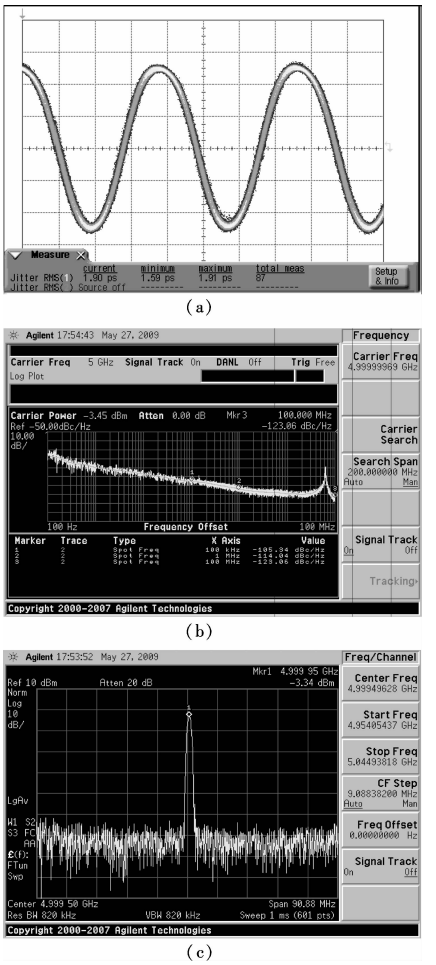


Fig. 6 Measured VCO tuning characteristic curve

Fig. 7 shows the measured waveform, phase noise, and spectrum of the 5-GHz recovered clock with an input of a 5 Gbit/s pseudorandom bit sequence (PRBS) of length $2^{31}-1$ from a 1.8 V supply. From Fig. 7, it can be found that the recovered clock has a phase noise of −114 dBc/Hz at 1 MHz offset (−105 dBc/Hz at 100 kHz offset), an rms jitter of 1.9 ps, and an output single-ended swing of above 300 mV.

The measurement results show that under a 1.8 V sup-



(a)

(b)

(c)

Fig. 7 Measured results of the 5 GHz recovered clock. (a) Waveform; (b) Phase noise; (c) Spectrum

ply, the pull-in range of the CR is actually limited by the available operating range of the VCO, that is, approximately between 4.5 and 5.5 GHz. In other words, the CR can work properly with any input data rate between 4.5 and 5.5 Gbit/s. And, the CR IC consumes about 90 mW with an input sensitivity of less than 25 mV.

A comparison with the results from previously published similar studies is listed in Tab. 1. According to Tab. 1, it can be found that the proposed CR has a better performance.

Tab. 1 Performance comparison of previously published full-rate CMOS CRs

Parameter	This paper	Ref. [4]	Ref. [5]	Ref. [1]	Ref. [6]
Process	0.18-μm CMOS	0.18-μm CMOS	0.25-μm CMOS	0.25-μm CMOS	0.18-μm CMOS
Speed/(Gbit·s^{-1})	5	2.5	2.5	2.5	2.5
Off-chip capacitor	No	Yes	Yes	Yes	No
Off-chip tuning	No	No	Yes	Yes	
Reference clock	No	No	No	No	No
P_{diss}/mW	90	26.1	550	680	120
Area/μm^2	670×760	2 400×2 400	970×970	1 490×1 000	675×875
Pull-in range/MHz	1 000	220	80	40	250
Phase noise	−114 dBc/Hz @1 MHz	−100 dBc/Hz @1 MHz	−106 dBc/Hz @100 kHz	−110 dBc/Hz @100 kHz	−111 dBc/Hz @10 kHz

3 Conclusion

A 5 Gbit/s monolithic PLL-based bang-bang CR is designed and fabricated in SMIC 0.18-μm CMOS technology. The circuit designs are shown in detail, and the measurement results are given. The CR core has an active area of 170 μm ×270 μm, and consumes about 90 mW under a 1.8 V supply voltage, with an input sensitivity of less than 25 mV, and an output single-ended swing of above 300 mV.

The CR works reliably at any input data rate between 4.5 and 5.5 Gbit/s without any need for reference clock, off-chip tuning, or external components. It has a phase noise of −114 dBc/Hz at 1 MHz offset at 5 Gbit/s data input.

References

[1] Wang Huan, Wang Zhigong, Feng Jun, et al. 2.488 Gbit/s clock and data recovery circuit in 0.35 μm CMOS [J]. *Journal of Southeast University*: *English Edition*, 2006, **22** (2): 143−147.

[2] Gutierrez G, Shyang K. Unaided 2.5 Gb/s silicon bipolar clock and data recovery IC [C]//*IEEE Radio Frequency Integrated Circuits Symposium*. Piscataway, NJ, USA: IEEE, 1998: 173−176.

[3] Gutierrez G, Shyang K, Bruce C. 2.488 Gb/s silicon bipolar clock and data recovery IC for SONET (OC-48) [C]// *IEEE Custom Integrated Circuits Conference*. Piscataway, NJ, USA: IEEE, 1998: 575−578.

[4] Raja M K, Yan D L, Ajjikuttira A B, et al. A 1.4-psec Jitter 2.5-Gb/s CDR with wide acquisition range in 0.18-μm CMOS [C]//*European Solid-State Circuits Conference*. Piscataway, NJ, USA: IEEE, 2007: 524−527.

[5] Chen Yingmei, Wang Zhigong, Xiong Mingzhen, et al. 2.5 Gb/s monolithic IC of clock recovery, data decision, and 1∶4 demultiplexer [J]. *Chinese Journal of Semiconductors*, 2005, **26** (8): 1532−1536.

[6] Liu Yongwang, Wang Zhigong, Li Wei. 2.5 Gb/s 0.18 μm CMOS clock and data recovery circuit [J]. *Chinese Journal of Semiconductors*, 2007, **28** (4): 537−541.

[7] Pottbäcker A, Langmann U, Schreiber H U. A Si bipolar phase and frequency detector IC for clock extraction up to 8 Gb/s [J]. *IEEE Journal of Solid-State Circuits*, 1992, **27** (12): 1747−1751.

[8] Rogers J E, Long J R. A 10 Gb/s CDR/DEMUX with LC delay line VCO in 0.18 μm CMOS [J]. *IEEE Journal of Solid-State Circuits*, 2002, **37** (12): 1781−1789.

[9] Walker R C. Designing bang-bang PLLs for clock and data recovery in serial data transmission systems [C]//*Phase-Locking in High Performance Systems*: *From Devices to Architectures*. Wiley-IEEE Press, 2003: 34−45.

[10] Razavi B. *Design of integrated circuits for optical communications* [M]. New York: McGraw-Hill, 2003: 197−200.

5-Gbit/s 0.18-μm CMOS 单片集成低功耗时钟恢复电路设计

张长春[1] 王志功[1] 施 思[1] 潘海仙[2] 郭宇峰[1] 黄继伟[1]

([1] 东南大学射频与光电集成电路研究所, 南京 210096)

([2] 东南大学生物电子学国家重点实验室, 南京 210096)

摘要:为了使一个 10 Gbit/s 2∶1半速率复接器电路能够在无外部提供时钟的环境中工作,需要一个 5 Gbit/s 时钟恢复电路从一路输入数据中提取出所需时钟.该时钟恢复电路采用 3 级环形压控振荡器,以克服 2 级振荡器存在的起振不可靠和 4 级振荡器振荡频率低的问题;采用鉴频鉴相器来增加牵引范围,以适应由于工艺、电压及温度偏差等原因而导致的压控振荡器的宽调谐范围; 采用 SMIC 0.18-μm CMOS 工艺,核心电路面积为 170 μm×270 μm.测试表明:在 1.8 V 电压下,该电路功耗大约为 90 mW,输入灵敏度低于 25 mV,输出摆幅大于 300 mV,且具有 −114 dBc/Hz@1 MHz 的相位噪声和 1 GHz 牵引范围.

关键词:时钟恢复;鉴频鉴相器;压控振荡器;相位噪声

中图分类号:N913.7