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Modified Benes network architecture for WiMAX LDPC decoder

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Abstract: A modified Benes network is proposed to be used as an optimal shuffle network in worldwide interoperability for microwave access (WiMAX) low density parity check (LDPC) decoders. When the size of the input is not a power of two, the modified Benes network can achieve the most optimal performance. This modified Benes network is non-blocking and can perform any sorts of permutations, so it can support 19 modes specified in the WiMAX system. Furthermore, an efficient algorithm to generate the control signals for all the 2×2 switches in this network is derived, which can reduce the hardware complexity and overall latency of the modified Benes network. Synthesis results show that the proposed control signal generator can save 25.4% chip area and the overall network latency can be reduced by 36.2%.

Key words: worldwide interoperability for microwave access (WiMAX); quasi-cycle low density parity check (QC-LDPC); LDPC decoder; Benes network

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Low-density parity-check codes were first proposed by Gallager[1] in 1962. After the discovery of the turbo code, Mackay et al.[2] reinvestigated LDPC codes and found that they can achieve a good bit error rate (BER) performance approaching the Shannon limit. Therefore, LDPC codes have become widely used in the communication systems with high data transmission rates. QC-LDPC is a kind of structured LDPC code. It is suitable to be implemented in hardware and its performance is close to the randomly generated LDPC code. In the WiMAX system, QC-LDPC codes include 19 code rates and code lengths. Therefore, in order to fulfill the flexibility in the LDPC decoder architecture, it is important to design a programmable shuffle network between the variable node processor units (VNU) and the check node processor units (CNU).

The Benes network[3] is one of the best-known rearrangeable networks that can perform any sorts of permutations over N data units, where N stands for the number of network inputs or outputs and is optimized to be a power of two. So the Benes network is introduced into designing flexible QC-LDPC decoders as a switch network and it is optimal when the size of the permutation matrix is a power of two.

However, it is not trivial to generate the control signals for all the 2×2 switches in the Benes network. In Refs. [4 – 5], the control signals are stored in a dedicated lookup table (LUT) directly. But when the size of the Benes network becomes large, the intense requirement of LUT storage makes it inefficient and impractical to implement. In order to reduce the LUT storage requirement, Sun et al.[6] introduced a reconfigurable shuffle network based on the use of two Benes networks: one switches the data and the other configures the first one on-the-fly. Although this network can achieve significant savings on area and routing complexity compared with the direct implementation of N-to-1 multiplexers proposed in Refs. [3 – 4], it still suffers from large hardware complexity. In Refs. [7 – 8], two novel algorithms were proposed to more efficiently generate the control signals for the Benes network and reduce the hardware complexity. However, in Ref. [7] the proposed network is not optimal when the input size is not a power of two. And in Ref. [8] there are some redundancies in the control signal generating algorithms and that increases the overall latency of the shuffle network.

In this paper, we propose a novel efficient shuffle network for the reconfigurable WiMAX LDPC decoder which can support 19 modes specified in the system. Compared with the traditional Benes network, the proposed network has lower hardware complexity when the input size of the network is not a power of two. In addition, based on the fact that in the QC-LDPC decoder the outputs of the shuffle network can only be the cyclic shifts of the inputs, we introduce a novel efficient algorithm to generate the control signals for all the switches in the network, which can reduce the overall latency proposed in Ref. [8].

1 Modified Benes Network

As shown in Fig. 1, the Benes network can be constructed in a recursive way. The N-input Benes network can be derived from two $N/2$-input Benes networks and two additional stages where each stage consists of $N/2$ 2×2 switches (each switch can be set either in the bar state or the cross state). Totally, the network consists of $2\log_2 N - 1$ stages.

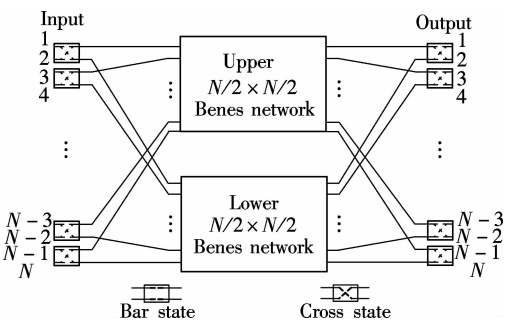

Fig. 1 Benes network structure

The $N \times N$ Benes network is an optimal switch network when the input size N is a power of two, which means that the $N \times N$ Benes network can be used as the shuffle network

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in the LDPC decoder when the input size is equal to or less than N. However, in the WiMAX system, the largest size of the sub matrix is 96 which is not a power of two. Therefore, a 128×128 Benes network should be used in the WiMAX LDPC decoder, which will cause low hardware utilization efficiency. And totally 832 2×2 switches should be used to implement this 128×128 Benes network.

In this paper, we modify the Benes network and propose an efficient shuffle network (with 96 inputs or outputs) to support all the required 19 modes in the reconfigurable WiMAX LDPC decoder. As shown in Fig. 2, the proposed network is constructed in a recursive way similar to the traditional Benes network until the input size becomes 3. Here we design a 3×3 switch (marked in Fig. 2) which is built from three 2×2 switches and this non-blocking switch can perform any required permutation. There are a total of thirty-two 3×3 switches to connect the left half and the right half of the shuffle network, and each half includes five columns (with 48 switches in each column). And this network can be implemented with 576 2×2 switches and can save 30.8% hardware compared with the traditional Benes network.

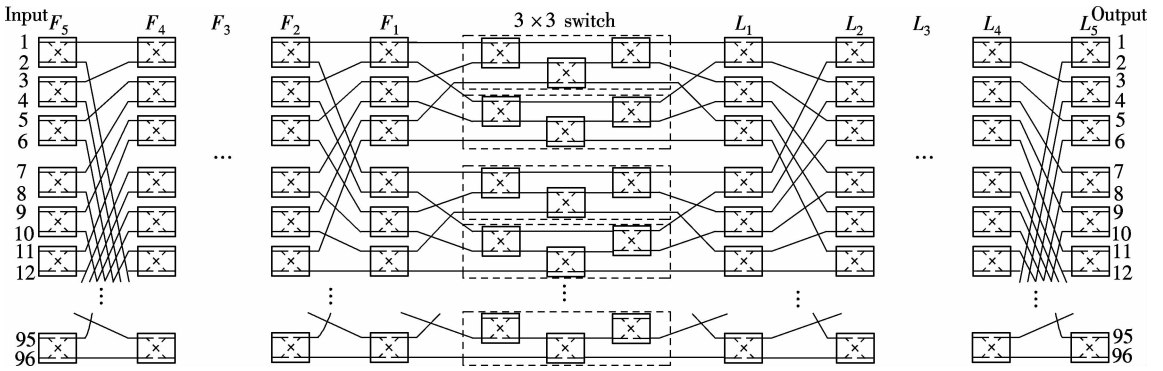

Fig. 2 Modified Benes network structure

2 Efficient Algorithm for Control Signal Design of Modified Benes Network

In the QC-LDPC parity-check matrix, the sub matrices are constructed from identity matrices by cyclic shifts. Therefore, it is only necessary to achieve cyclic shift permutations for sub matrices in the QC-LDPC decoder. To better demonstrate the control signal design of our modified Benes shuffle network, three parameters and two functions are defined as follows:

p stands for the size of sub matrices in the WiMAX system. It is also called an expansion factor in Tab. 1 and varies from 24 to 96 with increments of 4.

c stands for the required cyclic shifting number of the sub matrix.

P_m stands for the maximum input size of the shuffle network. It is set to be 96 initially.

Function Floor (A) rounds A to the nearest integer less than or equal to A.

Function Ceil (A) rounds A to the nearest integer greater than or equal to A.

Tab. 1 WiMAX QC-LDPC codes

System	Code rate	Expansion factor	Code length
WiMAX	1/2, 2/3, 3/4, 5/6	$24+4n$ $n=(0,1,\ldots,18)$	$576+96n$ $n=(0,1,\ldots,18)$

These three parameters are all positive integers and constrained by $c \leqslant p \leqslant P_m$. And parameters (p, c, P_m) mean cyclic shifting of p messages by c in the P_m-input shuffle network. The control signals of the shuffle network are generated from the above three parameters recursively. The proposed control signal generating algorithms are shown as follows.

Algorithm 1

With a given (p, c, P_m),

If $(P_m == 3)$, call Algorithm 2

Else, call Algorithm 3

Return

Algorithm 2

Check the least significant bits of p and c, and compute Ceil$(p/2)$ and Ceil$((p-c)/2)$.

Set all the 2×2 switches in the Benes network to the bar state in default.

Set 2×2 switches in the first and last stages of P_m-input switch network as follows:

If ($p ==$ even and $c ==$ even),

Call Algorithm 1 $(p/2, c/2, P_m/2)$ and Algorithm 1 $(p/2, c/2, P_m/2)$.

If ($p ==$ even and $c ==$ odd),

Set the top-most Ceil$(p/2)$ switches in the first stage to the cross state.

Call Algorithm 1 $(p/2,$ Ceil$(c/2), P_m/2)$ and Algorithm 1 $(p/2,$ Floor$(c/2), P_m/2)$.

If ($p ==$ odd and $c ==$ even),

Set all the switches between the Ceil$((p-c)/2)$-th switch and the Ceil$(p/2)$-th switch, (including Ceil$((p-c)/2)$-th and Ceil$(p/2)$-th switches) in the first stage to the cross state.

Set the Ceil$(p/2)$-th switch in the last stage to the cross state.

Call Algorithm 1 (Floor $(p/2)$, $c/2$, $P_m/2$) and Algorithm 1 (Ceil$(p/2)$, $c/2$, $P_m/2$).

If ($p ==$ odd and $c ==$ odd),

Set the top-most Ceil$((p-c)/2) - 1$ switches in the first stage to the cross state.

Call Algorithm 1 (Ceil$(p/2)$, Ceil$(c/2)$, $P_m/2$) and Algorithm 1 (Floor$(p/2)$, Floor$(c/2)$, $P_m/2$).

Return

Algorithm 3

Set 3×3 switches with properly configured signals for a given cyclic shift as follows:

For $(2, 1, 3)$, set switch 1 to the cross state.

For $(3, 1, 3)$, set switch 2 and switch 3 to the cross state.

For $(3, 2, 3)$, set switch 1 and switch 3 to the cross state.

For others, set all the switches to the bar state.

Return

The algorithm produces the control signals for the first and last stages according to parameters $(p,\ c,\ P_m)$ and also produces the following two parameters $(p_1,\ c_1,\ P_m/2)$ and $(p_2,\ c_2,\ P_m/2)$. And these two parameters are used to generate the control signals for the first and last stages of their two sub shuffle networks.

Compared with the algorithm in Ref. [8], our algorithm needs to set fewer switches to the cross state (all the switches are set to the bar state initially) as shown in Tab. 2. And this means that fewer logic gates are required to generate the control signals of the shuffle network, which can reduce the hardware implementation complexity and lower the overall latency of the shuffle network.

Tab. 2 Number of switches considered in Ref. [8] and the proposed algorithm

$(p,\ c,\ P_m)$	Algorithm in Ref. [8]	Proposed algorithm	Difference
p = = even c = = even	0	0	0
p = = even c = = odd	Floor$(p/2)$	Ceil$(p/2)$	0
p = = odd c = = even	P_m-Floor$((2p - c)/2)$	Ceil$(c/2) + 1$	$P_m - p$
p = = odd c = = odd	P_m-Floor$((p - c)/2)$	Ceil$((p - c)/2)$	$P_m - p + c$

One example $(p,\ c,\ P_m) = (21,\ 13,\ 24)$ is listed in Fig. 3 to demonstrate the proposed algorithm (all the notations are similar to Ref. [8] and all the switches are set to the bar state in default).

F_3 setting	$(p,\ c,\ P_m) = (21,\ 13,\ 24)$							
L_3 setting	$F_{3,1} = F_{3,2} = F_{3,3} = F_{3,4} = 1$							
F_2 setting	$(11,\ 7,\ 12)$				$(10,\ 6,\ 12)$			
L_2 Setting	$F_{2,1} = F_{2,2} = 1$				None			
F_1 setting	$(6,\ 4,\ 6)$		$(5,\ 3,\ 6)$		$(5,\ 3,\ 6)$		$(5,\ 3,\ 6)$	
L_1 Setting	None		$F_{1,1} = 1$		$F_{1,1} = 1$		$F_{1,1} = 1$	
3×3 switch	(3,2,3)	(3,2,3)	(2,1,3)	(3,2,3)	(2,1,3)	(3,2,3)	(2,1,3)	(3,2,3)

Fig. 3 Control signal generation for $(21,\ 13,\ 24)$

3 Hardware Implementation for Modified Benes Network

The control signal generator can be implemented with a look-up table (LUT) as proposed in Refs. [4 −5]. The configuration information for each 2×2 switch is computed according to the parameters $(p,\ c,\ P_m)$ and stored in the LUT. Then during the operation, switches are set to either the bar state or the cross state accordingly. For our modified 96×96 Benes network, the overall control signals can be implemented with 9 072 bit[8]. Although this number has decreased dramatically compared with traditional Benes networks, it can still consume a large silicon area.

In this paper, we use combinational logic to construct the control signal generator according to the input parameters $(p,\ c,\ P_m)$.

For all the switches in the shuffle network, the control signals are determined by p and c. Different groups of switch control signals are assigned to "1", which means that the corresponding switches are set to the cross state, depending on the least significant bits of p and c as stated in the algorithm (four possible combinations totally). For example, when $p_0 = 1$ and $c_0 = 0$, the control signals of switches from No. Ceil$((p - c)/2)$ to No. Ceil$(p/2)$ in the first stage are assigned to "1". The control signal generator is implemented with two levels. In the first level, one $\log_2(P_m/2)$-to-$(P_m/2)$ decoder is used to generate a control signal output which will set those switches to the cross state, and those switches can be set to the cross state in any of the four possible combinations of p_0 and c_0. It means that in the first stage, the least Ceil$(p/2)$ significant bits of the control signal output will be "1" while in the last stage, the Ceil$(p/2)$-th bit of the control signal output will be "1". In the second level, the output of the first level will be modified by p_0 and c_0 according to the algorithm.

The control signal generator structure is shown in Fig. 4. The decoder is similar to that in Ref. [8]. The combinational logic in the second level is much simpler than that in Ref.

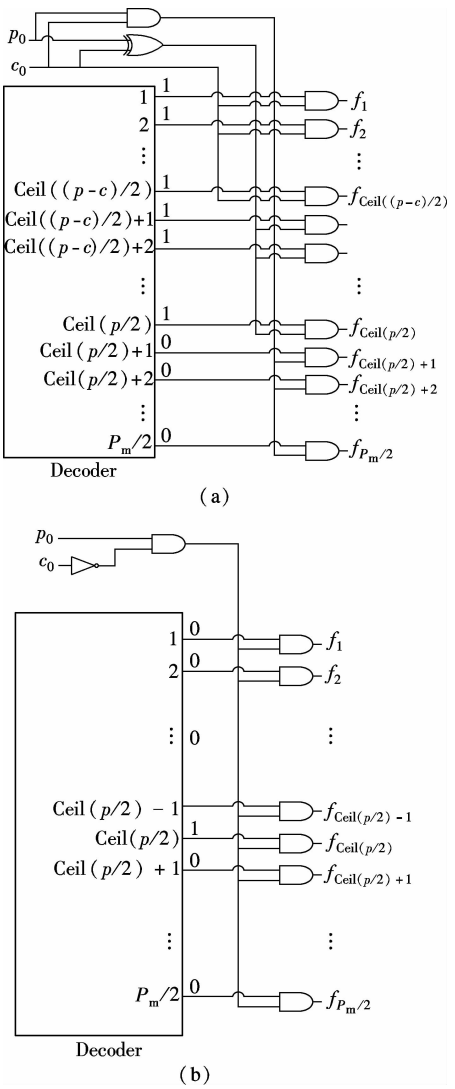

Fig. 4 Control signal generator. (a) First stage; (b) Last stage

[8]. For the first stage, one XOR gate and ($P_m/2+1$) AND gates are used while in Ref. [8] ($P_m/2$) AND gates are used. For the last stage, the hardware complexity is reduced dramatically, one INVERTER and ($P_m/2+1$) AND gates are used in our proposed structure while ($P_m/2$) AND gates and ($P_m/2+1$) XOR gates are used in Ref. [8].

Tab. 3 demonstrates the synthesis results using the TSMC 0.18-μm standard cell CMOS technology. The modified 96×96 Benes network can be implemented with an area of 0.693 mm^2 and a maximum clock frequency of 118 MHz. And the control signal generator implementation occupies an area of 0.085 mm^2, which can save 25.4% area compared with Ref. [8]. And the overall latency of our network can achieve a 36.2% reduction compared with Ref. [8].

Tab. 3 Hardware complexity using TSMC 0.18-μm

Parameter	Ref. [7]	Ref. [8]	This paper
Network size	128×128	96×96	96×96
Switch network/mm^2	0.909	0.608	0.608
Control signal/mm^2	1.262	0.114	0.085

4 Conclusion

In this paper, a modified Benes shuffle network is proposed to support all the 19 modes required in the reconfigurable WiMAX LDPC decoder. This non-blocking network is also optimal even when the input size is not a power of two. And an efficient algorithm to generate the control signals for this network is also presented to reduce the overall latency of the network. Compared with previous published work, the proposed network architecture has lower hardware complexity. From the hardware synthesis results, compared with the previous work, the area saving of our control signal generator is 25.4%, and the overall latency reduction of the shuffle network is 36.2%.

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一种用于 WiMAX 系统中 LDPC 译码器的改进型 Benes 网络结构

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摘要:提出了一种性能优化的 Benes 网络结构作为开关网络用于 WiMAX 系统中的低密度奇偶校验码译码器. 该网络结构在译码器的输入数目不是 2 的指数时,能获得最优化的性能. 该网络结构是非阻塞的并且可以实现输入输出之间的任何排列组合,因此可以支持 WiMAX 系统中规定的 19 种模式. 为了减少网络结构的硬件复杂度,提出一种用来产生该网络中所有 2×2 开关的控制信号的高效算法. 同时,使用该高效算法可以减少整个网络的延时. 结果表明,该控制信号的生成电路可以节省 25.4% 的芯片面积,并且总体网络的延时可以缩短 36.2%.

关键词:全球互通微波存取(WiMAX); 准循环低密度奇偶校验码; 低密度奇偶校验码译码器; Benes 网络

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