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Analysis and design of sigma-delta interface circuit for quartz flexural pendulum accelerometer

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Abstract: For the high resolution required in a digital interface circuit of an accelerometer used in feeble gravity measurement, a switched-capacitor (SC) sigma-delta modulator (SDM) is proposed. Based on the principle and the topology structure of the SDMs, the influence of oversampling ratio, bits of an internal quantizer and the cascaded structure on weak signal detecting precision is analyzed, and an ideal low-distortion SDM with a second-order 1-bit structure satisfying the high-resolution interface circuit of an accelerometer is designed. With the research on non-idealities of each SDM block in the SC circuit implementation and their impacts on power consumption, the realized parameters of low-power SDMs based on different bandwidths are devised and the power consumption of each SDM is estimated. Time-domain behavioral simulation is explored based on Simulink. The results demonstrate that a 21-bit resolution of the designed SDMs can be achieved on the premise of low power, and the parameters for the circuit implementation can be directed to the transistor-level circuit design.

Key words: switched-capacitor (SC) circuit; sigma-delta modulator (SDM); high resolution; non-ideality; low power

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Gravity data is one of the important fundamental information sources for earth science research, resources exploration, national economic construction and national defense construction. Gravimetry can be divided into ground gravimetry, marine gravimetry, airborne gravimetry and satellite gravimetry[1-2]. The airborne gravity gradiometry has been widely used due to its high resolution. There are two airborne gravity gradient surveying systems, the partial tensor gradient measuring system of BHP company in Australia called Falcon and the full tensor gradient measuring system of Bell Aerospace Company in the USA called Air-FTG™, which have been put into commercial applications at present. The core component of the two systems is both a gravity gradient instrument (GGI) which contains four accelerometers mounted on a rotating platen[3-4]. The control loop in a flexural pendulum accelerometer was designed and analyzed in Ref. [5], and it was presented that accelerometers with a resolution of $10^{-10}g$ can lead the smallest change in capacitance to an aF level, which requires that the digital output interface circuit must have a high resolution. A sigma-delta modulator (SDM) can achieve more than 20-bit resolution in analog-to-digital conversion, and this paper presents the analysis and design of an SDM in the weak signal detecting circuit for a quartz flexural pendulum accelerometer.

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1 High Resolution of SDM

An SDM, which is combined with the oversampling technology to achieve high resolution in analog to digital conversion, is a closed-loop system consisting of an integrator and a low-resolution internal quantizer. A first-order SDM is illustrated in Fig. 1.

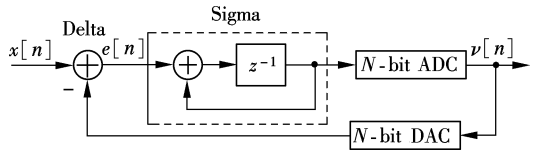

Fig. 1 Block diagram of a first-order SDM

One can assume that the input signal is a sinusoidal wave, and then the maximum possible signal-to-quantization noise ratio (SQNR) for an N-bit A/D converter is

$$\mathrm{SQNR}_{\max} = 20\log(2^N - 1) + 1.76 \quad (1)$$

If the same input signal is used in the first-order SDM (N-bit internal quantizer), the best SQNR confined by the modulator quantization noise is

$$\mathrm{SQNR}_{\max} = 20\log(2^N - 1) + 1.76 - 5.17 + 30\log\mathrm{OSR} \quad (2)$$

where OSR is the oversampling ratio.

It can be seen that an SDM has a high resolution when comparing Eq. (1) with Eq. (2). For example, if the bandwidth of an input signal is 1 kHz and a sampling clock is 1 MHz, then the OSR is 500 and the first-order 1-bit SDM can result in 77 dB in $\mathrm{SQNR}_{\max}$ (equivalent to 12.5 bit of resolution). Eq. (2) also depicts that every doubling of the OSR generates an increase of 9 dB in SQNR (1.5 bit increase in the resolution).

High-order single-loop SDMs can be constructed by inserting $L(L \geqslant 3)$ integrators into the forward path of the modulator (see Fig. 1), while the topology of MASH (multi-stage noise shaping) can be constructed by cascading several low-order single-loop SDMs. They can both produce higher resolution as follows:

$$\mathrm{SQNR}_{\max} = 20\log(2^N - 1) + 1.76 - 10\log\frac{\pi^{2L}}{2L+1} + 20(L + 0.5)\log\mathrm{OSR} \quad (3)$$

However, these structures also have some limitations. High-order single-loop SDMs encounter instability problems and noise cancellation circuits in MASH structures cause noise leakage problems; therefore, the choice of the appropriate structure should be based on actual requirements.

2 SDM Design

2.1 Resolution requirements of interface circuit

The input and output of a quartz flexural pendulum accelerometer shown in Fig. 2 are inertial acceleration and corresponding current, respectively. When there is an acceleration input, the quartz proof mass goes off the balanced position by inertia force, while the moving electrode on the proof mass combined with the fixed electrode senses the angle deflection and transforms it into the capacitance change. The capacitance change is then converted to the corresponding current signal by a switched-capacitor (SC) charge amplifier and then the current signal is fed back to the torque coil. Torque coils suffer from the electromagnetic force in the air gap magnetic field and work in a push-pull mode, which puts the tongue-shaped proof mass back to the equilibrium position[6]. The current in torque coils is in proportion to the input acceleration, so detecting the torque coil current can obtain the input acceleration. For computer calculations, the accelerometer system needs to add an ADC in the forward path and a corresponding DAC in the feedback path. After the introduction of a 1-bit SDM, the resolution of an ADC can be achieved more than 1 bit with two simple converters.

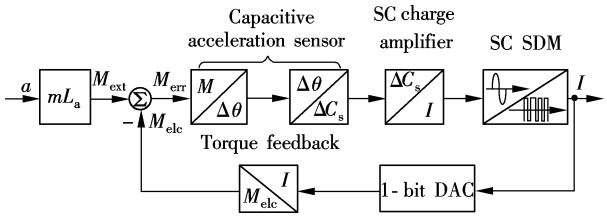

Fig. 2 A sigma-delta capacitive accelerometer

Assume that the minimum change in capacitance is at an aF level and the gain of the SC charge amplifier is at an A/pF level, then the amplifier output is at a μA level. Resolution of a 10^{-6} level in an SDM is required to detect a μA current signal. If the full-scale output of the quantizer is 1 V, it is calculated from the equation of $1/(2^N - 1) = 10^{-6}$ that the effective number of bits (ENOB) in the modulator should be at least 20 bit. Accordingly, an SDM with a 24-bit resolution is set as the target for the margin.

2.2 Determination of SDM topology

The bandwidth of a gravity signal is usually small (taking 500 Hz as an example), and the possible structures which achieve the target resolution can be predicted according to Eq. (3). Considering the simplicity of the circuit, the stability of the modulator and the feasibility of the sampling rate, the SDM with a second-order 1-bit single loop is selected. In the low-distortion feed-forward structure as shown in Fig. 3, as long as the design of the structural parameters makes the input signal transfer function be one[7], it yields the output without the input signal, which avoids distortion.

In the SC circuit, a structural parameter of the modulator is implemented by a capacitance ratio. The gain of the input signal b_1 and the gain of feedback signal c_1 in Fig. 3 are often taken as the same, which means that they have the same capacitance ratio, and can share an identical input capacitor. In addition, structural parameters are usually less than 1 in order to make sure that the output of the integrator will not overload. However, the feed forward parameters a_1 and a_2 are exceptions due to being gains of the input of a 1-bit quantizer (comparator). Therefore, the structural parameters of the SDM can be designed as follows: $a_1 = a_2 = 6$, $b_1 = c_1 = 1/3$, $c_2 = 0.5$.

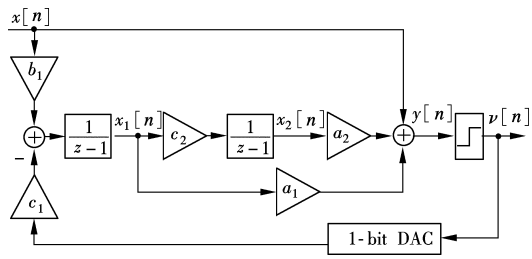

Fig. 3 A low-distortion second-order 1-bit SDM

2.3 Design of the block parameters

In the actual SC circuit, the ideal performance of an SDM is degraded by such various non-idealities as the non-ideal operational amplifier, thermal noise of integrators and clock jitter. The finite DC gain of an opamp changes the transfer function of an integrator, while the finite gain-bandwidth product (GBW) and the slew rate (SR) of an opamp produce an incomplete settling error or distortion in the modulator output[8]. These non-idealities must be taken into account in the design of block performance parameters in the SC SDM.

In addition to considering high sensitivity to the feeble signal during the design of an SC SDM, minimizing the power consumption is needed. There is a figure-of-merit (FOM) for the low-pass sigma-delta IC performance, which illustrates the power of each conversion with the unit of pJ/conversion. It is defined as[9]

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \times \mathrm{DOR}} \times 10^{12} \tag{4}$$

where DOR is the digital output rate, which equals twice the input signal bandwidth. The smaller the FOM value, the less the power consumption of the SDM.

Several low-power SC SDMs are designed for the signal bandwidths of 500, 50, 5 and 1 Hz, respectively based on the ideal SDM. Presuming that the supply range is 3.3 V, the reference voltage is 1 V and the temperature is 300 K, the design parameters of SDMs are shown in Tab. 1 and their estimated power consumption is shown in Tab. 2.

Tab. 1 Design parameters for SDMs with different bandwidths

Bandwidth/Hz	Sampling frequency/kHz	Sampling capacitor/nF	Operational amplifier					RSM of sampling jitter/ns
			Maximum output current/mA	GBW/MHz	SR/(V·μs^{-1})	Transconductance of input transistors/(A·V^{-1})	DC gain/dB	
500	3 072	1.161 0	56.82	13.52	155.9	0.134 8	65.0	1
50	819.2	0.426 8	2.462	3.604	18.39	0.029 9	73.6	1
5	81.92	0.426 8	0.113 6	0.360 4	0.848 6	0.006 5	73.6	1
1	16.38	0.426 8	0.014 2	0.072 1	0.106 1	0.002 1	73.6	1

Tab. 2 Estimation of the performance of SC SDMs

Bandwidth/Hz	Static power consumption/mW	Dynamic power consumption/mW		FOM/pJ
		Analog circuit	Digital circuit	
500	1 500	171	0.15	99.6
50	65	16.8	0.041	48.8
5	3	1.68	0.004 1	27.9
1	0.375	0.338	0.000 8	21.2

3 Behavioral Simulation and Results

The SDtoolbox developed by Simona Brigati and others is used for behavioral simulation of SDMs. It contains a set of Simulink blocks which consider the major non-idealities, such as clock jitter, thermal noise, and operational amplifier parameters (finite DC gain, GBW and SR)[10]. The behavioral simulation model of a second-order two-level SDM based on this toolbox is shown in Fig. 4.

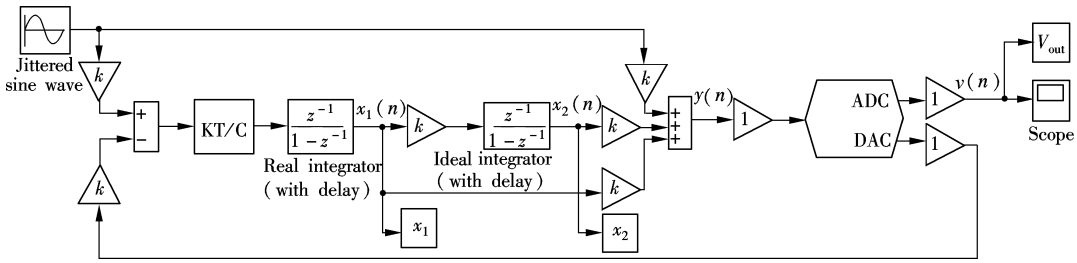

Fig. 4 Simulation model of the second-order two-level SDM

Taking the designed SDM with a signal bandwidth of 1 Hz as an example, its simulation conditions are as follows: the sampling frequency is 16.38 kHz; the input signal is a sinusoidal with an amplitude of 0.25 V and a frequency of 0.5 Hz; sampling points are 2^{18}. Fig. 5(a) shows the power spectrum of the modulator output, from which the SNR is calculated as 124.6 dB. Figs. 5(b) and (c) show the output SNR and the maximum absolute output of the two integrators as a function of the input signal amplitude, respectively. It can be revealed that the output of the second integrator is not overloaded and the output is less than −1 dB in the input level. The dynamic range (DR) of SDMs is defined as[11]

$$\mathrm{DR} = \mathrm{SNR_L} + 12\ \mathrm{dB} + 20\log(\mathrm{OL}) \qquad (5)$$

where $\mathrm{SNR_L}$ is the SNR for a relative input amplitude of −12 dB (a linear scale of 0.25), and OL is the relative input amplitude in the linear scale when the structure overloads. It can be obtained that $\mathrm{SNR_L}$ is 125.1 dB and 20log(OL) is −1 dB from Figs. 5(b) and (c), respectively, and then DR is 136.1 dB using Eq. (5), which also means that ENOB = (DR − 1.76)/6.02 ≈ 22.3 bit.

The $\mathrm{SNR_L}$, DR and ENOB of the designed SDMs with different signal bandwidths are shown in Tab. 3, which clarifies that the resolution of each SDM considering non-idealities and low power can be still over 21 bit.

Tab. 3 Resolution of the designed SDMs

Bandwidth/Hz	$\mathrm{SNR_L}$/dB	DR/dB	ENOB/bit
500	122.8	133.8	21.9
50	123.3	134.3	22.0
5	125.9	136.9	22.4
1	125.1	136.1	22.3

4 Conclusion

The quartz flexural pendulum accelerometer used in gravity measurement does not only require high-sensitivity sensors but also high-resolution interface circuits. An SDM combines oversampling with noise shaping to improve the resolution of analog to digital conversion, which is extensively applied to the weak signal detection. This paper presents some designed high-resolution low-power SC SDMs with different

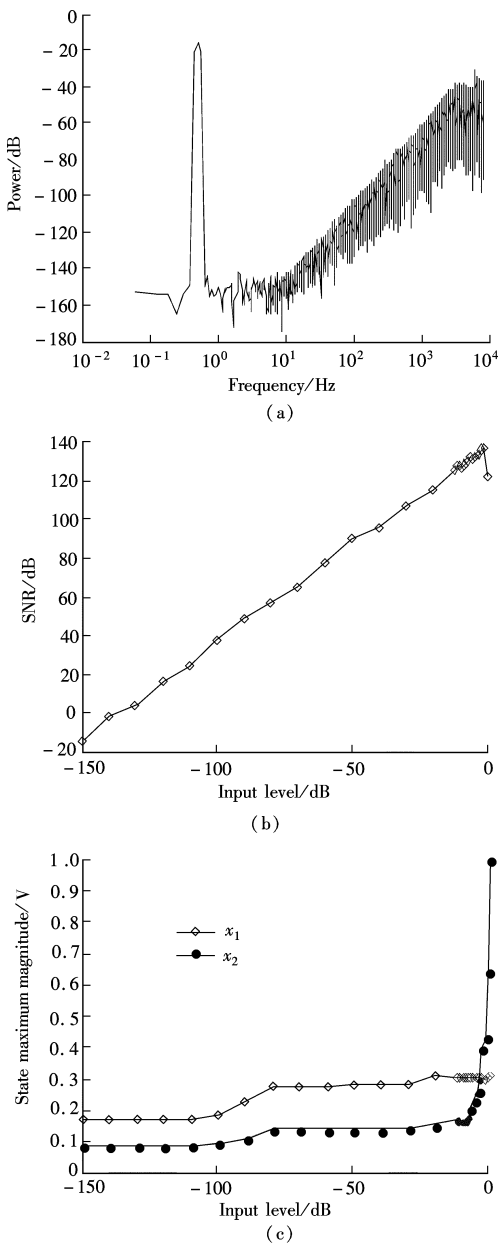

Fig. 5 Analysis of SDM output. (a) Power spectrum; (b) SNR vs. input level; (c) Maximum output of two integrators vs. input level

signal bandwidths which are verified by behavioral simulations. The results show that the designed SDMs are reasonable, whose specifications can be a guide to future transistor-level circuit design.

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石英挠性摆式加速度计 sigma-delta 接口电路的分析与设计

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摘要:针对微弱重力信号测量中加速度计的数字输出接口电路应具有高分辨率的问题,引入了开关电容(SC) sigma-delta 调制器(SDM). 基于 SDM 的工作原理和拓扑结构,分析了过采样比、内部量化器位数以及级联结构对提高微弱信号检测精度的影响,设计了满足加速度计接口电路高分辨率要求的理想二阶 1 位低失真 SDM 结构. 通过研究各模块在 SC 电路实现中的非理想特性及其对电路功耗的影响,设计了基于不同带宽的低功耗 SDM 实现参数,给出了相应的功耗估计. 利用 Simulink 对各设计方案进行了时域的行为级仿真. 结果表明,所设计 SDM 在低功耗的前提下其分辨率可达 21 位以上,其电路实现参数可用于指导晶体管级电路设计.

关键词:开关电容电路;sigma-delta 调制器;高分辨率;非理想特性;低功耗

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