Journal of Southeast University (English Edition) Vol. 28, No. 4, pp. 398 - 403 Dec. 2012 ISSN 1003—7985

Design of 10 Gbit/s burst-mode transimpedance preamplifier for PON systems

Gu Gaowei Zhu En Lin Ye

(Institute of RF and OE-ICs, Southeast University, Nanjing 210096, China)

Abstract: A 10 Gbit/s burst-mode preamplifier is designed for passive optical networks (PONs). To achieve a high dynamic range and fast response, the circuit is DC coupled, and a feedback type peak detector is designed to perform auto-gain-control and threshold extraction. Regulated cascade (RGC) architecture is exploited as the input stage to reduce the input impedance of the circuit and isolate the large parasitic capacitance including the photodiode capacitance from the determination pole, thus increasing the bandwidth. This preamplifier is implemented using the low-cost 0.13 μm CMOS technology. The die area is 425 μm × 475 μm and the total power dissipation is 23.4 mW. The test results indicate that the preamplifier can work at a speed from 1.25 to 10.312 5 Gbit/s, providing a high transimpedance gain of 64.0 dBΩ and a low gain of 54.6 dBΩ with a dynamic input range of over 22.9 dB. The equivalent input noise current is 23.4 pA/$Hz^{1/2}$. The proposed burst amplifier satisfies related specifications defined in 10G-EPON and XG-PON standards.

Key words: burst-mode; passive optical network (PON); transimpedance preamplifier; regulated cascade (RGC); peak detector; auto-gain-control; threshold extraction

doi: 10.3969/j.issn.1003 - 7985.2012.04.005

Gigabit-class passive optical network (PON) systems such as ethernet PON (EPON) and gigabit-capable PON (GPON) are widely developed as a flexible, large-capacity, and economical solution for fiber-to-the-home (FTTH) access. To meet the increasing demand of user bandwidth, the next generation PON systems are being actively discussed to offer even higher data rates. In 2009, IEEE 802.3av task force approved a 10-Gigabit Ethernet PON (10GE-PON)[1] standard, and ITU-T G.987.2 recommendation series about 10-Gigabit-capable PON (XG-PON)[2] have been ratified in succession from 2010.

To realize the PONs, one of the key components is the burst-mode optical receiver in the optical line termination (OLT). Several burst-mode optical receivers and transimpedance amplifiers have been reported by overseas institutes in recent years, most of which work on a data rate of 1.25 Gbit/s[3-6] and efforts are being made towards 10 Gbit/s burst receivers[7]; yet implementations of such devices remain blank in China.

In this paper, we design and implement a 10 Gbit/s burst-mode transimpedance preamplifier with fast-response auto-gain-control function and threshold extraction for burst-mode applications in SMIC 0.13 μm CMOS technology.

1 Burst-Mode Receiver Requirements

A PON system is a point-to-multipoint (P2MP) network over a single branched topology, as illustrated in Fig. 1. A number of (typically 16 or 32) optical network units (ONUs) located at the subscriber premises are connected to one optical line terminal (OLT) which resides at the service provider's facility through a passive optical distribution network (ODN). In the downstream direction from the OLT to an ONU, continuous signals are transmitted by the OLT through passive splitters and reach each ONU. In the upstream direction from the ONUs to the OLT, both 10G-EPON and XG-PON systems adopt a time-division-multiplexing (TDM) method. Signals are transferred in burst-mode: an ONU can only launch burst data packets in the dedicated time slots and the OLT should receive data packets generated from different ends. Due to different transfer distances, the transfer loss differs greatly with a range of over 15 dB. Besides, there are multiple data rates on the same network. 10G-EPON supports two configurations of the symmetric rate (10 Gbit/s downstream and 10 Gbit/s upstream) and the asymmetric rate (10 Gbit/s downstream and 1.25 Gbit/s upstream). The XG-PON standard allows coexistence of different line rates of XG-PON1 featuring a 2.5 Gbit/s upstream path and XG-PON2 featuring a 10 Gbit/s one. On the other side, the preamble time of each packet is limited for transfer efficiency. The settling time for the OLT receiver should be less than 800 ns according to the 10G-EPON standard (IEEE 802.3av). The XG-PON specifications are much stricter. The total preamble time is only 100 ns, for transmitter turning on/off, receiver settling, and clock recovering. These specifications impose new challenges on the OLT receiver design in terms of speed, sensitivity, dynamic range, and settling time, implying that

Received 2012-04-24.

Biographies: Gu Gaowei (1982—), female, graduate; Zhu En (corresponding author), male, doctor, professor, zhuenpro@seu.edu.cn.

Foundation item: The Key Technology Research and Development Program of Jiangsu Province (No. BE2008128).

Citation: Gu Gaowei, Zhu En, Lin Ye. Design of 10 Gbit/s burst-mode transimpedance preamplifier for PON systems. [J]. Journal of Southeast University (English Edition), 2012, 28(4): 398 - 403. [doi: 10.3969/j.issn.1003 - 7985.2012.04.005]

the receiver architecture as well as blocks should be revised for burst-mode communication.

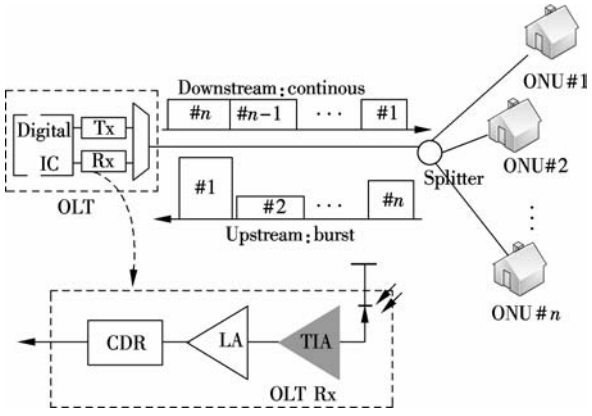

Fig. 1 TDM-PON system

2 Circuit Description

2.1 Architecture design

In an optical receiver, the preamplifier is used for converting a weak photo-current generated by an external photodiode (PD) into a visible voltage signal. The input photo-current is

$$i_s(t) = R_0 P(t) \tag{1}$$

where R_0 is the responsivity of the photodiode (i.e., 0.9 A/W) and $P(t)$ is the received optical power. Since the power is always a positive value, both the DC current and the decision threshold vary according to the maximum received power of each packet. In a continuous-mode optical communication system, the DC offset can be cancelled by an AC-coupled architecture. For burst-mode receiving, a DC-coupled architecture is employed to achieve a short settling time, so a fast-response threshold extraction circuit is essential. Gain switching is also necessary for processing the input signal of a wide dynamic range without overdrive or distortion. The block diagram of the proposed preamplifier is shown in Fig. 2, including two matched variable-gain transimpedance amplifiers (TIA), a novel peak detector which performs fast-response auto-gain-control and threshold extraction, a single-to-differential (S2D) circuit and an output buffer. TIA1 is used to convert the input current into a voltage signal and TIA2 is to provide a reference.

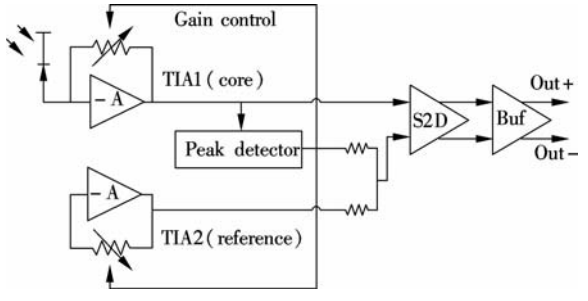

Fig. 2 Architecture of the proposed preamplifier

2.2 TIA design

There is an inevitable large parasitic capacitance at the input node of the preamplifier which is contributed by the photodiode, pad and so on. For a total input capacitance C_{in} of 250 fF, the input resistance of the TIA should be smaller than 80 Ω to achieve a bandwidth of 8 GHz. The first issue in a multi-gigahertz preamplifier design is to reduce the input impedance of the TIA and isolate C_{in} from the following amplifier stages.

The designed variable gain TIA is composed of three stages: the regulated cascade (RGC) input stage[8], the common-drain (CD) stage and the common-source (CS) amplifier stage with a switchable feedback resistor, as shown in Fig. 3.

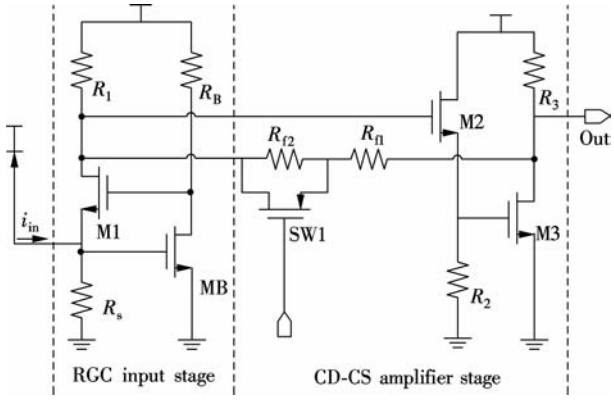

Fig. 3 RGC-CDCS TIA

The RGC input stage provides a positive feedback of $g_{m,B}R_B$. When M1 keeps in the saturation region, the input impedance Z_{in} is obviously reduced and can be approximately calculated as

$$Z_{in} \approx \frac{1}{g_{m,1}} \frac{1}{(1 + g_{m,B}R_B)} \tag{2}$$

The domain pole of the TIA is thus pushed from the input node to the output node of the RGC stage. A CD stage is inserted after the RGC stage. Due to the Miller effect, the equivalent capacitance at the gate of transistor M2 is reduced to $(1 - g_{m,2}R_2)C_{gs,2}$. This CD stage also shifts the signal level of the RGC out to a better operating point of the common source amplifier stage. Feedback resistors connect the output of the CS stage and the input node of the CD stage, and ensure a more stable gain and a larger dynamic range. Supposing that $R_1 \gg R_f$, the low frequency transimpedance gain of the TIA is determined as

$$Z_T(0) \approx -\alpha_2 g_{m,3} R_3 \left[R_1 \parallel \frac{R_f}{1 + \alpha_2 g_{m,3} R_3} \right] \tag{3}$$

where

$$\alpha_2 = \frac{g_{m,2}R_2}{1 + g_{m,2}R_2} \tag{4}$$

$$R_f = R_{f1} + (R_{f2} \parallel r_{ds,SW1}) \tag{5}$$

and the 3-dB bandwidth is

$$f_{3dB} \approx \frac{1 + \alpha_2 g_{m,3} R_3}{2\pi R_f (C_{gd,1} + (1 - \alpha_2) C_{gs,2} + C_{gd,2})} \tag{6}$$

2.3 Peak detector, gain-switching, and threshold-extraction

The reported peak detectors for optical receivers are mainly implemented utilizing diodes or diode-connected transistors. Unfortunately, within our available technologies (CMOS or 0.18 μm SiGe BiCMOS), simulation results show that these diodes present a too large capacitance to work at gigabit data rates. A novel peak detector is presented, employing a feedback architecture based on a common-source differential amplifier, so it can work at a rather high speed. Due to the inverting feature of the designed TIA core, a negative peak detector corresponding to the maximum optical power is actually implemented. The circuit of this peak detector and the gain-control cell is demonstrated in Fig. 4.

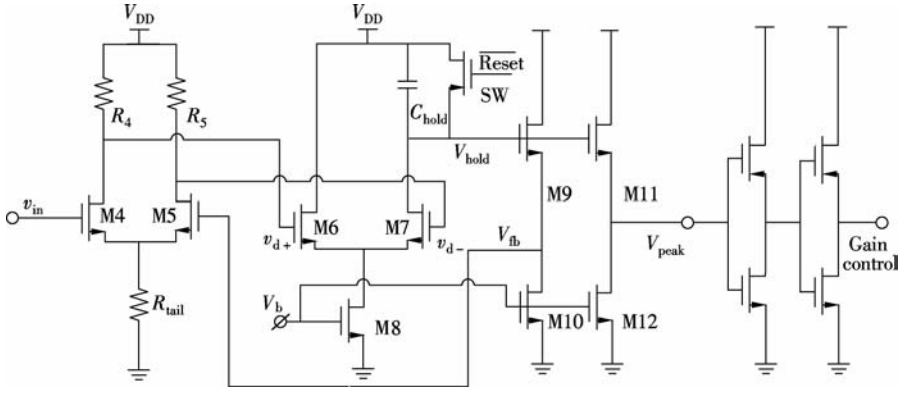

Fig. 4 Negative peak-detector and gain-control

Transistors M4, M5 and resistor loads R_4, R_5 compose a differential amplifier stage. The difference between the input voltage signal v_{in} and the feedback voltage V_{fb} is calculated and amplified to v_d with a voltage gain of A_{v1}. The current tail in Fig. 4 is realized using the resistor R_{tail} instead of a biased MOS transistor for a larger track range. This also compensates for the nonlinearity of the detected peak value. M6 and M7 form another differential pair. V_{ov} is defined as the overdrive voltage of M6 when all the tail current of M8 flows through M6. The circuit can track the lowest input value when the reset switch is cut-off. In this condition, if $v_d < V_{ov}$, then

$$V_{fb} > v_{in} - \frac{V_{ov}}{A_{v1}} \tag{7}$$

There is current flowing through the capacitor C_{hold}. The voltage of V_{hold} decreases, and so does the feedback signal V_{fb} and the negative peak value V_{peak} until the circuit reaches the steady state.

$$V_{fb,steady} = \min v_{in} - \frac{V_{ov}}{A_{v1}} \tag{8}$$

M9 and M10, M11 and M12 are two source followers with different voltage drops. With the dedicated designed device parameters, the fixed error between $\min v_{in}$ and V_{fb} can be compensated for.

A two-stage CMOS inverter is inserted to obtain a rail-to-rail gain control signal. The maximum output of the TIA corresponding to the dark photo-current can be obtained through the output voltage of the reference TIA (V_{ref}). In this way, the decision threshold can be easily extracted as

$$V_{TH} = \frac{V_{peak} + V_{ref}}{2} \tag{9}$$

The working process of the fast-response peak detector is simulated and shown in Fig. 5. Fig. 5(a) is the input current signal with different amplitudes, and Fig. 5(b) is

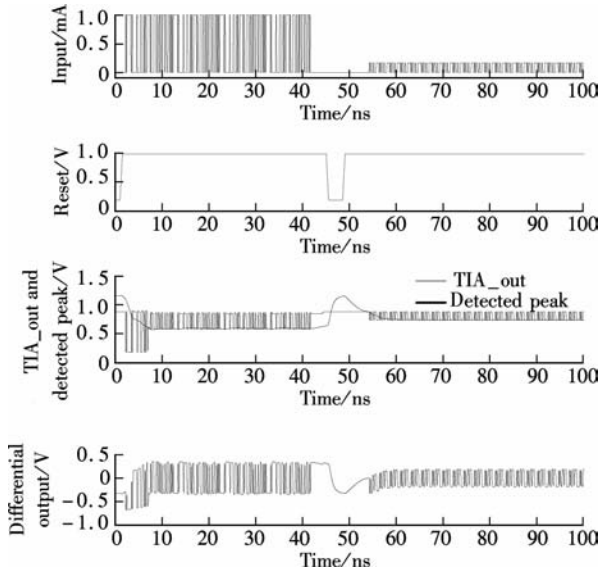

Fig. 5 Transient simulation results. (a) Input current signal; (b) Reset signal; (c) TIA_out and detected peak; (d) Differential output.

the reset signal given by upper-layer protocols to indicate the end of each data packet. At the beginning of a new coming packet, the current signal is first amplified by the core TIA to a voltage signal (TIA_out) with the maximum transimpedance gain. The negative peak detector tracks the bottom of the TIA output and switches the TIA transimpedance to a low-gain mode if the detected negative value is lower than the presupposition, as shown in Fig. 5(c). The threshold is extracted at the same time. Finally, in Fig. 5(d), we obtain the simulation results of the differential output of the proposed preamplifier. The simulation results indicate that the required time for the gain-switching and threshold extraction is less than 20 ns.

3 Layout and Experimental Results

The designed burst-mode transimpedance preamplifier is fabricated in the SMIC 0.13 μm CMOS process and the micrograph is shown in Fig. 6. Due to the absence of peaking inductors, the core circuit occupies an area of only 136 μm × 90 μm, and the total chip size is 425 μm × 475 μm. This circuit is measured on a cascade probe station. The total power dissipation is 23.4 mW under a 1.2 V supply voltage.

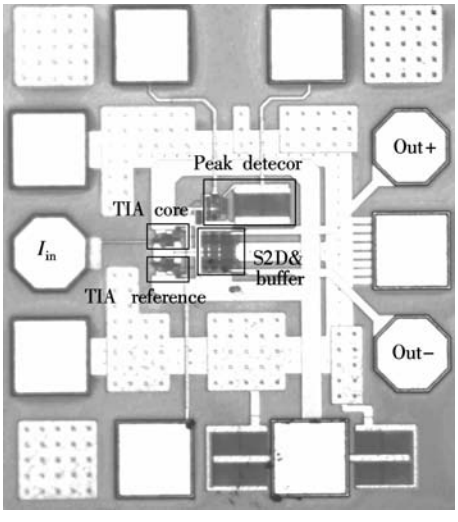

Fig. 6 Micrograph of the burst-mode preamplifier

Eye-diagram tests are performed with a $2^{23}-1$ pseudo-random bit sequence (PRBS) pulse for different data rates and input amplitudes. Fig. 7 shows the measured eye-diagram at different line rates of 1.25 Gbit/s and 10.312 5 Gbit/s with a 20 mV input voltage. Due to the noise generated by the circuit itself, the pattern generator, the oscillator, and the environment, the minimum input peak-to-peak voltage ($V_{P\text{-}P}$) is 5 mV. The exact measurement of sensitivity is done by the noise analyzer, which will be described later. Fig. 8 is the output eye-diagram of 10 Gbit/s PRBS for different input amplitudes of 5 and 200 mV, respectively.

Frequency characterizations of the amplifier are tested through the Agilent E83638 network analyzer. Since the

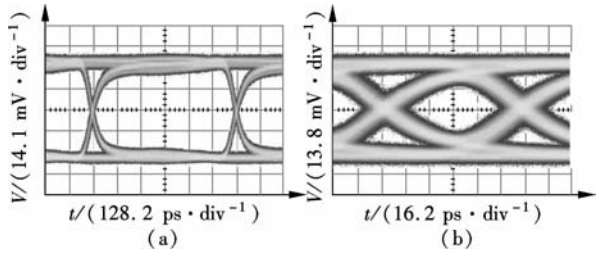

Fig. 7 Eye diagrams of different data rates. (a) 1.25 Gbit/s; (b) 10.312 5 Gbit/s

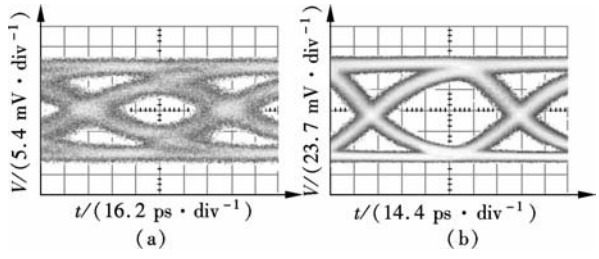

Fig. 8 Eye diagrams of different input amplitudes. (a) Input $V_{P\text{-}P}=5$ mV; (b) Input $V_{P\text{-}P}=200$ mV

high-frequency network analyzers are mostly single-ended, only single-ended *S*-parameters are measured. The input impedance Z_{in} and transimpedance gain Z_T can be calculated as

$$Z_{in}=Z_{11}-\frac{Z_{21}Z_{12}}{Z_{22}+Z_0} \tag{10}$$

$$Z_T=Z_{21}=\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}}Z_0 \tag{11}$$

where Z_{11}, Z_{12}, Z_{21} and Z_{22} are the *Z*-parameters of the amplifier which can be derived from *S*-parameters, and Z_0 is 50 Ω. The input-referred equivalent noise current density is tested by the Agilent N8975A noise figure analyzer and it is derived as

$$\overline{i_{n,eq}}=\sqrt{\frac{4kTR_s}{|Z_{in}+R_s|^2}(10^{NF/10}-1)} \tag{12}$$

where k is Boltzmann's constant; T is the absolute temperature; R_s equals 50 Ω; and NF is the measured noise figure. Assuming that the responsivity of the PD is 0.9 A/W, the bit-error-ratio (BER) can be estimated using the following formula[4]:

$$\mathrm{BER}=\mathrm{erfc}\left(\frac{Q}{\sqrt{2}}\right) \tag{13}$$

where

$$Q^2=\mathrm{SNR} \tag{14}$$

In other words,

$$Q=\frac{P_{sen}}{i_n\sqrt{B/R_0}} \tag{15}$$

where P_{sen} is the sensitivity of the whole preamplifier.

The test results are shown in Fig. 9. The measured input impedance is about 60 Ω due to the RGC input stage. The high transimpedance gain is 64.0 dBΩ (1.58 kΩ), and the 3-dB bandwidth is 6.13 GHz. For the large input signals, the transimpedance of the low gain state is also tested, and the gain is 54.6 dBΩ with a 3-dB bandwidth of 6.62 GHz. The equivalent input noise current density is measured to be 23.4 pA/Hz$^{1/2}$. This is larger than the simulated result due to various environmental disturbances. The estimated sensitivity is −19.6 dBm at a BER of 10^{-9} and a dynamic range of over 22.6 dB as the preamplifier has an overload input current larger than 2 mA.

A comparison of the burst-mode transimpedance amplifiers reported in recent years is given in Tab. 1. Our design presents a high transimpedance gain as well as a high speed, which satisfies the related specifications defined in 10G-EPON and XG-PON standards.

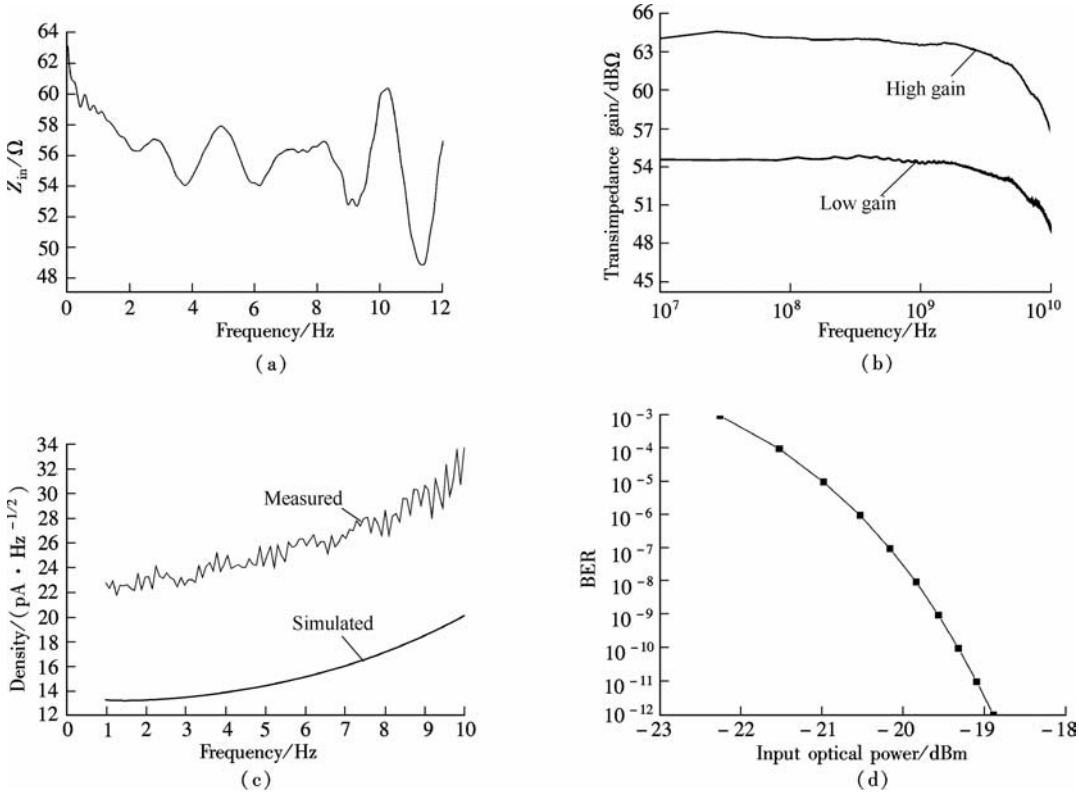

Fig. 9 Test results. (a) Input impedance; (b) Transimpedance gain; (c) Equivalent input noise; (d) Sensitivity

Tab. 1 Performance comparison of the burst-mode transimpedance amplifier

Reference	Ref. [9]	Ref. [6]	Ref. [10]	Ref. [11]	Proposed
Process	0.18 μm CMOS	0.25 μm SiGe BiCMOS	0.18 μm CMOS	0.35 μm CMOS	0.13 μm CMOS
Data rate/(Gbit · s^{-1})	3	9.8	2.5	NA	10
Z_T/dBΩ	66 57	NA	59 (High) 54 (Low)	66 (High) 55 (Low)	64.0 (High) 54.6 (Low)
Bandwidth/GHz	2.1	NA	1.9/2.5	0.256/0.305	6.13/6.62
Sensitivity/dBm	−23.3	−15	NA	NA	−19.6
Dynamic range/dB	17	12.2	NA	NA	22.9
Power/mW	43.2	400	54	12	23.4
Area/mm^2	0.27	1.98	NA	NA	0.20
Year	2005	2008	2008	2009	2011

4 Conclusion

A burst-mode transimpedance preamplifier for 10 Gbit/s TDM-PON applications, including variable gain TIA and fast-response peak-detector cell is implemented in SMIC 0.13 μm CMOS technology. The chip area is 425 μm × 475 μm, and the power dissipation is 23.4 mW. Experimental results show that the preamplifier provides a high transimpedance gain of 64.0 dBΩ with a 3-dB bandwidth of 6.13 GHz and a low gain of 54.6 dBΩ with a 3-dB bandwidth of 6.62 GHz. The input-referred noise current is 23.4 pA/Hz$^{1/2}$, corresponding to a sensitivity of

−19.6 dBm for a BER of 10^{-9}, and the dynamic range is over 22.9 dB.

References

[1] IEEE 802.3av 10G-EPON Task Force. Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specification, amendment 1: physical layer specifications and management parameters for 10 Gb/s passive optical networks [S]. New York: The Institute of Electrical and Electronics Engineers, Inc., 2009.

[2] ITU-T. G.987.2 10-gigabit-capable passive optical networks (XG-PON): physical media dependent (PMD) layer specification [S]. Geneva: Telecommunication Standardization Sector of International Telecommunication Union, 2010.

[3] Oh Y-H, Lee S-G, Le Q, et al. A burst-mode receiver for 1.25-Gb/s Ethernet PON with AGC and internally created reset signal [J]. *IEEE Journal of Solid-State Circuits,* 2004, **39**(12): 2379−2388.

[4] Ko H-S, Han S, Lee M-S, et al. 1.25 Gb/s burst-mode optical receiver for the Ethernet PON using 0.35 μm CMOS technology [C]//*The 6th International Conference on Advanced Communication Technology.* Phoenix Park, South Korea, 2004: 2379−2388.

[5] Schneider K, Zimmermann H. Three-stage burst-mode transimpedance amplifier in deep-sub-μm CMOS technology [J]. *IEEE Transactions on Circuits and Systems,* 2006, **53**(7): 1458−1467.

[6] Lee S-H, Kim J, Le Q, et al. A single-chip 2.5-Gb/s burst-mode optical receiver with wide dynamic range [J]. *IEEE Photonics Technology Letters,* 2011, **23**(2): 85−87.

[7] Ridder T D, Ossieur P, Baekelandt B, et al. A 2.7 V 9.8 Gb/s burst-mode TIA with fast automatic gain locking and coarse threshold extraction [C]//*IEEE International Solid-State Circuits Conference.* San Francisco, USA, 2008: 220−221.

[8] Park S M, Yoo H J. 1.25-Gb/s regulated cascode CMOS transimpedance amplifier for Gigabit Ethernet applications [J]. *IEEE Journal of Solid-State Circuits,* 2004, **39**(1): 112−121.

[9] Chen W-Z, Gan R-M. 1.8V, variable gain transimpedance amplifiers with constant damping factor for burst-mode optical receiver [C]//*Radio Frequency Integrated Circuits* (*RFIC*) *Symposium.* Long Beach, CA, USA, 2005: 691−694.

[10] Raja K M, Yan D L, Yeoh W G. Burst mode receiver for GPON [C]//*IEEE International Photonics Global Conference* (*IPGC*). Singapore, 2008: 1−4.

[11] Chen R Y, Chang M J. A CMOS variable-gain fully-differential transimpedance amplifier for multimedia data links [C]//*International Conference on Intelligent Information Hiding and Multimedia Signal Processing.* Kyoto, Japan, 2009: 402−405.

10 Gbit/s PON 系统突发模式前置放大器设计

顾皋蔚　朱　恩　林　叶

(东南大学射频与光电集成电路研究所,南京 210096)

摘要:针对无源光网络(PON)设计了 10 Gbit/s 的突发模式前置放大器. 为了获取大动态范围和快速响应,电路采用 DC 耦合结构,并设计了一种反馈型峰值检测单元以实现自动增益控制与阈值提取功能. 利用调节型共源共栅(RGC)结构的输入级单元减小了电路的输入电阻,使得包括光检测器电容在内的大寄生电容与电路的主极点相隔离,从而提高了带宽. 该前置放大器采用低成本的 0.13 μm CMOS 工艺实现,芯片面积为 425 μm×475 μm,总功耗为 23.4 mW. 测试结果表明,电路的工作速率范围在 1.25～10.312 5 Gbit/s,可提供 64.0 dBΩ 的高跨阻增益与 54.6 dBΩ 的低跨阻增益,输入动态范围大于 22.9 dB. 等效输入噪声电流为 23.4 pA/$Hz^{1/2}$. 该放大器可满足 10G-EPON 与 XG-PON 的相关指标.

关键词:突发模式;无源光网络;跨阻前置放大器;调节型共源共栅;峰值检测;自动增益控制;阈值提取

中图分类号:TN722