Frequency synthesizer for DRM/DAB/AM/FM RF front-end

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Abstract: This paper describes a wideband low phase noise frequency synthesizer. It operates in the multi-band, including digital radio mondiale (DRM), digital audio broadcasting (DAB), amplitude modulation (AM) and frequency modulation (FM). In order to cover the signals of the overall frequencies, a novel frequency planning and a new structure are proposed. A wide-band low-phase-noise low-power voltage-control oscillator (VCO) and a high speed, wide band, high frequency division ratio pulse swallow frequency divider with a low power consumption are presented. The monolithic DRM/DAB/AM/FM frequency synthesizer chip is also fabricated in a SMIC's 0.18-μm CMOS process. The die area is 1 425 μm × 795 μm including the test buffer and pads. The measured results show that the VCO operating frequency range is from 2.22 to 3.57 GHz, the measured phase noise of the VCO is 120.22 dBc/Hz at 1 MHz offset; the pulse swallow frequency divider operation frequency is from 0.9 to 3.4 GHz. The phase noise in the phase-locked loop (PLL) is − 59.52 dBc/Hz at 10 kHz offset and fits for the demand of the DRM/DAB/AM/FM RF front-end. The proposed frequency synthesizer consumes 47 mW (including test buffer) under a 1.8 V supply.
Key words: frequency synthesizer; wideband voltage-control oscillator; pulse swallow frequency divider; low phase noise
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R adio broadcasting is a part of our lives that cannot be dismissed, but the traditional broadcast system has inherent shortcomings. The digital radio broadcasting shows the merits of anti noise, anti interferences, anti radio wave propagation weakness, and so on. Thus, the digital radio broadcasting receiver, being compatible with analog radio broadcasting, becomes a research focus. At present, the digital radio receivers of high quality are of less integration scale, expensive, and not compatible with

analog radio broadcasting. Thus, the hot research topic of digital radio is to increase the integration scale, reduce the cost, and be compatible with analog radio broadcasting.

Digital radio mondiale (DRM)[1]/digital audio broadcasting (DAB) [2]/amplitude modulation (AM)/frequency modulation (FM) radio-frequency (RF) front-end is crucial in the design of the radio receiver. Thus, the double conversion low-IF DRM/DAB/AM/FM radio tuner architecture is adopted and the first intermediate frequency is set to be at 35.452 MHz[3]. The frequency grids of the DRM/DAB/AM/FM receiver are 1, 3, 5, 25, 64, and 128 kHz, respectively. The minimum frequency step is 1 kHz, and the maximum frequency step is 128 kHz. The receiving frequency range is from 148.5 to 1 496 MHz; thus the RF local oscillator (LO) tuning range must be able to cover from 35.600 5 to 1 572.452 MHz.

The traditional structure of the frequency synthesizer is the single loop, the single voltage-control oscillator (VCO) and its output signal is the output of the VCO[4]. Now, with the development of multi-standard communication systems, the frequency range becomes wider and wider so that the structure of the frequency synthesizer becomes more and more complicated, for example, including two VCOs in the loop [5–6] or adding the mixer and frequency divider to the outside of loop[7].

In this paper, in order to generate the LO quadrature signals and cover the frequency range of the DRM, DAB, AM and FM, the structure of the frequency synthesizer for DRM/DAB/AM/FM is a single VCO and a single loop, supplemented with a multi-mode frequency divider (MMFD), as shown in Fig. 1.
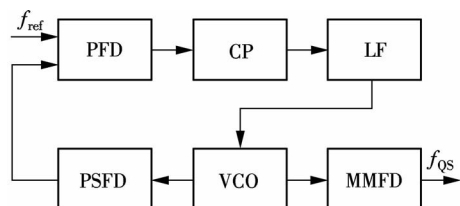

Fig. 1　Structure of DRM/DAB/AM/FM frequency synthesizer

1　Circuit Design

Referring to Fig. 1, the frequency synthesizer consists

of six parts: VCO, pulse swallow frequency divider (PS-FD), phase frequency detector (PFD), charge pump (CP), loop filter (LF), and MMFD. The VCO must be wide-band and of low-phase noise to meet the demands of the frequency plans, and all standards. The PSFD must be of high speed and wide band, high frequency division ratio to cover all the bands. The MMFD is designed aiming at high speed and wide-band low-phase noise to meet the demands of the LO.

1. 1　Voltage-control oscillator

Fig. 2 shows the schematic of the proposed oscillator[3]. It uses a double cross-coupled transconductance structure without tail current source, which is usually preferred in low-power and low phase noise applications. It consists of four parts, including a double cross-coupled transconductance circuit, an LC tank, two LC filter networks, and two isolation circuits for output nodes. The loss of the LC tank is canceled by the double cross-coupled transconductance circuit through generating a negative resistance. The LC tank consists of a spiral inductor, two MOS varactors, and a parallel switchable capacitor bank. The band width of the proposed VCO is controlled by the LC tank. The parallel switchable capacitor bank is a 4-bit coarse tuning element that changes the control codes, and two MOS varactors are fine-tuning elements that change the control voltages. Both the static output voltage and the static current in two sides are set by the size of the MOSFETs. The nominal output $(V+, V-)$ bias point is 0.9 V and the circuit draws a static supply current of about 3.8 mA, which is enough for an oscillation. When the circuit begins to oscillate, it operates in the voltage-limited regime along the entire tuning range. The features of the supply current peaks coincide with the positive and negative peaks of the output voltage and thus vary at $2\omega_0$. The average supply current is about 4.4 mA.
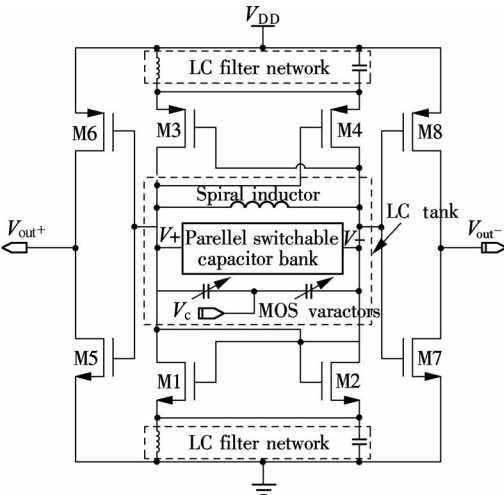

Fig. 2　Schematic of the proposed VCO

1. 2　Pulse swallow frequency divider

The architecture of the PSFD is shown in Fig. 3. The programmable PSFD includes a divided-by-32/33 dual-modulus prescaler (DMP), a 5-bit programmable swallow counter (SC), an 11-bit programmable counter (PC), and a control circuit (CC). The frequency division ratio of the DMP is controlled by the modulus control (MC) signal. The frequency division ratio of the SC and PC are changed by initially-set values of P and S ($P > S$). The CC controls the time sequence of the SC and PC and the modulus control (MC) signal through the swallow counter and the programmable counter.
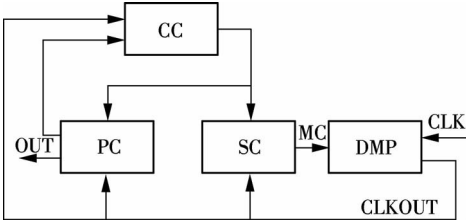

Fig. 3　Architecture of the PSFD

The DMP divides the VCO clock S times in $(32+1)$ mode, and $(P-S)$ times in (32) mode. The total division factor of the divider is $N = 33S + 32(P-S) = 32P + S$. The programmable counter with P values is between 32 and 4 095; the swallow counter with S values is between 0 and 31. So, when the synthesizer is locked, the output frequency of the VCO is: $f_{osc} = (32P + S)f_{ref}$, where f_{ref} is the frequency of a reference signal. The frequency of the VCO output may contain 64 512 frequency points such as $1\,024f_{ref}$, $1\,025f_{ref}$, …, or $65\,536f_{ref}$, according to the values of S and P.

To improve the performance, three types of DFF, i. e. SCL, TSPC and CMOS static flip-flops, are employed in the DMP[8]. Among of them the SCL is applied in the synchronous divided-by-4/5 counter since it can work at a higher speed, a wide band and an appropriate power consumption. A TPSC (true-single-phase-clock)[9] and two CMOS static flip-flops are applied in the asynchronous divided-by-8 counter; since the TSPC can work at a high speed and a low power consumption and a CMOS static flip-flop circuit structure, it can assure a good noise performance and keep a better interface with the next part simultaneously.

The SC consists of three blocks: a 5-bit programmable counter, a combination-logic circuit and a sample latch. The programmable counter is based on a chain of a 5-bit asynchronous preset static-logic divided-by-2 divider. The CLK signal of the SC is provided by the output signal of the proposed DMP. The input signals of the NOR gate are the output signals of all divided-by-2 dividers in the SC and the output signal of the NOR gate is the MC signal of the proposed DMP.

The PC consists of an 11-bit programmable counter, several combination circuits, and a latch. The programmable counter is based on a chain of 11-bit asynchronous preset static-logic divided-by-2 divider. Other circuits contain two NOR gates of three input ports, two NOR gates of four input ports, two NAND gates of three input ports, a NOT gate, and a latch. The CLK signal of the PC is provided by the output signal of the proposed DMP. The output signal is the final output of the proposal programmable PSFD.

1.3　Multi-mode frequency divider

In order to convert the output signals of the VCO to LO quadrature signals as shown in Tab. 1, a novel MMFD is given, and the architecture of the MMFD is shown in Fig. 4. The MMFD includes a divided-by-5/6/7/8 divider, a divided-by-4/3/2/0.5 divider, a divided-by-4 divider, and a mode control circuit.

Tab. 1　The frequency of 12 bands

| Band	LO quadrature signals/MHz	f_{VCO}/MHz
LF	35.600 5 to 35.735 5	2 848 to 2 858.8
MF	35.977 to 37.162	2 878.2 to 2 973
HF_ I	37.732 to 41.66	2 718 to 3 000
HF_ II	41.66 to 46.87	2 666.2 to 3 000
HF_ III	46.87 to 53.57	2 624.7 to 3 000
HF_ IV	53.57 to 62.452	2 571.4 to 3 000
FM_ I	111.452 to 125	2 674.8 to 3 000
FM_ II	125 to 143.452	2 500 to 2 869
III _ I	209.452 to 214.28	2 932.3 to 3 000
III _ II	214.28 to 250	2 571.4 to 3 000
III _ III	250 to 275.452	2 500 to 2 754.5
L	1 487.452 to 1 572.452	2 975 to 3 055
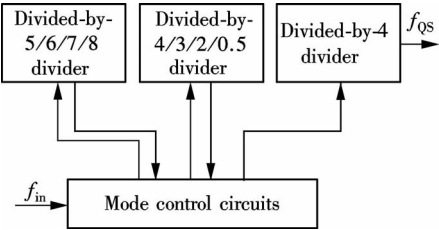
Fig. 4　Architecture of the MMFD

According to the tuning words of the system, the mode control circuits control the modes of the divided-by-5/6/7/8 divider and the divided-by-4/3/2/0.5 divider to choose a band. Finally, the synchronization 4 frequency divider is to generate the LO quadrature signals.

2　Measured Results

The chip of the frequency synthesizer is fabricated in a SMIC's 0.18-μm RF CMOS process. The chip photograph is shown in Fig. 5. Its area is 1 425 μm × 795 μm, including pads and test circuits.

2.1　Measured results of voltage-control oscillator

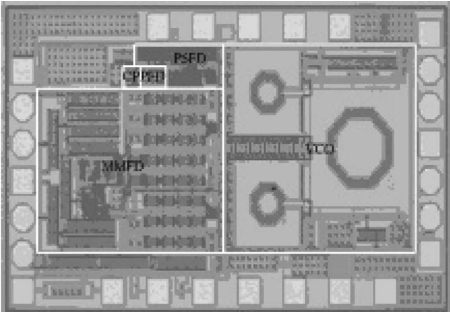The f-V curve of the proposed VCO is measured as a

Fig. 5　Chip photograph of proposal frequency synthesizer

function of the control codes of the parallel switchable capacitor bank. The results are shown in Fig. 6. The measured results show that its tuning range is 44.6% from 2.27 to 3.57 GHz, and its core power consumption is 6.16 mW under a 1.8 V power supply.
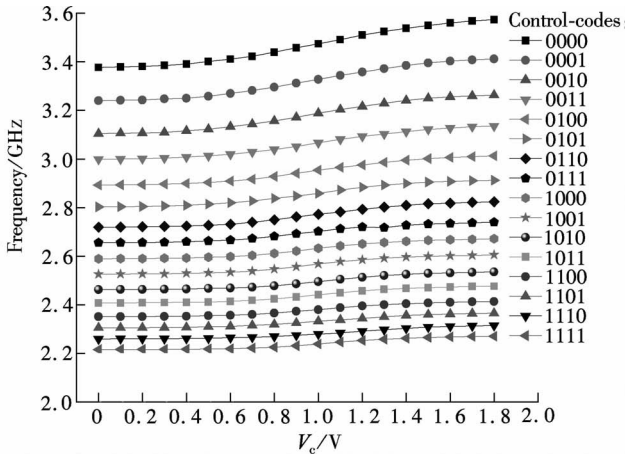

Fig. 6　Measured f-V curve of the proposal VCO

The phase noise is measured by using an Agilent E4440A spectrum analyzer. To measure the phase noise, the control voltage is 1.4 V and the control-code is "0001". The oscillation frequency is 3.385 GHz. The phase noise of the output is measured to be 120.22 dBc/Hz at 1 MHz offset from the carrier as shown in Fig. 7. The FoM [10] of the proposed VCO is 182.6.
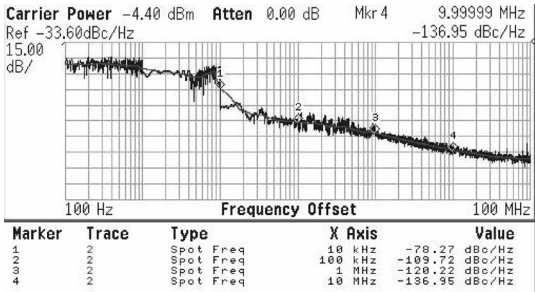

Fig. 7　Measured phase noise of proposal VCO

2.2　Measured results of pulse swallow frequency divider

When the frequency of the input signal is 2.958 4 GHz and the frequency division ratio is 36 980, the proposed

programmable PSFD works at the MF band and the output signal is 80 kHz. The measured result is shown in Fig. 8.
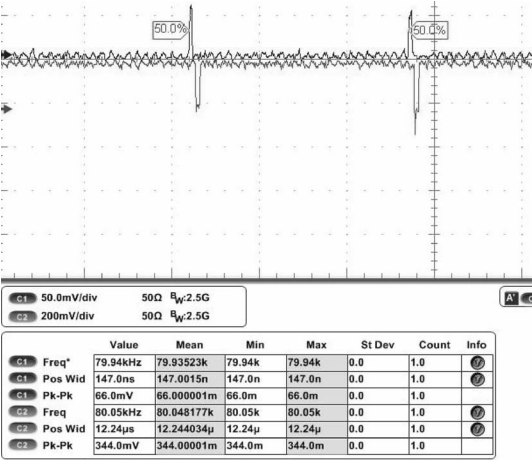

Fig. 8   Measured result in MF band

When the input voltage is minimum and the reliable operation of the above PSFD is guaranteed, the measured minimum input sensitivity V_{PP} vs. the input frequency of the PSFD is plotted in Fig. 9. The minimum input voltage of the frequency dividers is less than 0. 95 V in the frequency range of 0. 9 to 3. 4 GHz. The minimum input signal peak, for the PSFD working at 3. 4 and 0. 9 GHz are 0. 95 and 0. 59 V, respectively.
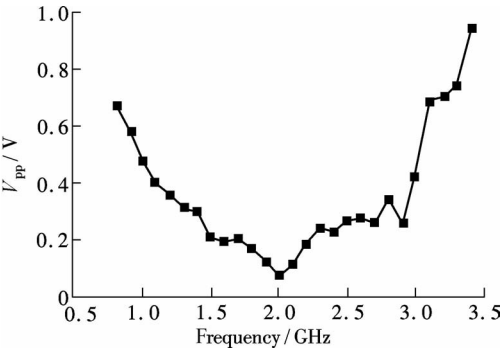

Fig. 9   Sensitivity measured from proposal PSFD

2. 3   Measured results of multi-mode frequency divider

When the frequency division ratio is 32, the measured phase errors of LO quadrature signals are less than 3°, as shown in Fig. 10.

2. 4   Measured results of frequency synthesizer

When the frequency of the reference signal is 240 kHz and the frequency division ratio is 12 134, the phase noise of the output is measured to be $-59. 52$ dBc/Hz at 10 kHz offset from the carrier as shown in Fig. 11.

3   Conclusion

In this paper, a frequency synthesizer for DRM/DAB/AM/FM RF front-end is demonstrated in SMIC's
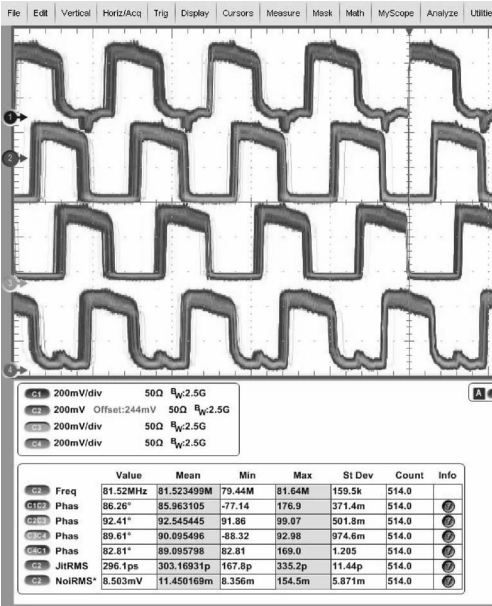

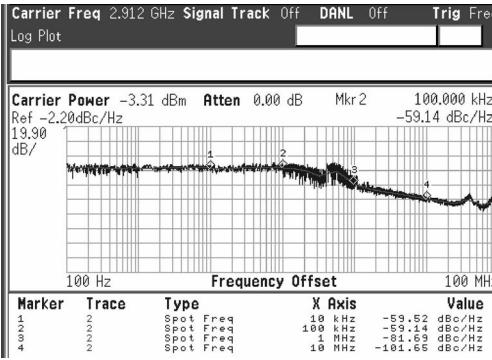**Fig. 10**   Output signals of multi-mode frequency divider

Fig. 11   Measured phase noise of proposal frequency synthesizer

0. 18-μm RF CMOS technology. The novel structure of the frequency synthesizer assures that one loop can cover the frequency range of 35. 600 5 to 1 572. 452 MHz and be compatible with the specification of radio standards of AM, FM, DRM and DAB. The measured results show that the performance of the frequency synthesizer meets the requirement of the DRM/DAB/AM/FM RF front-end.

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一种应用于 DRM/DAB/AM/FM 射频前端的频率综合器

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摘要:介绍了一种应用于宽带低相位噪声的频率综合器.此频率综合器为兼容 DRM,DAB,AM 和 FM 的射频前端提供本振信号.为了覆盖所有频段的信号,提出了一种新的频率规划和系统结构.此频率综合器包含宽带低功耗低相位噪声的 VCO 和高速宽带低功耗的大分频比吞吐脉冲分频器等模块.所设计的频率综合器应用中芯国际的 0.18 μm RF CMOS 工艺进行了流片实现.整个芯片面积为 1 425 μm × 795 μm,包括测试驱动电路和焊盘.测试结果表明,压控振荡器振荡频率范围为 2. 27 ~3. 57 GHz.在频偏为 1 MHz 时,其相位噪声为 120. 22 dBc/Hz;吐脉冲分频器的工作频率范围为 0. 9 ~3. 4 GHz;在频偏为 10 kHz 时,锁相环内的相位噪声为 −59. 52 dBc/Hz,完全满足 DRM/DAB/AM/FM 射频前端的要求.此频率综合器在 1. 8 V 的电源电压下,其功耗为 47 mW(包括测试驱动的功耗).

关键词:频率综合器；宽带压控振荡器；吞吐脉冲分频器；低相位噪声
中图分类号:TN752