

Novel lateral insulated gate bipolar transistor on SOI substrate for optimizing hot-carrier degradation

Huang Tingting Liu Siyang Sun Weifeng Zhang Chunwei

(National ASIC System Engineering Research Center, Southeast University, Nanjing 210096, China)

Abstract: A novel lateral insulated gate bipolar transistor on a silicon-on-insulator substrate (SOI-LIGBT) with a special low-doped P-well structure is proposed. The P-well structure is added to attach the P-body under the channel, so as to reduce the linear anode current degradation without additional process. The influence of the length and depth of the P-well on the hot-carrier (HC) reliability of the SOI-LIGBT is studied. With the increase in the length of the P-well, the perpendicular electric field peak and the impact ionization peak diminish, resulting in the reduction of the hot-carrier degradation. In addition, the impact ionization will be weakened with the increase in the depth of the P-well, which also makes the hot-carrier degradation decrease. Considering the effect of the low-doped P-well and the process windows, the length and depth of the P-well are both chosen as 2 μm .

Key words: lateral insulated gate bipolar transistor (LIGBT); silicon-on-insulator (SOI); hot-carrier effect (HCE); optimization

doi: 10.3969/j.issn.1003-7985.2014.01.004

The lateral insulated gate bipolar transistor (LIGBT) is the suitable device for the power integrated circuits (ICs) due to its capability of handling high voltage and heavy current and its compatibility with the standard CMOS process. The silicon on insulator (SOI) substrate can offer true dielectric isolation for power devices, which eases the integration of power devices and low voltage logic devices in power ICs. As a result, the SOI-LIGBT begins to be a promising device for power applications.

One typical application of the SOI-LIGBT (M1) is used as the high-voltage output stage in the plasma display panels (PDP) scan driver ICs^[1-5]. During the working conditions, M1 will suffer from high voltage at “off-state” and heavy current at “on-state”. Therefore, the

hot-carrier effect (HCE) becomes serious. So, the hot-carrier degradation of the SOI-LIGBT devices is one of the most important reliability issues in ICs.

The HC reliability of the SOI-LIGBT devices is becoming more and more important, but the in-depth study on the hot-carrier degradation mechanism of the SOI-LIGBT devices is less documented due to the complexity of its two kinds of carriers. Recently, to our knowledge, no studies have been focused on the structure optimization of these devices to decrease the hot-carrier degradation^[6-8].

In this paper, to reduce the electric field and the degradation of the electrical parameters, a novel SOI-LIGBT is proposed with a low-doped p-type well (P-well) attached to the P-body under the channel region. It can be compatible with low-voltage CMOS processes completely without any additional mask. The length and depth of the P-well are varied and their effects on the degradation are investigated by using the T-CAD simulator and the charge pumping (CP) technique, which well support the experimental findings.

1 Device Structure and Experiment

The schematic cross section of the investigated SOI-LIGBT device in this paper is shown in Fig. 1(a), and the fabrication of the device is implemented in the 0.5 μm complementary MOS technology and the SOI technology. The structural parameters are given as follows: the length of the polygate is 5 μm ; the accumulation region length is 2 μm ; the buried oxide thickness is 1.5 μm ; the thickness of the silicon film above the buried oxide is 6.5 μm . The threshold voltage and the off-state BV are 1.1 V and 230 V, respectively. The special P-well structure is added to attach the P-body under the channel so as to reduce the hot-carrier-induced degradation. Moreover, it is noted that the concentration of the proposed P-well is much lower than that of the P-body. The concentration of the proposed P-well is $3 \times 10^{12} \text{ cm}^{-2}$. The SEM image of the cathode region in the improved SOI-LIGBT can also be seen in Fig. 1(b). The length L and depth D of the low-doped P-well are varied to obtain their effects on the hot-carrier degradation.

2 Discussions and Optimization

2.1 Experiment

The current in the SOI-LIGBT is composed of the electron

Received 2013-08-06.

Biographies: Huang Tingting (1988—), female, graduate; Sun Weifeng (corresponding author), male, doctor, professor, swffrog@seu.edu.cn.

Foundation items: The National Natural Science Foundation of China (No. 61204083), the Natural Science Foundation of Jiangsu Province (No. BK2011059), the Program for New Century Excellent Talents in University (No. NCET-10-0331).

Citation: Huang Tingting, Liu Siyang, Sun Weifeng, et al. Novel lateral insulated gate bipolar transistor on SOI substrate for optimizing hot-carrier degradation[J]. Journal of Southeast University (English Edition), 2014, 30(1): 17–21. [doi: 10.3969/j.issn.1003-7985.2014.01.004]

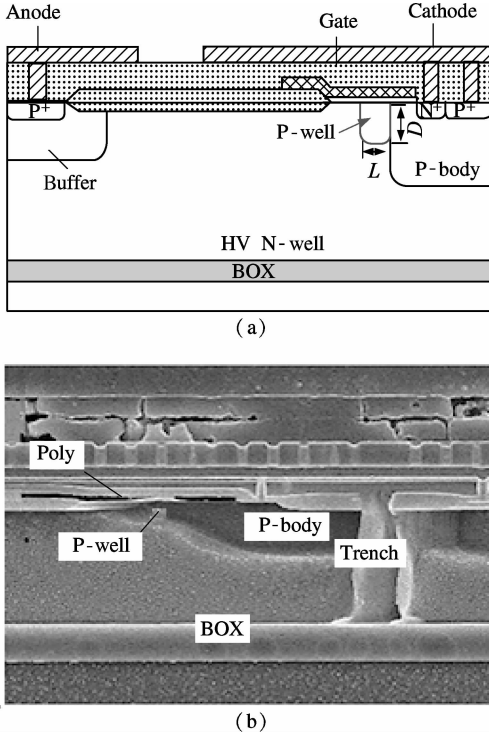


Fig. 1 Schematic diagram of the proposed SOI-LIGBT device. (a) Schematic cross section; (b) SEM image of the cathode region in the proposed device

current along the surface of the device and the hole current in the body of the silicon film above the buried oxide. The hole current is collected by the P^+ of the cathode, so the hole carriers generated from the impact ionization will be submerged into the large operation current of the SOI-LIGBT. Hence, the hole carriers cannot be detected. Therefore, the maximum substrate current cannot reflect the degradation level of the SOI-LIGBT device^[9]. In this paper, the hot-carrier stress condition of $V_{gc} = 2.5$ V and $V_{ac} = 165$ V is selected at the maximum substrate current of the SOI-LDMOS device, which fully owns the same structures except for the doping type in the anode area compared with the novel SOI-LIGBT. During the experiments, I_{alin} (measured at $V_{gc} = 5$ V and $V_{ac} = 1$ V) is monitored continuously to analyze the physical degradation. All the measurements in our experiments are performed at room temperature.

Before the hot-carrier degradation of the novel SOI-LIGBT is discussed, the influence of the added P-well on the electrical parameters of the SOI-LIGBT, such as the on-resistance, must be considered carefully. Actually, when the high gate operation voltage (7.8 V) is applied, the resistance of the P-well region will be much smaller than that of the added P-body region due to much more induced electron. Furthermore, it is the resistance of the HVN-well that will dominate the whole resistance of the device due to the long distance and the low doping. Therefore, the resistance of the added P-well region can be ignored compared with that of the P-body region and

the HVN-well region. That is to say, the added P-well will not obviously impact the whole resistance of the device. The measured I - V characteristics of the novel SOI-LIGBT and the conventional one under $V_{gc} = 7.8$ V are shown in Fig. 2. There is a little difference between them. And the key parameters of the two devices are shown in Tab. 1.

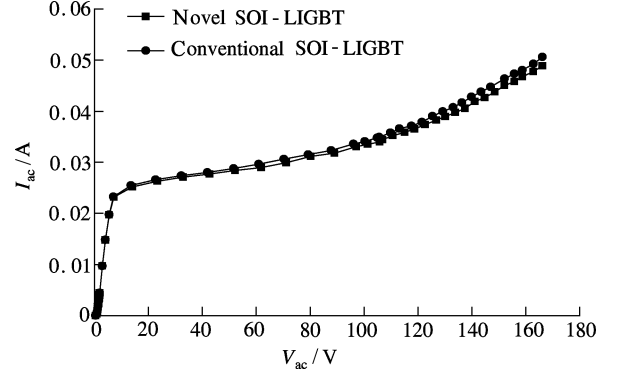


Fig. 2 I - V characteristics of novel SOI-LIGBT and conventional one

Tab. 1 Key parameters of novel SOI-LIGBT and conventional one

Device	I_{dsat}/mA	R_{on}/Ω	V_{th}/V	V_b/V	Degradation after 1 000 s/%
Conventional SOI-LIGBT	45.7	1 295	1.1	215	4.55
Novel SOI-LIGBT	44.3	1 297	1.1	230	1.66

Fig. 3 shows the parameter variations of the SOI-LIGBT devices under the stress of $V_{gc} = 2.5$ V and $V_{ac} = 165$ V. It is noted that there is almost no V_{th} shift, implying that no hot carriers inject into the channel region. The I_{alin} increases with the increase in the stress time, which reveals that there are many hot holes injecting into the bird's beak^[10] and the degradation is serious. It can also be found that the low-doped P-well can relax the increasing tendency of the I_{alin} and the hot carrier degradation. The longer and deeper the low doped P-well, the smaller the I_{alin} degradation will be.

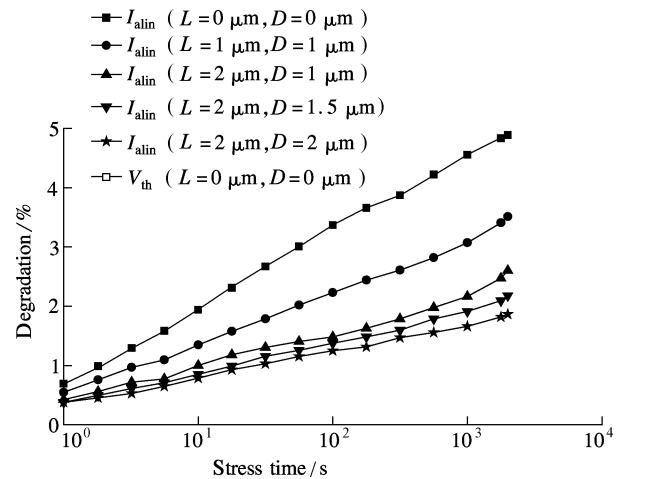


Fig. 3 I_{alin} and V_{th} degradation of the SOI-LIGBT devices with different L and D

2.2 Influence of L

In order to understand the above experimental results, The T-CAD simulations about the perpendicular electric field and the impact ionization are performed. Fig. 4 and Fig. 5 show the perpendicular electric field and the impact ionization along the Si/SiO₂ interface for the SOI-LIGBT with different L and $D = 1 \mu\text{m}$ at $V_{\text{gc}} = 2.5 \text{ V}$ and $V_{\text{ac}} = 165 \text{ V}$. The first perpendicular electric field peak in the bird's beak is negative (pointing to the oxide), which is helpful for the hot-hole injection, and the second perpendicular electric field peak in the channel region is positive, which is beneficial for the hot-electron injection. However, the impact ionization is mainly located in the bird's beak and no obvious impact ionization can be observed in the channel region. As a result, a great amount of hot holes will be injected and trapped into the bird's beak, resulting in the increase of I_{ain} due to the mirror induced negative charges. Less V_{th} shift can be discovered due to no hot-electron injection in the channel region. In addition, according to Figs. 4 and 5, it is observed that the increase of the length of the low-doped P-well will decrease the perpendicular electric field and the impact ionization in the bird's beak. As a result, the hot-hole injection into the bird's beak is diminished, and the I_{ain} degradation turns much smaller.

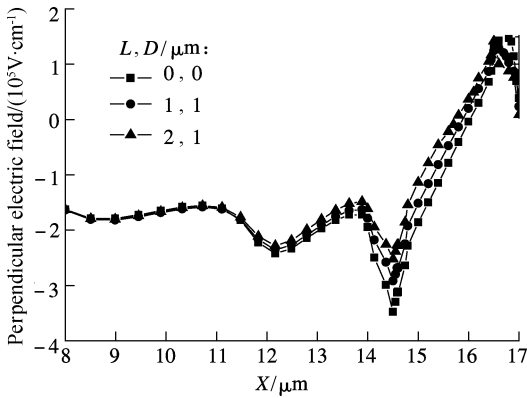


Fig. 4 Surface perpendicular fields with different L and $D = 1 \mu\text{m}$ at $V_{\text{gc}} = 2.5 \text{ V}$ and $V_{\text{ac}} = 165 \text{ V}$

According to the influence of L on the electric field and the impact ionization, one can know that the hot-hole injection and trapping into the bird's beak can be reduced effectively by adjusting the dimension of L . Although it is useful to increase L for hot carrier reliability, the dimension of L cannot be greater than $2 \mu\text{m}$ in this case. Otherwise, it will exceed the accumulation region and lead to the abnormal threshold voltage, making the operation of the SOI-LIGBT abnormal. Considering the effect of the low-doped P-well and the process windows, we choose L as $2 \mu\text{m}$ here. In this way, the hot carrier degradation of the SOI-LIGBT can be relaxed and its reliability can be optimized.

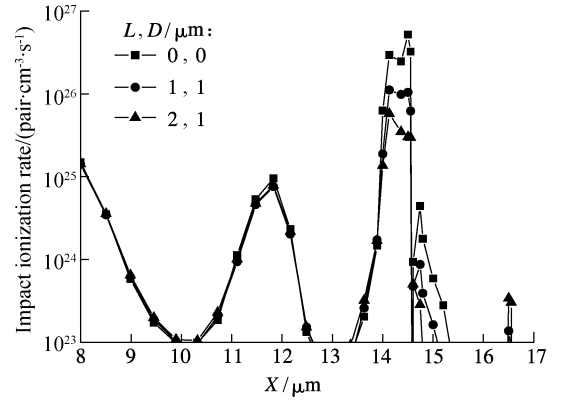


Fig. 5 Surface impact ionization with different L and $D = 1 \mu\text{m}$ at $V_{\text{gc}} = 2.5 \text{ V}$ and $V_{\text{ac}} = 165 \text{ V}$

2.3 Influence of D

The influence of the depth of the low doped P-well on the impact ionization, which reveals the hot carrier degradation, is also simulated and compared in this paper. Fig. 6 shows the 2D impact ionization of the proposed SOI-LIGBT with different D and an L of $2 \mu\text{m}$ at $V_{\text{gc}} = 2.5 \text{ V}$ and $V_{\text{ac}} = 165 \text{ V}$. It is clear that the increase of the depth of the low doped P-well will decrease the impact ionization of the device, leading to the reduction of the

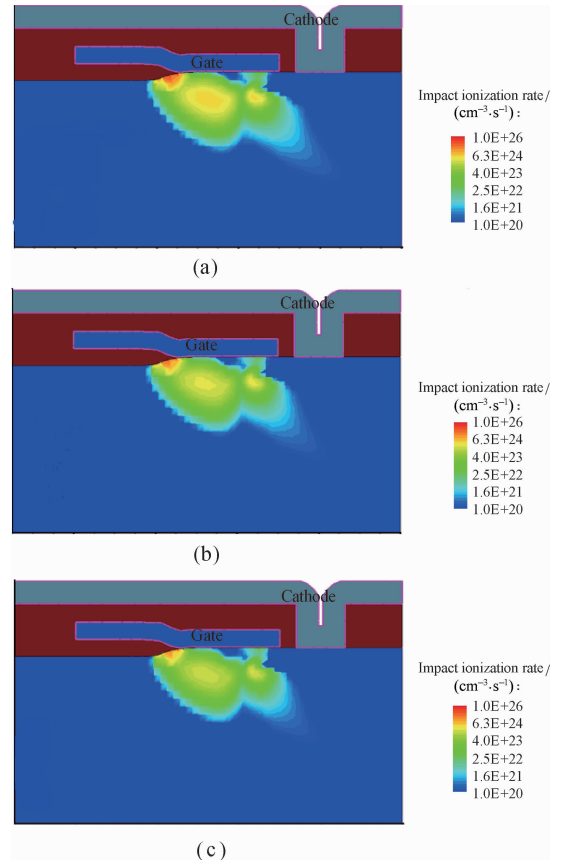


Fig. 6 2D impact ionization of the proposed SOI-LIGBT with different D at $V_{\text{gc}} = 2.5 \text{ V}$ and $V_{\text{ac}} = 165 \text{ V}$. (a) $D = 1 \mu\text{m}$ and $L = 2 \mu\text{m}$; (b) $D = 1.5 \mu\text{m}$ and $L = 2 \mu\text{m}$; (c) $D = 2 \mu\text{m}$ and $L = 2 \mu\text{m}$

hot carrier degradation. However, for the same L , the value of D cannot be too large. The reason is that during the production processes, the longtime annealing is used to obtain deep D , but at the same time it affects the value of L . The longer the annealing time, the larger L and D will be. The value of L cannot be too large since the depth of the low doped P-well is limited. In this paper, the value of D is chosen as $2\ \mu\text{m}$.

2.4 Charge pumping

In order to have a further understanding of the hot-carrier degradation of the SOI-LIGBT, the charge pumping (CP) technique is performed. The CP measurements are performed with the constant gate voltage pulse, whose amplitude and frequency are 10 V and 1 MHz, respectively. The base voltage V_{base} of the pulse is varied from -15 to 5 V. The rising and falling time of the pulse are both 100 ns. The anode and cathode are grounded. The CP current I_{cp} is measured from the substrate to reveal the hot-carrier trapping and the interface state generation. At the same time, the V_{ge} and V_{gh} (defined as the gate voltage to induce $1 \times 10^{14}\text{ cm}^{-3}$ electrons and holes, respectively) profiles of the SOI-LIGBT are shown in Fig. 7 by using the T-CAD simulations. According to Fig. 7, I_{cp} can be divided into three regions: the channel region (corresponding V_{base} from -5.5 ($V_{\text{ge}} - V_{\text{amplitude}}$) to 0 V (V_{gh}) for the unstressed device), the accumulation region (corresponding V_{base} from -7.5 to -5 V for the unstressed device) and the field oxide region (corresponding V_{base} from -10 to -7.5 V for the unstressed device)^[11–12]. The I_{cp} curves of the conventional and proposed SOI-LIGBT ($L=2\ \mu\text{m}$ and $D=2\ \mu\text{m}$) are measured and shown in Fig. 8. The stress condition is $V_{\text{gc}}=2.5$ V and $V_{\text{ac}}=165$ V for 2 000 s. Comparing the I_{cp} before and after the stress of the conventional device, it is clear that the I_{cp} curves shift left (change A), reflecting the hot hole injection into the bird's beak. And the change of the value of I_{cp} (change B) indicates the interface state generation in the channel region, the accumulation region and the field oxide region. Moreover, it is also noted that the change A and change B of the proposed device are smaller than

those of the conventional device after stress. That is to say, the hot-hole injection is restrained and the interface state generation is decreased in the proposed device. So the hot-carrier degradation for the SOI-LIGBT with the low-doped P-well is reduced.

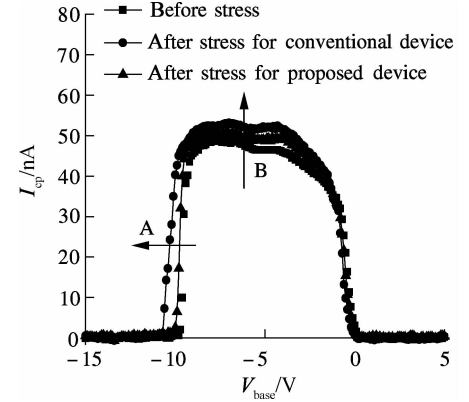


Fig. 8 CP curves of the conventional and proposed devices before and after stress

3 Conclusion

A special P-well structure is added to attach the P-body under the channel in the SOI-LIGBT devices to reduce the I_{alin} degradation without any additional mask. The special P-well is shown completely compatible with the low-voltage CMOS processes and does not impact the key parameters of the device. The influence of the length and depth of low doped P-well is studied in detail for the high-voltage SOI-LIGBT. With the increase of L , the perpendicular electric field peak and the impact ionization peak diminish, resulting in the reduction of the hot carrier degradation. In addition, the impact ionization will be weakened with the increase in the depth of the low-doped P-well, which also makes the hot-carrier degradation decrease. Therefore, considering the effect of the low-doped P-well and the process windows, $2\ \mu\text{m}$ is chosen for the length and depth of the P-well.

References

- [1] Chen W S, Xie G, Zhang B, et al. New lateral IGBT with controlled anode on SOI substrate for PDP scan driver IC [C]//*International Conference on Communications, Circuits and Systems*. Milpitas, CA, USA, 2009: 628–630.
- [2] Sumida H, Hirabayashi A, Kobayashi H. A high-voltage lateral IGBT with significantly improved ON-state characteristics on SOI for an advanced PDP scan driver IC [C]//*IEEE International SOI Conference Proceedings*. Williamsburg, VA, USA, 2002: 64–65.
- [3] Qiao M, Zhang B, Xiao Z Q, et al. High-voltage technology based on thin layer SOI for driving plasma display panels [C]//*International Symposium on Power Semiconductor Devices and ICs*. Orlando, FL, USA, 2008: 52–55.
- [4] Sun W F, Shi L X, Sun Z L, et al. High-voltage power

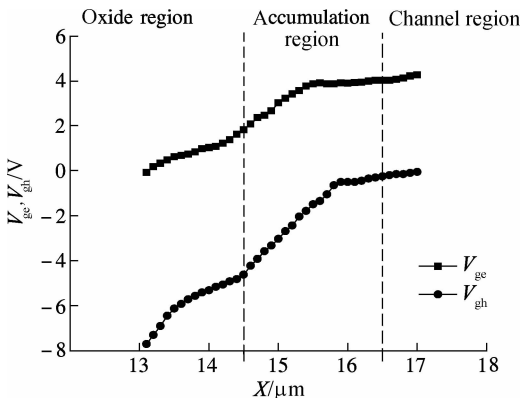


Fig. 7 V_{ge} and V_{gh} profiles of the SOI-LIGBT

- IC technology with nVDMOS, RESURF pLDMOS, and novel level-shift circuit for PDP scan-driver IC [J]. *IEEE Transactions on Electron Devices*, 2006, **53**(4): 891 – 896.
- [5] Tokumitsu S, Nitta T, Shiromoto T, et al. Enhancement of current drivability in field PMOS by optimized field plate [C]//*International Symposium on Power Semiconductor Devices and ICs*. Hiroshima, Japan, 2010: 253 – 256.
- [6] Wu H, Sun W F, Yi Y B, et al. Study and optimization of hot-carrier degradation in high voltage pldmos transistor with thick gate oxide [C]//*International Symposium on the Physical and Failure Analysis of Integrated Circuits*. Suzhou, China, 2009: 83 – 86.
- [7] Bakeroot B, Doutreligne J, Moens P. A new substrate current free nLIGBT for junction isolated technologies [C]//*European Solid-State Device Research Conference*. Leuven, Belgium, 2004: 461 – 464.
- [8] Lu D H, Mizushima T, Kitamura A, et al. Retrograded channel SOI LIGBTs with enhanced safe operating area [C]//*International Symposium on Power Semiconductor Devices and ICs*. Orlando, FL, USA, 2008: 32 – 35.
- [9] Liu Siyang, Sun Weifeng, Qian Qinsong, et al. Comparisons of hot-carrier degradation behavior in SOI-LIGBT and SOI-LDMOS with different stress conditions [J]. *Solid-State Electronics*, 2010, **54**(12): 1598 – 1601.
- [10] Qian Q S, Sun W F, Liu S Y, et al. Novel hot-carrier degradation mechanisms in the lateral insulated-gate bipolar transistor on SOI substrate [J]. *IEEE Transactions on Electron Devices*, 2011, **58**(4): 1158 – 1163.
- [11] Moens P, Van Den Bosch G, Wojciechowski D, et al. Charge trapping effects and interface state generation in a 40 V lateral resurf pDMOS transistor [C]//*European Solid-State Device Research Conference*. Grenoble, France, 2005: 407 – 410.
- [12] Heremans P, Witters J, Groeseneken G, et al. Analysis of the charge pumping technique and its applications for the evaluation of MOSFET degradation [J]. *IEEE Transactions on Electron Devices*, 1989, **36**(7): 1318 – 1335.

一种新型优化热载流子退化效应的 SOI-LIGBT

黄婷婷 刘斯扬 孙伟锋 张春伟

(东南大学国家 ASIC 系统工程技术研究中心, 南京 210096)

摘要:提出了一种新型绝缘体上硅横向绝缘栅双极型晶体管(SOI-LIGBT),该晶体管在沟道下方的P型体区旁增加了一个特殊的低掺杂P型阱区,在不增加额外工艺的基础上减小了器件线性区电流的退化.分析了低掺杂P阱的宽度和深度对SOI-LIGBT器件热载流子可靠性的影响.通过增加低掺杂P型阱区的宽度,可以减小器件的纵向电场峰值和碰撞电离峰值,从而优化器件的热载流子效应.另外,增加低掺杂P型阱区的深度,也会减小器件内部的碰撞电离率,从而减弱器件的热载流子退化.结合低掺杂P型阱区的作用和工艺窗口大小的影响,确定低掺杂P型阱区的宽度和深度都为2 μm .

关键词:绝缘栅双极型晶体管;绝缘体上硅;热载流子效应;优化

中图分类号:TN432