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Design and implementation of GM-APD array readout circuit for infrared imaging

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Abstract: Based on an avalanche photodiode (APD) detecting array working in Geiger mode (GM-APD), a high-performance infrared sensor readout integrated circuit (ROIC) used for infrared 3D (three-dimensional) imaging is proposed. The system mainly consists of three functional modules, including active quenching circuit (AQC), time-to-digital converter (TDC) circuit and other timing controller circuit. Each AQC and TDC circuit together constitutes the pixel circuit. Under the cooperation with other modules, the current signal generated by the GM-APD sensor is detected by the AQC, and the photon time-of-flight (TOF) is measured and converted to a digital signal output to achieve a better noise suppression and a higher detection sensitivity by the TDC. The ROIC circuit is fabricated by the CSMC 0.5 μm standard CMOS technology. The array size is 8 × 8, and the center distance of two adjacent cells is 100 μm. The measurement results of the chip show that the performance of the circuit is good, and the chip can achieve 1 ns time resolution with a 250 MHz reference clock, and the circuit can be used in the array structure of the infrared detection system or focal plane array (FPA).

Key words: infrared 3D (three-dimensional) imaging; readout integrated circuit (ROIC); Geiger mode avalanche photodiode; active quenching circuit (AQC); time-to-digital converter (TDC)

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Single-photon avalanche photodiode (SPAD) can detect and count the single-photon incident, which can be used in laser ranging and 3D imaging in an extremely low light environment[1]. According to different relative relationships between reverse bias voltage and avalanche breakdown voltage, APD can be divided into Geiger mode APD and linear mode APD. When the APD avalanche breakdown voltage is higher than the reverse bias voltage, it is said to be a Geiger mode APD[2].

Traditional laser radar systems mechanically scan a photon detector resulting in the limitation of the data acquisition rate. With the plane array GM-APD detector, the new laser radar measures the round-trip time of the photon passively, and a 3D laser imaging can thus be obtained with a single laser pulse and no scanning is necessary[3].

For the current mature infrared detection technology, it is not the detector but the readout integrated circuit that limits its performance. There are several basic requirements for the infrared readout circuit: high data acquisition accuracy and intensity, low crosstalk noise, a wide dynamic range, low power consumption, good control of the infrared detector bias, large array size and a small center distance. As the signal transmission interface between the sensor and the 3D imaging system, the infrared readout circuit has become one of the most key technologies of the whole 3D imaging system.

The current mainstream ROIC includes analog ROIC and digital ROIC. The analog readout circuit is used for the infrared focal plane array (FPA) passive imaging system[4]. It converts the optical signal of target radiation detected by the infrared sensor into an analog voltage signal output, which then is used for the subsequent circuit to complete digital signal processing by the ADC conversion. The digital ROIC is used for the scannerless active imaging systems of the Geiger mode detector array. The laser launch system implements active exposure for the objective of detection, and then the pulsed laser signal reflected by the target is detected by the GM-APD detector, and directly converted into a digital output signal for subsequent digital signal processing circuits.

Based on the InGaAs-APD array detector[5], a digital GM-APD array infrared readout integrated circuit is designed. The ROIC has the characteristics of effective noise suppression, high detection sensitivity and low noise. The size of the two-dimensional array is 8 × 8; the operating voltage is 5 V, and the center distance of the two adjacent cells is 100 μm. The proposed ROIC is taped out and verified based on the CSMC 0.5 μm standard CMOS process, and it can be integrated into the 8 × 8 InGaAs-APD sensor array based on hybrid-package technology.

1 Working Principle of the APD Detection

1.1 APD detection principle

The APD array detector in a broad sense is composed

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of a Geiger-mode APD and a CMOS timing circuit. When the system is operating, the laser emits laser signals, and the CMOS timing circuit works at the same time. When the GM-APD receives the light reflected by the target, APD will generate a large current pulse due to the avalanche triggering effect. After the corresponding circuit is processing, the current pulse is converted into a digital voltage pulse signal APD-STOP that can directly trigger the frame frequency type CMOS timing circuit, and then causes the CMOS timing circuit to stop counting. The process needs no ADC conversion. Thus, under the trigger of the digital voltage pulse, the time information of TOF is registered in the register set in each pixel.

1.2 System timing

Aimed at the 3D imaging application of infrared distance measurement, the integrated array ROIC should have the ability to continuously process sensed signals according to the frame frequency timing. Therefore, a frame rate type of 8×8 array ROIC is designed in this paper. Fig. 1 shows the timing diagram of ROIC key signals within a frame time.

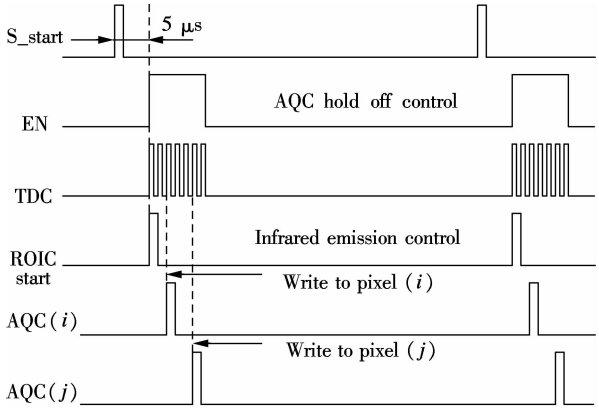


Fig. 1 Timing diagram of ROIC system

The timing diagram shows the timing of the ROIC system. At the beginning of each frame, AQC circuit sets APD in the Geiger mode, and the signal S_start activates the laser emission while TDC starts counting. When APD detects photons, the interface circuit generates a STOP signal, causing TDC to stop counting, and then the AQC circuit is quenched, making the APD exit from the detection mode. The detected data is read out in a serial transmission mode under the low frequency clock. The maximum duty cycle of APD which is biased on the Geiger mode in a frame is about 1%, which not only ensures that the APD works stably and reliably, but also is helpful in reducing the power consumption of the system.

2 Design of ROIC

In the early stages of the study, the Lincoln Laboratory proposed a classic pixel cell circuit structure[6]. Considering the factors in practical applications, technology and other aspects, a frame rate type of array ROIC suitable for 3D imaging applications is proposed. The design draws on the advantages of the classic pixel cell circuit in the Lincoln Laboratory. The DFF of the counting module and the AQC detecting circuit are improved. With the corresponding peripheral control circuits, the design of GM-ROIC 8×8 array is completed.

Fig. 2 shows the overall structure diagram of the frame rate type array ROIC based on GM-APD, which is comprised an array of 8×8 pixels, the timing control circuit, and data readout circuit, etc. In the design process, taking into account the influence caused by the transmission delay of signals and the clock skew in a high speed large array detection circuit, the demand of signal transmission consistency in the array circuit is high, and a multi-stage H tree structure is introduced to transfer clock signals and control signals. Furthermore, the output data of each row of pixels is transferred in parallel, the output data of pixels in each row is sent serially to the data output interface circuit, and then the parallel data is converted into serial data through the data output interface circuit.

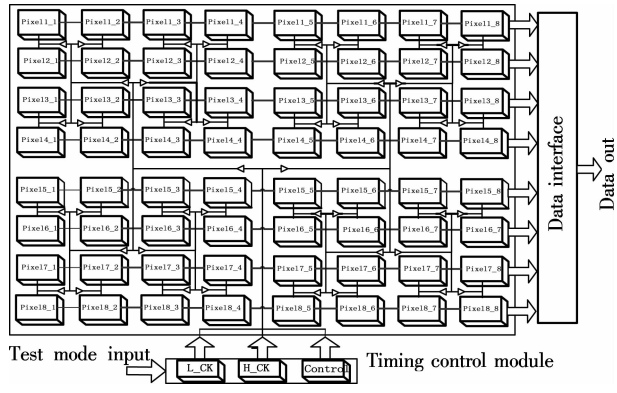


Fig. 2 Structure diagram of ROIC

An 8×8 array is composed of 64 identical pixel cells, and each pixel cell circuit is composed of a photon detection circuit and a pixel-level TDC circuit. The circuit configuration of each pixel is shown in Fig. 3.

The photon detection circuit mainly consists of Geiger mode avalanche photoelectric sensors and the AQC module. In the Geiger mode, the p-side of the APD is biased towards a negative voltage whose magnitude is just below the avalanche breakdown, and the assertion of the ARM signal causes the n-side of the APD to be pulled up to +5 V, thereby those bias volts are above the breakdown voltage. When a photon is detected by an APD, the resulting avalanche discharges it to the breakdown voltage, an event that is equivalent to a logical high-to-low transition, and then it generates a STOP signal. The assertion of the DISARM signal causes the n-side of each APD to be pulled down to 0 V, thereby turning the APD "off" and resetting the sensor.

The pixel level TDC circuit is mainly composed of

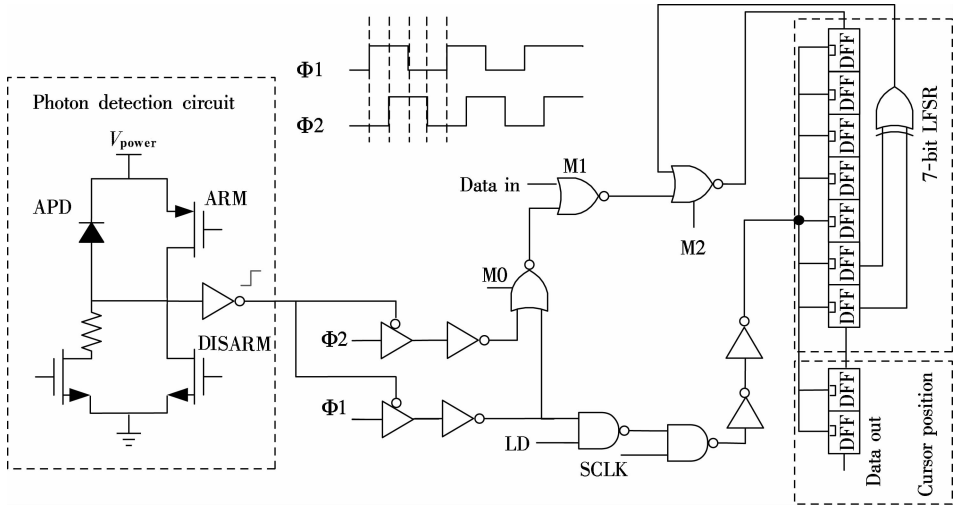


Fig. 3 The pixel unit circuit

a dual-mode 7-bit LFSR (pseudo-random counter), 2-bit cursor position and 2-to-1 multiplexer. Compared with traditional asynchronous counters, the time delay of the LFSR simply depends on the delay of a single logic gate. It can effectively improve the counting speed and reduce the chip areas. 2-bit cursor position and 2-to-1 multiplexer are used for choosing the counting and data transmission mode, which can measure the time interval of the host sending the START signal and APD inducting reflection photon, and the time interval is twice the time-of-flight (TOF) of the photon. TOF can be expressed as

$$T_{\text{meas}} = \left(N_{\text{coarse}} + \frac{N_{\text{fine}}}{4} \right) T_{\text{ck}}$$

where T_{ck} is the cycle of high frequency clock, and the design value is 2 to 4 ns; therefore, the minimum time resolution that the pixel-level TDC circuit can provide is $T_{\text{ck}}/4 = 1$ ns, and the range is 512 ns.

Using the 2-to-1 multiplexer to choose the time measurement mode or readout mode, the pixel-level TDC completes counting and data transmission. This structure is conducive to the compact design of the pixel circuit. The 2-bit cursor position ensures that ROIC can achieve 0.5 to 1 ns time resolution as a result of a 250 to 500 MHz counting clock.

The high-frequency clock circuit DLL outside the pixel generates a master clock Φ1 and a secondary clock Φ2; the clocks are all 250 MHz, and the phase shift between the two clocks is 90°. The timing function of the pixel is completed with the help of Φ1 and Φ2. Meanwhile, the low-frequency clock circuit generates the low frequency clock SCLK used for the data transmission.

3 ROIC Measurement and Verification

An 8 × 8 ROIC chip is fabricated using the CSMC 0.5 μm CMOS process. The chip photograph is shown in Fig. 4. The chip occupies an area of 2 mm × 2 mm, and the pixel area is 100 μm × 100 μm. The measurements show that the readout speed is 2 Mbit/s, and the maximum frame rate is 1 000 frame/s. The test operation temperature is at the room temperature under a 5 V supply voltage.

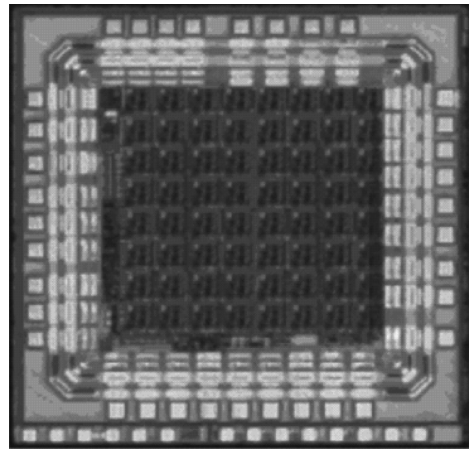
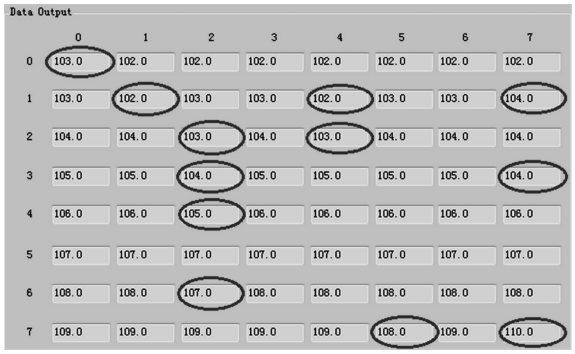
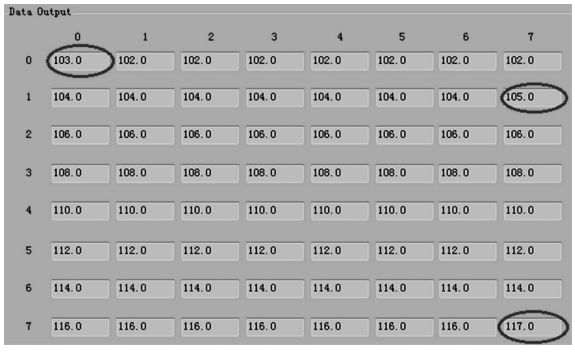


Fig. 4 Photograph of 8 × 8 ROIC chip

The ROIC readout circuit and sensor require hybrid packaging when working in practice. However, there is no external sensor in the testing chip, and the digital pulse signal generated by APD sensor is simulated by the external STOP signal. The flight time, from the moment when the photon is sent by the laser emission to the moment when the photon is reflected by the object and measured by APD, is simulated by the interval between the rising edge of EN and the external STOP signal. Each row of pixels in the chip of 8 × 8 shares one different external STOP testing signal to verify the time resolution, and the key control signals and the STOP signals are generated by FPGA, which can realize the precise set of the excitation signal. The test results under external STOP with 1 and 2 ns steps are shown in Figs. 5(a) and (b), and the annotation with the circle refers to the error pixels.



(a)



(b)

Fig. 5 Output data of chip under external STOP. (a) 1 ns step; (b) 2 ns step

As shown in Fig. 5, the ROIC chip works well and obtains the counting function. Compared the decoding results of pixels which are located in (00), (17), (77) in Figs. 5(a) and (b), the data of these three pixels is 1 ns greater than that of the same row; this is not error code, but the offset caused by process deviation during tape-out. Actually, it is the fixed error and absolute error of the system and has no effect on its relative accuracy and time resolution. Meanwhile, the data of the other pixels circled out in Fig. 5(a) is 1 ns smaller than the pre-defined pixel value, the unavoidable random errors mainly arise from the array clock skew, clock jitter, and the unconformity of the transmission delay. Generally, a time resolution of 1 ns can be achieved under 250 MHz, while the error code is relatively serious.

In order to make the testing results more accurate, the chip needs to be tested continuously. During the time period of 100 to 500 ns, different stop intervals such as 1, 10, 100 ns are applied. The output data are decoded and compared to analyze the degree of linearity, as shown in Fig. 6. It can be directly seen that the linearity of the chip is good.

Fig. 7 shows the analysis of absolute error and relative error of the two sets of data. It can be seen that there is deviation between the measurement and STOP set value. The absolute error of the system can be controlled within 3 ns, which is mainly caused by the transmission delay resulting from parasitic effects in the layout and wire. Inherent errors of the system cannot be eliminated, and they

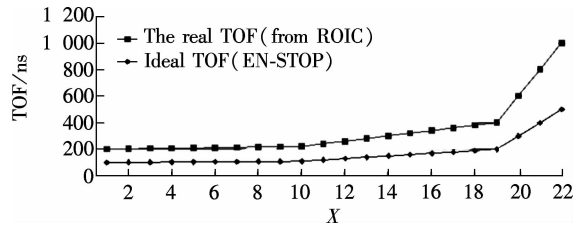


Fig. 6 Linearity analysis of chip's measurement data

have no effect on the relative accuracy as well as the precision of the 3D imaging. The index of relative error is more important in our design, as shown in Fig. 7. The relative error of our chip is small on the whole, but the relative error of some pixels is large. It belongs to system error, and it occurs when the edge of stop signal is too close to the rising edge of the DFF. Also, it is limited by the setup and hold time of DFF[7-8]. In the following design, we will focus on the decrease of setup and hold time of the DFF to reduce the system probability of error code.

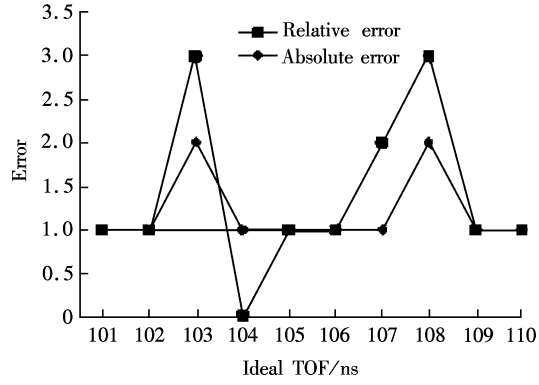


Fig. 7 Analysis of chip's absolute/relative error

Tab. 1 summarizes the comparison measurement results of the proposed circuit with other published readout circuits. The performance of the readout circuit is directly affected by the characteristics of TDC and the timing clock. According to the comparison results, the designed ROIC in this paper has the merits of high clock frequencies and wide measurement ranges. Nevertheless, there is still a certain gap between the designed ROIC in this paper and most advanced designs abroad.

Tab. 1 Comparison of readout circuit measurement results

Method	This paper	Ref. [9]	Ref. [10]
Process/μm	CSMC 0.5	Silicon CMOS 0.25	Standard CMOS 0.18
Supply/V	5	3.3	3.3
Operating temperature/K	298	290	
Pixel array	8×8	64×64	340×96
Frame frequency/(frame·s^{-1})	1 000	250	100
Time resolution/ns	1	3	0.2
Measurement range/ns	512		333

4 Conclusion

In this paper, an 8 × 8 array readout integrated circuit of frame type based on the Geiger mode InGaAs-APD sensor is designed. The pixel array of the ROIC system adopts the TDC built-in structure and each pixel counts independently. The test results show that under the 250 MHz clock, the ROIC can achieve a time resolution of 1 ns and resist the influence of power noise and external noise on the circuit. Future work will deal with the design of the clock phase separation and distance range in order to experimentally achieve a better performance of the infrared detection system or FPA.

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GM-APD 阵列型红外传感读出电路设计与实现

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摘要:基于盖革模式(GM)雪崩光电二极管(GM-APD)探测阵列,设计了一种可用于红外 3D 成像的高性能红外传感读出电路 (ROIC). 该电路系统主要由主动淬火电路(AQC)、时间数字转换电路(TDC)和其他时序控制电路 3 个模块组成. AQC 与 TDC 共同构成像素电路,在其余模块的配合下,由 AQC 电路检测 GM-APD 传感器产生的电流信号,TDC 电路进行光子飞行时间(TOF)的计量,并转换为数字信号输出,从而实现更好的噪声抑制,更高的探测灵敏度. 该电路采用 CSMC 0.5 μm 标准 CMOS 工艺流片,阵列规模为 8 × 8,像元中心距离 100 μm,芯片测试结果表明,电路功能良好,在 250 MHz 时钟驱动下,芯片可达到 1 ns 的时间分辨率,该电路可用于面阵结构红外探测系统或焦平面阵列.

关键词:红外 3D 成像;读出电路;盖革-雪崩光电二极管;主动淬火电路;时间-数字转换电路

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