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SPICE model of trench-gate MOSFET device

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Abstract: A novel simulation program with an integrated circuit emphasis (SPICE) model developed for trench-gate metal-oxide-semiconductor field-effect transistor (MOSFET) devices is proposed. The drift region resistance was modeled according to the physical characteristics and the specific structure of the trench-gate MOSFET device. For the accurate simulation of dynamic characteristics, three important capacitances, gate-to-drain capacitance C_{gd}, gate-to-source capacitance C_{gs} and drain-to-source capacitance C_{ds}, were modeled, respectively, in the proposed model. Furthermore, the self-heating effect, temperature effect and breakdown characteristic were taken into account; the self-heating model and breakdown model were built in the proposed model; and the temperature parameters of the model were revised. The proposed model is verified by experimental results, and the errors between measured data and simulation results of the novel model are less than 5%. Therefore, the model can give an accurate description for both the static and dynamic characteristics of the trench-gate MOSFET device.

Key words: trench-gate metal-oxide-semiconductor field-effect transistor (MOSFET); simulation program with integrated circuit emphasis (SPICE) model; drift region resistance model; dynamic model

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The trench-gate MOSFET is considered to be one of the most promising devices for power switching at voltages up to 100 V due to its low on-resistance and low gate charge[1-3]. Therefore, much attention has been focused on the development of the trench-gate MOSFET[4-5]. With the wide application of the trench-gate MOSFET device, an accurate and efficient SPICE model of trench-gate MOSFET is urgently needed for the design and simulation of power circuits.

Many studies about power MOSFET modeling have been reported[6-7]. These studies mainly focus on the modeling of double diffused MOSFET (DMOSFET). Since the gate of the trench-gate MOSFET extends into the N-drift region, the parasitic JEFT region of the conventional DMOSFET is eliminated. Therefore, the conventional models of power DMOSFET cannot reflect the drift region resistance of the trench-gate MOSFET and they are also unsuitable for the trench-gate MOSFET.

In this paper, a novel SPICE model of trench-gate MOSFET is proposed. In the static modeling section, the effect of accumulation and depletion regimes upon drift region resistance was considered under different gates and drain biases to model the drift region resistance accurately.

For the dynamic characteristics of trench-gate MOSFET, three important capacitances, drain-to-source capacitance C_{ds}, gate-to-source capacitance C_{gs}, and gate-to-drain capacitance C_{gd}, which have the significant effects on transient characteristics, were modeled, respectively. Besides, the self-heating effect and temperature effect were taken into account. In order to evaluate the reliability of the trench-gate MOSFET device, the breakdown voltage model was also included in the proposed model. According to the simulation results of the novel model and measured data, the errors of all the validations are less than 5%. Therefore, the proposed model gives a good description for trench-gate MOSFET devices.

1 Device Characterization

Fig. 1 shows the schematic cross-section structure of the trench-gate MOSFET. As shown in the figure, the trench gate extends into the N- epitaxial layer, and as the gate voltage is larger than the flat band voltage, the accumulation

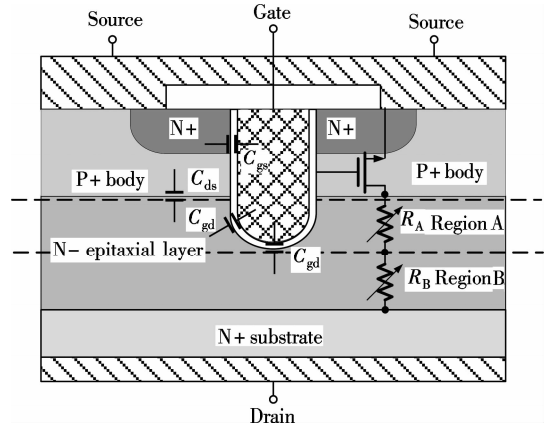

Fig. 1 The schematic cross-section structure of the trench-gate MOSFET

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region is formed along with the trench wall within the drift region. Furthermore, for different values of gate bias, the bottom of the trench-gate edge operates in different regimes, accumulation or depletion. However, the drift region which is the closest to the drain terminal is barely influenced by the variation of gate bias. According to this feature, the drift region can be separated into two parts: region A and region B. The resistance of region A is dependent on the gate bias and drain bias, while the resistance of region B is almost completely controlled by the drain bias.

2 SPICE Model for Trench-Gate MOSFET

2.1 The static model of trench-gate MOSFET

The static part of the trench-gate MOSFET model is shown in Fig. 2. The properties of the MOSFET core in the trench-gate MOSFET structure are captured by using the advanced low voltage model BSIM3v3, and the influences of region A and region B for static characteristic are presented as two resistors, which are R_A and R_B. Besides, the breakdown voltage model is built as a sub-circuit (the diode D_{break} in series with the controlled source E_{break}).

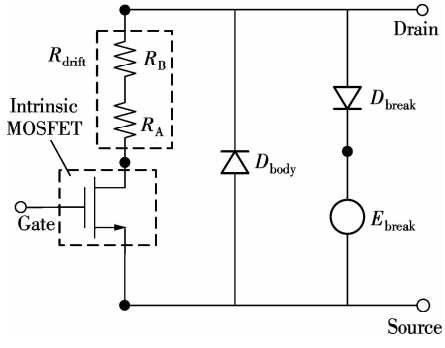

Fig. 2 The static model of trench-gate MOSFET

2.1.1 Drift region resistance model

The simulations of technology computer aided design (TCAD) reveal that, for lower V_{gs}, i.e. $V_{gs}=2$ V or $V_{gs}=4$ V, the current flow tends to stay away from the bottom of the trench-gate edge, and the drift region near the gate oxide operates in depletion regime[8]. For larger V_{gs} cases, the current flow tends to spread to the bottom of the trench-gate edge, gradually filling an otherwise depleted region, and an accumulation region is formed around the gate oxide within the drift region[9]. Therefore, the drift region can be partitioned into two sub-regions based on the current flow path. In region A, a portion of the current is confined to the accumulation layer at the trench wall, whereas in region B, the current flows throughout the total area.

According to the description above, the operating regime of region A is significantly influenced by the variation of gate and drain biases. Furthermore, due to the influence of the velocity saturation effect, the resistance of region A increases with the increase of V_{ds}. On the other hand, as the accumulation path beside the trench wall is formed, the resistance of region A decreases with the increase of V_{gs}, as observed in the TCAD simulation results in Fig. 3. Hence, the resistance of region A can be modeled as

$$R_A=(r_d+r_{dvd}V_{ds}+r_{dvdl}V_{ds}^2)(1-r_{dvg}(V_{gs}+r_{dvgl})) \quad (1)$$

where r_d is the intrinsic resistance of region A; r_{dvd}, r_{dvdl} are the impact factors of the velocity saturation effect; and r_{dvg}, r_{dvgl} are the parameters introduced by the forming accumulation path.

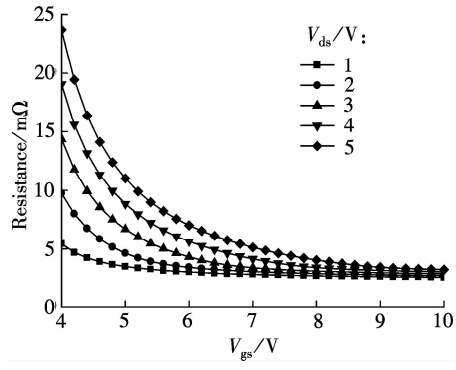

Fig. 3 Drift region resistance of TCAD simulations

In addition, the electrical resistivity of region B depends on its carrier mobility and doping concentration. Furthermore, the carrier mobility of region B is influenced by the vertical electric field, which is dependent on V_{ds}; therefore, the resistance of region B can be empirically modeled as

$$R_B=r_{vd}+r_{vdl}V_{ds} \quad (2)$$

where r_{vd} is the intrinsic resistance which depends on the doping concentration of region B, and r_{vdl} is the parameter introduced by the carrier mobility variation caused by the vertical electric field in region B.

By synthesizing Eqs. (1) and (2), the drift region resistance R_{drift} can be written as

$$R_{drift}=R_A+R_B=(r_d+r_{dvd}V_{ds}+r_{dvdl}V_{ds}^2)(1-r_{dvg}(V_{gs}+r_{dvgl}))+(r_{vd}+r_{vdl}V_{ds}) \quad (3)$$

With the increase in temperature, the reduction of the bulk mobility in the drift region results in the increase of drift region resistance[10]. The variation of the drift region resistance can be expressed as

$$R_{drift}(T)=R_{drift}(1+T_{C1}(T-T_0)+T_{C2}(T-T_0)^2) \quad (4)$$

where T_{C1} is the linear temperature coefficient; T_{C2} is the quadratic temperature coefficient for the drift region resistance; T_0 is the room temperature; and T is the operating temperature.

2.1.2 Breakdown voltage model

The breakdown characteristic of the trench-gate MOSFET device is important for its reliability. When the electrical field in the impact ionization region is sufficiently large, the channel current may increase significantly and cause breakdown.

As shown in Fig. 2, when the drain-to-source voltage is larger than the sum of the controlled source voltage and threshold voltage of the diode, the diode is opened-up, and then the current between drain and source becomes large. Moreover, the impact ionization is heavily influenced by temperature, and the breakdown voltage increases as the temperature increases[11]. Therefore, the characteristic of breakdown voltage V_b can be expressed as

$$V_{b,DSS}(T) = V_{t,Dbreak} + E_{break}(T) = 0.7 + k(1 + T_{C3}(T - T_0) + T_{C4}(T - T_0)^2) \quad (5)$$

where T_{C3} is the linear temperature coefficient; T_{C4} is the quadratic temperature coefficient; and k is the multiplication factor.

2.2 Dynamic model of trench-gate MOSFET

As for the dynamic model of trench-gate MOSFET, we introduce three important capacitances, C_{gd}, C_{ds} and C_{gs}. The dynamic model of the trench-gate MOSFET is completed by modeling the three capacitances accurately.

2.2.1 Model of C_{ds}

As shown in Fig. 1, C_{ds} is mainly a depletion capacitance which is made up of the vertical Pbody-Nepi junction[12], and the drain-to-source capacitance is written as

$$C_{ds} = C_{Jo}\left(1 - \frac{V_{ds}}{p_b}\right)^{-m_j} \quad (6)$$

where C_{Jo} is the zero-bias junction capacitance; p_b is the junction built-in potential; m_j is the varying coefficient of the junction capacitance. Therefore, as shown in Fig. 4, the depletion capacitance of the body diode D_{body} is used to simulate C_{ds}.

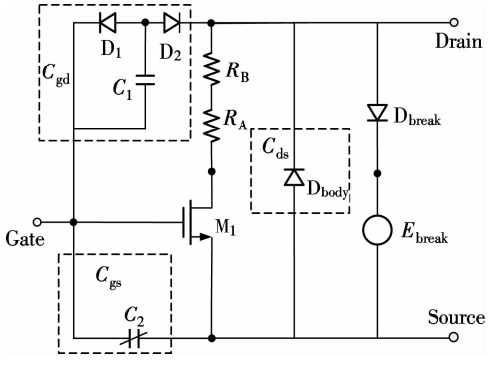

Fig. 4 Complete SPICE model of trench-gate MOSFET

2.2.2 Model of C_{gd}

The miller capacitance C_{gd} is one of the decisive factors for the dynamic characteristics of the trench-gate MOSFET[13]. As shown in Fig. 1, the miller capacitance C_{gd} is the series combination of the gate oxide layer capacitance at the trench bottom and the depletion capacitance of the drift region. The depletion capacitance of the drift region is present only if the drain voltage is larger than the gate voltage. Moreover, the trench-gate oxide layer capacitance at the trench bottom is the parallel combination of the bottom oxide layer capacitance $C_{ox,b}$ and the trench sidewall oxide layer capacitance $C_{ox,s}$[14]. Therefore, the Miller capacitance is presented as

$$\frac{1}{C_{gd}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \quad (7)$$

$$C_{ox} = C_{ox,b} + C_{ox,s} \quad (8)$$

$$C_{dep} = C_{Jo}\left(1 - \frac{V_{dep}}{p_b}\right)^{-m_j} \quad (9)$$

where C_{ox} is the trench bottom oxide capacitance; C_{dep} is the drift region depletion capacitance; V_{dep} is the potential difference within the drift region.

The trench gate oxide capacitance can be seen as a constant capacitance, therefore, it can be expressed as

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} W_1 L_1 \quad (10)$$

where t_{ox} is the thickness of the gate oxide; ε_{ox} is the permittivity of SiO_2; W_1 is the width of the oxide layer; and L_1 is the length of the oxide layer.

According to the description above, the gate-to-drain capacitance can be simulated by a simple macro circuit, as shown in Fig. 4, The constant capacitance C_1 is used to simulate the trench bottom oxide capacitance (the capacitance C_1 is much larger than the barrier capacitance of diode D_1). As for the drift region depletion capacitance, it is modeled by the barrier capacitance of diode D_2.

2.2.3 Model of C_{gs}

The capacitance C_{gs} consists of the channel capacitance and the overlap capacitance between gate and source. As shown in Fig. 5 (extracted gate-to-source capacitance of simulation results in TCAD), with the increase of V_{gs}, C_{gs} decreases first, then it increases nearly to a constant.

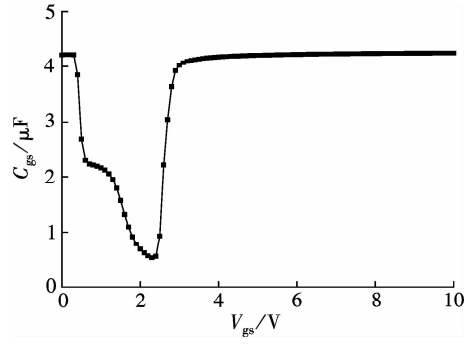

Fig. 5 Gate-to-source capacitance under $f = 1$ MHz and $V_d = 0$ V

According to the characteristic shown in Fig. 5, the gate-to-source capacitance C_{gs} can be empirically modeled as

$$C_{gs} = C_1\left(1 - \exp\left(-\frac{(V_{gs} - 1.5)^{\alpha}}{\beta}\right)\right) \quad (11)$$

where C_1 is the zero-bias junction capacitance; α, β are the fitting factors.

2.3 Self-heating model

The self-heating effect (SHE) represents the heating of the device due to its internal power dissipation. The increase of the internal temperature mainly affects the mobility, the threshold voltage and velocity saturation in devices[15]. Fig. 6 shows the standard equivalent sub-circuit used for the self-heating representation.

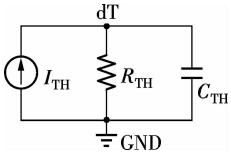

Fig. 6 Standard equivalent sub-circuit of self-heating effect

Clearly, the self-heating effect is related to the heat dissipation capacity of devices. The area and the width of the device have a great effect on the thermal resistance and thermal capacitance. Moreover, the thermal resistance and thermal capacitance vary dynamically with the device temperature. Therefore, the expressions of thermal resistance and capacitance are written as

$$R_{TH} = (R_{TH0} + R_{THW}W + R_{THL}L + R_{THA}WL)(1 + \theta_{RTH}(T - T_0)) \quad (12)$$

$$C_{TH} = (C_{TH0} + C_{THW}W + C_{THL}L + C_{THA}WL)(1 + \theta_{CTH}(T - T_0)) \quad (13)$$

where R_{TH0}, C_{TH0} are the intrinsic thermal resistance and thermal capacitance, respectively; R_{THW}, R_{THL}, R_{THA} are the thermal resistance fitting factors depending on length, width and area, respectively; C_{THW}, C_{THL}, C_{THA} are the thermal capacitance fitting factors depending on length, width and area; W, L are the width and length of device; and θ_{RTH}, θ_{CTH} are the temperature fitting factors.

3 Parameters Extraction and Model Validation

This model is validated on the measured characteristics of a 40 V trench-gate MOSFET device. The parameters of the presented model are extracted with the model building software MBP for the later verifications of the model. In order to verify the accuracy of our model under conditions which are different from those used for parameter curve fitting, the on-resistance characteristic and gate charge characteristic of the model are validated by several simple circuit simulations.

3.1 Parameters extraction

3.1.1 Static characteristics

The static characteristics fitting results in MBP are shown in Figs. 7 to 9. The comparisons of measured *I-V*

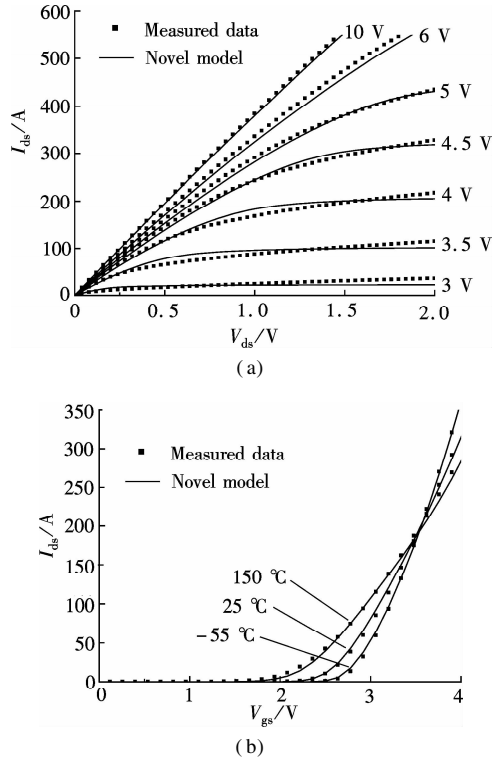

Fig. 7 Typical output and transfer characteristic curves. (a) Output under $T = 25$ ℃ with different gate-to-drain voltages; (b) Transfer under $V_{ds} = 10$ V with different temperatures

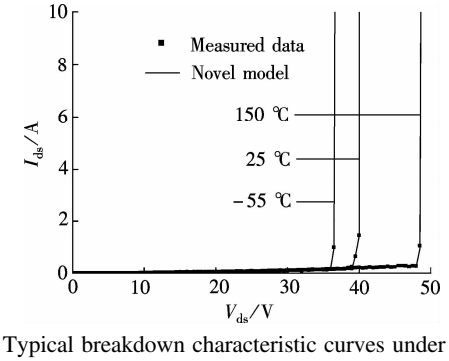

Fig. 8 Typical breakdown characteristic curves under $V_{gs} = 0$ V with different temperatures

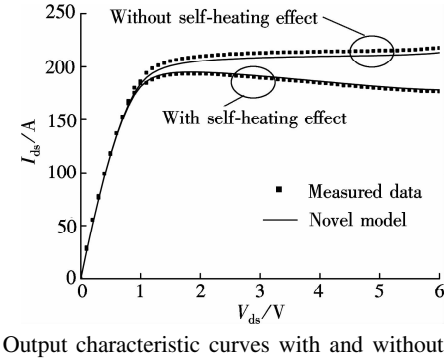

Fig. 9 Output characteristic curves with and without self-heating effect under $V_{gs} = 4$ V

curves and the novel model are shown in Fig. 7. It is clear that the presented model fits the measured data well. The fitting results of breakdown characteristic with different temperatures are shown in Fig. 8. In Fig. 9, the output characteristic curves with and without self-heating effect are fitted, respectively.

According to the presented curves, it is clear that the proposed model well fits the measured data in all operation regimes at the wide temperature ranges.

3.1.2 Dynamic characteristic

The fitting results of the input capacitance C_{iss} ($C_{iss} = C_{gs} + C_{gd}$), output capacitance C_{oss} ($C_{oss} = C_{gs} + C_{ds}$) and transfer capacitance C_{rss} ($C_{rss} = C_{gd}$) are presented in Fig. 10, and it confirms that the presented model well fits the measured *C-V* curves.

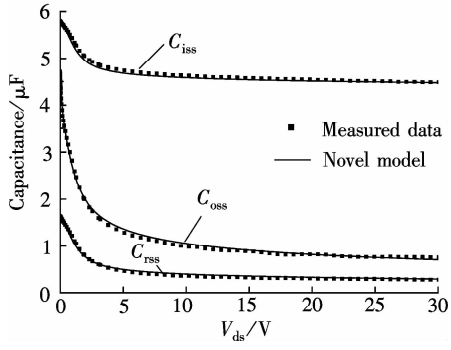

Fig. 10 Typical input capacitance, output capacitance and transfer capacitance curves under $f = 1$ MHz and $V_{gs} = 0$ V

According to the fitting *I-V* and *C-V* curves shown in Fig. 7 to Fig. 10, the parameters of the drift region resistance model, breakdown model, self-heating model and dynamic model are all extracted. Tab. 1 shows the extracting main parameters of the novel model for the target device based on the above figures.

Tab. 1 Main parameters for the normal MOSFET

Parameters	Value	Parameters	Value
V_{th0}/V	3.4	$K_1/V^{1/2}$	0.36
$K_2/10^{-2}$	−2.183 45	$U_0/(cm^2 \cdot (V \cdot s)^{-1})$	0.2
$U_a/10^{-11}(m \cdot V^{-1})$	7.242 5	$U_b/(10^{-19} m \cdot V^{-1})^2$	1.025 9
$U_c/10^{-10} V^{-1}$	−2.452 086	$V_{sat}/(10^5 m \cdot s^{-1})$	1.2
A_0	1.9	A_{gs}/V^{-1}	0.1

3.2 Model validation

For power semiconductor devices, the optimal value, which is the product of on-resistance and gate charge, is the indicator of device performance. In order to verify the on-resistance and gate charge of the presented model, the model has been simulated in several simple simulation circuits.

3.2.1 Static verification

As for static verification, the typical drain-to-source on-resistance curves between measured data and novel model results are shown in Fig. 11. Besides, the normalized breakdown voltage with different temperatures is shown in Fig. 12. It is clear that the model proposed in

Tab. 2 Added parameters in the proposed MOSFET

Parameters	Value	Parameters	Value
$r_d/10^{-3}$ Ω	2.154 45	$r_{dvd}/10^{-4}$	1.009 7
$r_{dvdl}/10^{-6}$	2.33	r_{dvg}	0.285 31
r_{dvgl}	0.576 94	$r_{vd}/10^{-4}$	1.108 2
r_{vdl}/Ω	0.426 52	T_0/℃	25
$T_{C1}/10^{-3}$	6.228 5	$T_{C2}/10^{-6}$	1.815 9
$C_{Jo}/(10^{-10} F \cdot m^{-2})$	9.2	p_b/V	0.238
m_j	0.7	$t_{ox}/10^{-8}$ m	1.5
$C_1/10^{-9}$ F	1.95	α	20.372 5
β	4.014 3	k	39.3
$T_{C3}/10^{-3}$	1.250 4	$T_{C4}/10^{-6}$	1.875 8
$R_{TH0}/(Km^2 \cdot W^{-1})$	0.051	$R_{THW}/10^{-3}$	1.012
$R_{THL}/10^{-4}$	2.784	$R_{THA}/10^{-3}$	0.592
$C_{TH0}/(J \cdot K^{-1})$	0.202	$C_{THW}/10^{-3}$	7.465
$C_{THL}/10^{-4}$	5.113	$C_{THA}/10^{-3}$	7.0282
$\theta_{RTH}/10^{-2}$	4.223	$\theta_{CTH}/10^{-2}$	2.174

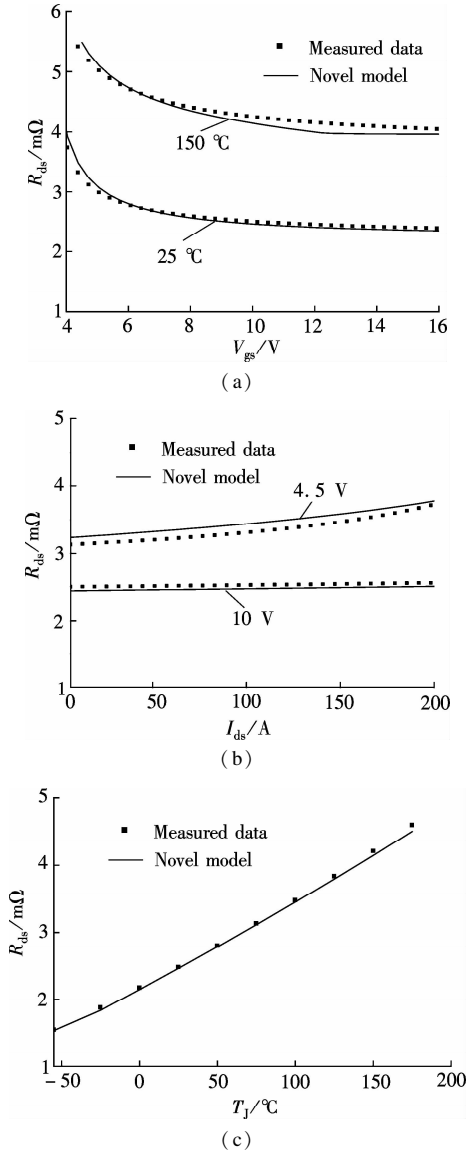

Fig. 11 On-resistance curves. (a) Under $I_{ds} = 80$ A with different temperatures; (b) Under $T = 25$ ℃ different V_{gs}; (c) Under $V_{gs} = 10$ V and $I_{ds} = 80$ A

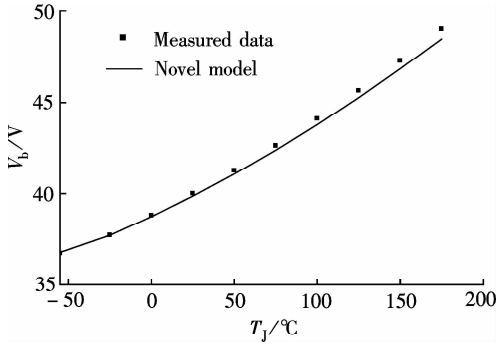

Fig. 12 Breakdown voltage under $V_{gs} = 0$ V and $I_{ds} = 10$ mA

this paper gives an accurate description for the drift region resistance and breakdown voltage.

For the validation of the self-heating model, on account of the difficulty in measuring the internal temperature of the operative target device, only the simulation results of the switching circuit are shown in Figs. 13 (a) and (b). As shown in the figures, the self-heating effect can be observed. Moreover, the drain-to-source current decreases with a larger duty cycle and higher frequency. Hence, the presented model can reflect the heat production of device and the power dissipation between the device and environment.

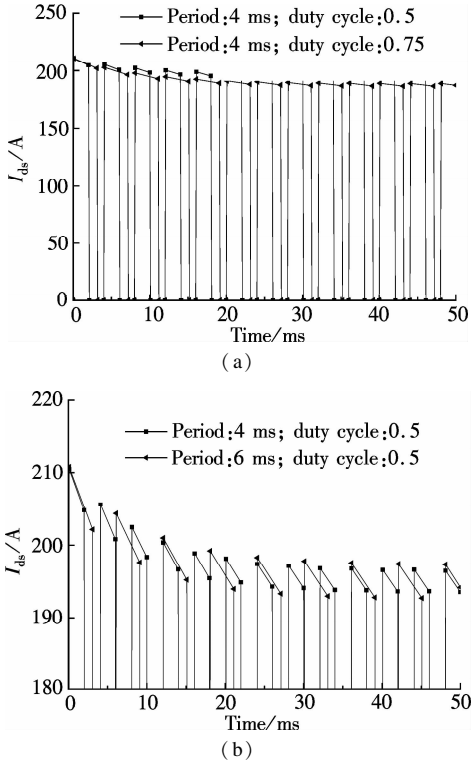

Fig. 13 Simulated *I-V* curves of presented model with self-heating model under $V_{ds} = 5$ V (V_{gs} with a high level of 4 V and a low level of 0 V). (a) With the same period but different duty cycles; (b) With the same duty cycle but different periods

3.2.2 Dynamic verification

For dynamic verification, as shown in Fig. 14, the novel model gives an accurate description to the gate

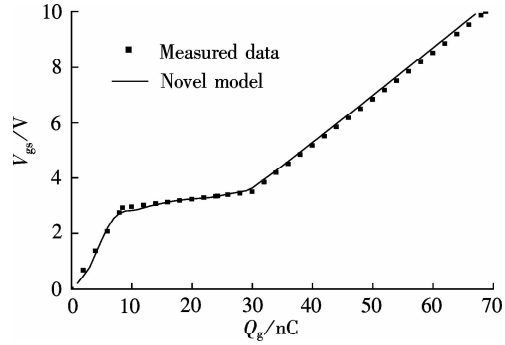

Fig. 14 Typical gate charge curves under $V_{ds} = 20$ V and $I_{ds} = 80$ A

charge characteristic.

According to the specific data, the errors of all the validation are less than 5%, therefore, the proposed model gives the accurate description for both the static and dynamic characteristics.

4 Conclusion

In this paper, a novel SPICE model for the trench-gate MOSFET device is presented. During the development of the static part of the proposed model, the drift region resistance is modeled according to its physical characteristics and specific structure. To account for the dynamic characteristics of devices, three important capacitances are modeled respectively. In addition, the breakdown voltage model and the self-heating model are also included in this model. In terms of the model verification with the actual measured data of the target devices, the novel model provides an accurate description of all operation regions for both the static and dynamic characteristics of the trench-gate MOSFET device.

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沟槽栅 MOSFET 器件 SPICE 模型

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摘要:针对沟槽栅纵向双扩散场效应晶体管(trench-gate MOSFET),提出了一种新型的 SPICE 模型. 通过对沟槽栅 MOSFET 器件的物理特性及其内在结构分析,建立了漂移区电阻模型. 为了准确模拟器件的动态特性,对栅源电容、栅漏电容及源漏电容分别建立了模型. 考虑了器件的自热效应、温度效应及击穿特性,建立了自热模型和击穿电压模型,并对模型温度参数进行了修正. 通过器件测试结果验证,各参数测试结果和对应模型的仿真结果误差均小于5%. 因此,该模型能准确地反映器件的静态和动态特性.

关键词:沟槽栅 MOSFET;SPICE 模型;漂移区电阻模型;动态模型

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