

Design of a 12-Gbit/s CMOS DNFFCG differential transimpedance amplifier

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Abstract: A 12-Gbit/s low-power, wide-bandwidth CMOS (complementary metal oxide semiconductor) dual negative feedback feed-forward common gate (DNFFCG) differential trans-impedance amplifier (TIA) is presented for the very-short-reach (VSR) optoelectronic integrated circuit (OEIC) receiver. The dominant pole of the input node is shifted up to a high frequency, and thus the bandwidth of the CMOS DNFFCG TIA is improved. Besides, two negative feedback loops are used to reduce the input impedance and further increase the bandwidth. The proposed TIA was fabricated using TSMC 0.18 μm CMOS technology. The whole circuit has a compact chip area, the core area of which is only 0.003 6 mm². The power consumption is 14.6 mW excluding 2-stage differential buffers. The test results indicate that the 3 dB bandwidth of 9 GHz is achieved with a 1.8 V supply voltage and its trans-impedance gain is 49.2 dB Ω . The measured average equivalent input noise current density is 28.1 pA/Hz^{1/2}. Under the same process conditions, the DNFFCG has better gain bandwidth product compared with those in the published papers.

Key words: very-short-reach; optoelectronic integrated circuit; negative feedback; feed-forward common gate; trans-impedance gain

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With the exponential growth in high speed transmission, electrical interconnection has encountered a bottleneck for the skin effect, dielectric loss, and channel cross-talk noises^[1]. As an alternative method to replace electrical interconnection, optical interconnection has attracted more and more attention. Optoelectronic integrated circuit receivers fabricated by standard CMOS technology have become such a huge trend in optical interconnects for their high cost-efficiency^[2–3].

For an optical receiver, the photodetector converts the optical signal into a current signal, and then the current signal is amplified and transformed into a voltage signal

by a trans-impedance amplifier (TIA). To achieve a photodetector with high responsivity, the area of the photodetector should be as large as possible, but that will make its parasitic capacitance large. However, large parasitic capacitance will have an impact on the bandwidth of the entire receiver.

Various techniques have been proposed to relax this bandwidth limitation. For example, inductive-peaking TIAs^[4–5] and regulated-cascode (RGC) TIAs and their modifications^[6–9] are widely used to enhance receiver bandwidths. RGC TIAs can effectively boost the bandwidth, but the intrinsic characteristics limit the performance. The inductive-peaking technology is another way to improve the bandwidth at the expense of voltage headroom and area consumption. Therefore, the challenge in designing TIAs is making a trade-off among bandwidth, area and power consumption.

In our OEIC system, a deep-N-well-strip-spatially-modulated photodetector (DNW-strip-SMPD) operating in an avalanche mode has been designed and tested. The parasitic capacitance is around 830 fF, and the responsivity is 1.4 A/W. Therefore, in this paper, a compact, low power and wide bandwidth TIA is proposed for the OEIC system.

1 Circuit Design and Analysis

1.1 Design of DNFFCG TIA

Fig. 1 shows the schematic of the DNFFCG TIA with a differential structure. The parasitic capacitance of the input node is a very large value compared with other nodes of the TIA circuit. Owing to these input parasitic capacitance components, the only way to improve the 3-dB bandwidth is to decrease the input resistance.

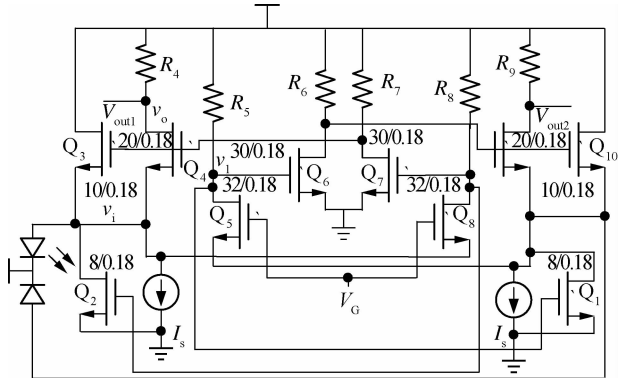


Fig. 1 The schematic diagram of DNFFCG differential TIA

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For the TIAs with common-gate topology, by increasing g_m , the input resistance can be reduced, but this will consume large amounts of power. Gain-boost technology is proposed with a large feedback gain to obtain enough equivalent g_m in the case of small g_{m4}/g_{m9} . In this design, a local feedback stage is employed, consisting of Q_8/Q_5 , R_8/R_5 , Q_7/Q_6 and R_7/R_6 . Besides, to further reduce the input resistance, two negative feedback loops are also designed. The first negative feedback loop is composed of Q_3/Q_{10} , Q_8/Q_5 , R_8/R_5 , Q_7/Q_6 and R_7/R_6 . The other negative feedback loop comprises Q_2/Q_1 , Q_8/Q_5 and R_8/R_5 . The input resistance of the DNFFCG differential TIA can be expressed as

$$Z_{in, DNFFCG} = \frac{1}{g_{m8} + g_{m8}g_{m2}R_8 + (g_{m4} + g_{m3})(1 + g_{m8}R_8g_{m7}R_7)} \quad (1)$$

It can be seen from Eq. (1) that the resistance can be reduced by increasing g_{m2} , g_{m3} or the local feedback gain. Fig. 2 shows the equivalent small-signal model of the DNFFCG TIA circuit to analyze poles and zeros. According to the Miller Theorem, C_{gs3} and C_{gs4} have been de-coupled between node 1 and 2. By solving the small-signal model equations, the approximate transfer function of DNFFCG TIA can be derived:

$$Z_{T, DNFFCG} = \frac{g_{m4}(g_7g_8 + g_{m7}g_{m8}) + g_{m4}M_1s + g_{m4}M_2s^2}{(g_4 + C_Ls)(M_3s^3 + M_4s^2 + M_5s + M_6)} \quad (2)$$

where

$$M_1 = g_8(C_{gs4} + C_{gs3}) + g_7(C_{gs7} + C_{gs2})$$

$$M_2 = (C_{gs4} + C_{gs3})(C_{gs7} + C_{gs2})$$

$$M_3 = (C_{gs4} + C_{gs3})(C_{gs7} + C_{gs2})(C_{gs8} + C_{in} + k(C_{gs4} + C_{gs3}))$$

$$M_4 = [(C_{gs4} + C_{gs3})(C_{gs7} + C_{gs2})(g_{m4} + g_{m8} + g_{m3}) + (C_{gs8} + C_{in} + k(C_{gs4} + C_{gs3}))][g_8(C_{gs4} + C_{gs3}) + g_7(C_{gs7} + C_{gs2})]$$

$$M_5 = (g_{m4} + g_{m8} + g_{m3})[g_8(C_{gs4} + C_{gs3}) + g_7(C_{gs7} + C_{gs2})] + g_7g_8(C_{gs8} + C_{in} + k(C_{gs4} + C_{gs3})) + g_{m2}g_{m8}(C_{gs4} + C_{gs3})$$

$$M_6 = (g_{m4} + g_{m8} + g_{m3})g_7g_8 + (g_{m3} + g_{m4})g_{m7}g_{m8} + g_7g_{m2}g_{m8}$$

Where, g_7 , g_8 , and g_4 are the conductance of R_7 , R_8 , and R_4 , respectively; C_L is the equivalent loading capacitance at the output node coming from the secondary circuit; k is the equivalent miller factor of C_{gs3} and C_{gs4} . In order to facilitate the analysis, the equation needs to be simplified as

$$Z_{T, DNFFCG} = \frac{E_3 + E_2s + E_1s^2}{(g_4 + C_Ls)(Z_1s^2 + Z_2s + Z_3)(D_1s + D_2)} \quad (3)$$

where

$$E_1 = g_{m4}(C_{gs4} + C_{gs3})(C_{gs7} + C_{gs2})$$

$$E_2 = g_{m4}[g_8(C_{gs4} + C_{gs3}) + g_7(C_{gs7} + C_{gs2})]$$

$$E_3 = g_{m4}(g_7g_8 + g_{m7}g_{m8})$$

$$D_1 = C_{gs8} + C_{in} + k(C_{gs4} + C_{gs3}) = C_{in, tot}$$

$$D_2 = (g_{m3} + g_{m4})\left(1 + \frac{g_{m7}g_{m8}}{g_7g_8}\right) + g_{m8} + g_{m2}g_{m8}\frac{1}{g_8} = \frac{1}{Z_{in}}$$

$$Z_1 = (C_{gs4} + C_{gs3})(C_{gs7} + C_{gs2})$$

$$Z_2 \approx \{(g_{m4} + g_{m8} + g_{m3})[g_8(C_{gs4} + C_{gs3}) + g_7(C_{gs7} + C_{gs2})] + g_{m2}g_8(C_{gs4} + C_{gs3})\}Z_{in}$$

$$Z_3 = g_7g_8$$

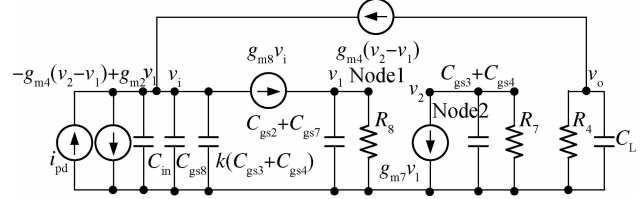


Fig. 2 Equivalent small-signal model for DNFFCG TIA circuit

For a typical complex-pole system $H(s) = \frac{\omega_n^2}{s^2 + 2\xi_{poles}\omega_n s + \omega_n^2}$, the frequency response of the complex poles can be characterized by the damping coefficient $\xi_{poles} = Z_2/(2\sqrt{Z_1Z_3})$. When $\xi_{poles} > 1$, the circuit response speed will slow down with the increase of ξ_{poles} , which will cause the eye diagram to not open. The maximal flat response will be obtained for $\xi_{poles} = 0.707$, while there is no bandwidth expansion effect. When $0 < \xi_{poles} < 0.707$, the amplitude response will have a peak, which will extend the bandwidth to some extent. The bandwidth expansion rate can be improved with the decrease of ξ_{poles} . However, ξ_{poles} cannot be too small, otherwise it will cause excessive gain overshoot, longer settling time and smaller phase linear range. In this design, there is a trade-off among the bandwidth extension, the gain overshoot, and settling time, and finally ξ_{poles} is chosen to be 0.3. In addition, two complex zeros in the denominator should be designed carefully. The complex zeros are arranged near the dominant pole, which can also play the role of expanding the bandwidth. The frequency responses of the complex zeros are opposite to the complex poles. To balance these two contrary effects, $\xi_{zeros} = Z_2/(2\sqrt{Z_1Z_3})$ is chosen to be 0.35.

Fig. 3 shows the pre-simulation AC curves of the DNFFCG differential TIA with the different input parasitic capacitance. The 3-dB bandwidths of 730, 830 and 930 fF are 9.9, 9.5 and 8.9 GHz, respectively.

1.2 Noise analysis

For the entire optical receiver, the noise of the frontend TIA is usually the dominant contributor to the input referred noise. The total equivalent input noise current spectral density of the TIA is derived by analyzing the equivalent input noise contributed by each noise sources.

First, the low frequency trans-impedance gain from each node to the output needs to be derived:

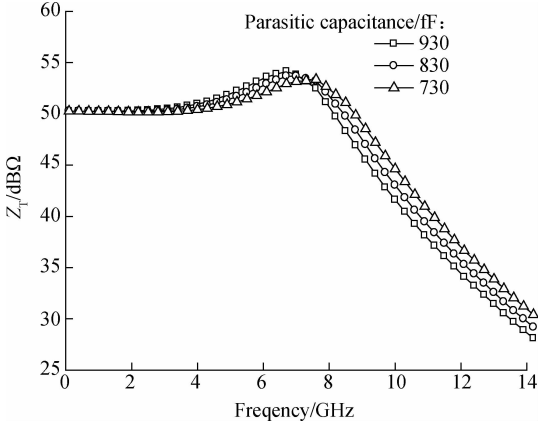


Fig. 3 The pre-simulation AC curves of the DNFFCG TIA

$$Z_{i-o} = \frac{g_{m4}(g_7g_8 + g_{m7}g_{n8})}{(g_{m4} + g_{n8} + g_{n3})g_7g_8g_4 + (g_{n3} + g_{m4})g_{m7}g_{n8}g_4 + g_7g_{m2}g_{n8}g_4} \quad (4)$$

$$Z_{l-o} = \frac{g_{m4}(-g_7g_{n7} + g_{m7}g_{n8})}{(g_{m4} + g_{n8} + g_{n3})g_7g_8g_4 + (g_{n3} + g_{m4})g_{m7}g_{n8}g_4 + g_7g_{m2}g_{n8}g_4} \quad (5)$$

$$Z_{2-o} = \frac{-g_{m4}(g_{n2}g_{n8} + g_{n8}g_8)}{(g_{m4} + g_{n8} + g_{n3})g_7g_8g_4 + (g_{n3} + g_{m4})g_{m7}g_{n8}g_4 + g_7g_{m2}g_{n8}g_4} \quad (6)$$

$$Z_{o-o} = g_4 \quad (7)$$

The overall input noise current spectral density can be evaluated as

$$\begin{aligned} \bar{V}_{o,eq}^2 \approx & \sum_{m=4}^9 \bar{i}_{n,eq,R_m}^2 Z_{R_m} + \sum_{k=1}^{10} \bar{i}_{n,eq,Q_k}^2 Z_{Q_k} = \\ & \left(\bar{i}_{nd,Q_3}^2 + \bar{i}_{nd,I_1}^2 \right) Z_{i-o}^2 + \left(\bar{i}_{nd,Q_4}^2 4kTR_8 \right) Z_{i-o}^2 + \\ & \left(\bar{i}_{nd,Q_1}^2 + 4kTR_7 \right) Z_{2-o}^2 + \left(\bar{i}_{nd,Q_4}^2 + 4kTR_4 \right) Z_{o-o}^2 \end{aligned} \quad (8)$$

where i_{n,eq,Q_k} is the drain noise current of transistor Q_k ; i_{n,eq,R_m} is the thermal noise current of resistor R_m ; and Z_{R_m} and Z_{Q_k} are the trans-impedance gain between corresponding nodes and output. The total average equivalent input noise current can be expressed as

$$\bar{i}_{in,eq}^2 = \frac{\bar{V}_{o,eq}^2}{Z_T^2} \quad (9)$$

As the values of R_4 , R_7 and R_8 are relatively high, the thermal noise from these resistances cannot be the major contributors. Theoretically speaking, Q_8/Q_5 contributes most to the total noise-current spectral density. Therefore, the W/L of Q_8/Q_5 needs to be optimized. Fig. 4 shows the pre-simulation results of the average equivalent input noise current densities at different W/L of Q_8/Q_5 . The average equivalent input noise current densities will decrease by increasing the W/L of Q_8/Q_5 . However, the C_{gs} of Q_8/Q_5 will be large, and it will have an impact on the bandwidth. Finally, the W of Q_8/Q_5 is chosen to be $32 \mu\text{m}$. Besides, Q_3/Q_{10} and Q_2/Q_1 are introduced to further

reduce the input resistance, but it will increase the noise and decrease sensitivity. The average equivalent input noise current densities are increased by $6 \text{ pA/Hz}^{1/2}$ by simulation. The sensitivity S can be calculated by^[10]

$$S = \frac{Q i_n \sqrt{B}}{R_{PD}} \quad (10)$$

where Q is the theoretical factor; B is the bandwidth of the TIA; and R_{PD} is the responsivity of the photodetector. As the responsivity of the DNW-strip-SMPD is larger than most of the photodetectors fabricated by CMOS technology, it can reduce the influence of the noise current densities on sensitivity. Also, it is more important to achieve a large bandwidth in the case of the large parasitic capacitance of the photodetector, so appropriate sacrifice of noise current densities is acceptable. For $\text{BER} = 10^{-12}$, $Q = 7$ and the theoretical calculation of sensitivity is approximately -33 dBm .

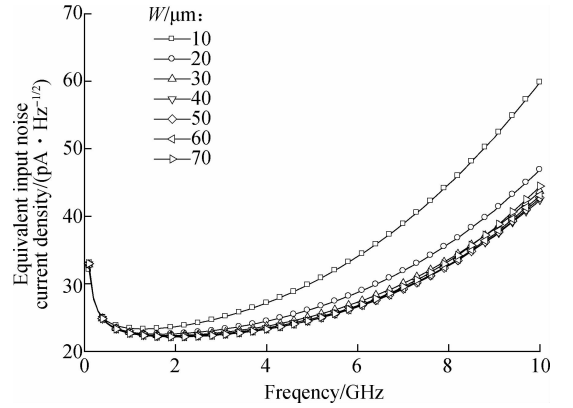


Fig. 4 The pre-simulation results of the average equivalent input noise current densities at different W of Q_8/Q_5

2 Implementation and Measurement Result

The chip micrograph of the proposed circuit and the diagram of the measurement setup are shown in Fig. 5 and Fig. 6, respectively. The chip area is $0.45 \times 0.49 \text{ mm}^2$ including all pads, while the core area is $0.06 \times 0.06 \text{ mm}^2$. At the bias condition of unified 1.8-V VDD , 1.1-V VG , the proposed circuit consumed 24.2 mW power including 2-stage differential buffers, while DNFFCG stages consumed 14.6 mW .

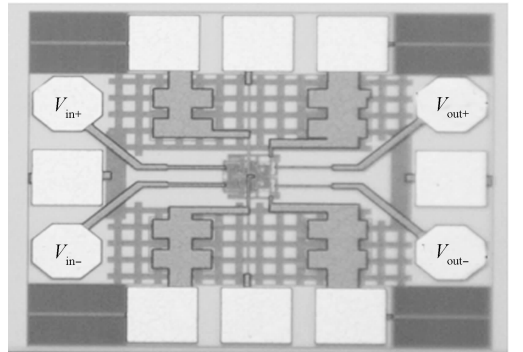


Fig. 5 The chip micrograph of the proposed circuit

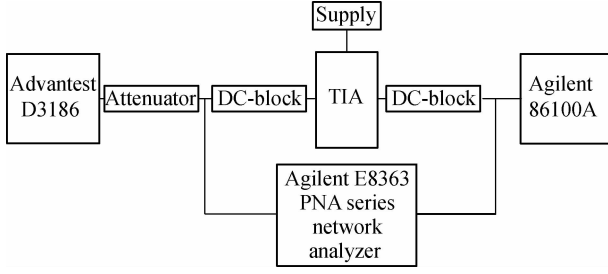


Fig. 6 Measurement setup

The test 3-dB bandwidth and gain are shown in Fig. 7, as well as the simulated 3-dB bandwidth and gain. The test 3-dB bandwidth of the proposed DNFFCG TIA is 9 GHz and the test transimpedance gain is 49.2 dB Ω . Fig. 8 shows the simulated and measured average equivalent input noise current densities. The measured average equivalent input noise current density is 28.1 pA/Hz $^{1/2}$. As the test environment will affect the test result, the results of the measured average equivalent input noise current densities are larger than the simulation results. Besides, the measured minimum input peak-to-peak voltage is 5 mV.

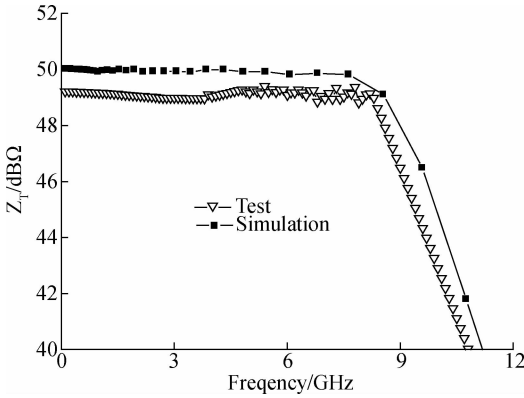


Fig. 7 The post simulated and measured frequency responses of the proposed TIA

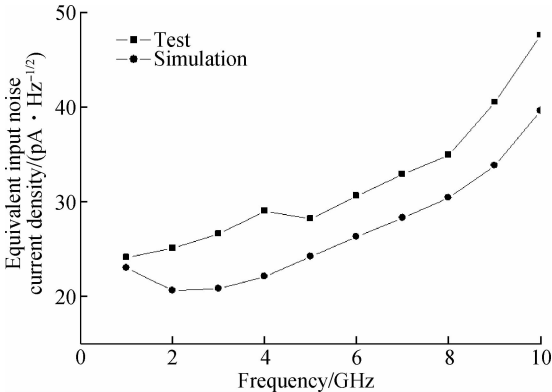


Fig. 8 The post simulated and measured average equivalent input noise current densities

The figure of merit (FoM) is defined as

$$\text{FoM} = \frac{Z_T f_{3\text{ dB}}}{I_{\text{noise}} P_{\text{DC}} S} \quad (11)$$

where Z_T is the transimpedance gain; $f_{3\text{ dB}}$ is the 3 dB bandwidth; I_{noise} is the average equivalent input noise current density; P_{DC} is the power consumption; S is the core area of the chip. FoM of the DNFFCG differential TIA is calculated to be 299.8. The proposed work shows superiority in terms of FoM. In addition, the output eye diagrams measured are shown in Fig. 9 with a $2^{23} - 1$ pseudorandom bit sequence input data at frequencies of 10 and 12 Gbit/s ($V_{\text{in-pp}} = 20\text{ mV}$).

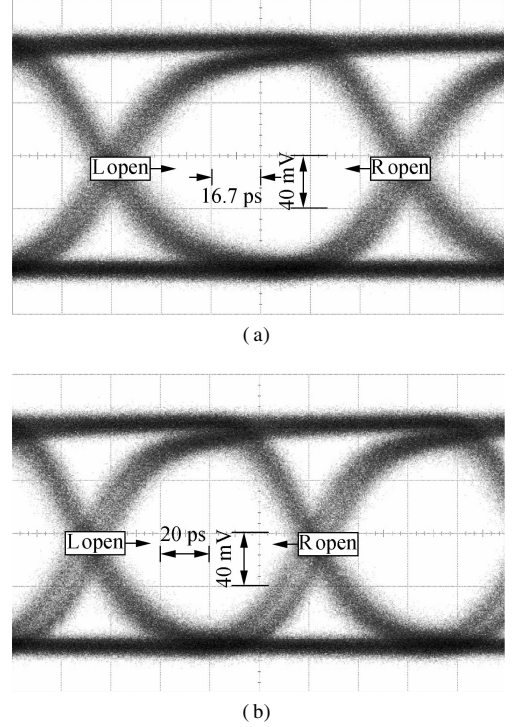


Fig. 9 Output eye-diagram of the proposed preamplifier with $2^{31} - 1$ PRBS NRZ input data. (a) 10 Gbit/s; (b) 12 Gbit/s

Tab. 1 shows a summary of the implemented CMOS UWB TIA, and recently reported state-of-the-art CMOS UWB TIAs. As can be seen, compared with other works, it exhibits the highest FOM. Moreover, if the difference of manufacturing costs between these processes is taken into account, the performance-to-cost ratio of this work is in the first class.

3 Conclusion

A DNFFCG differential TIA fabricated in a 0.18 μm CMOS process is proposed for the VSR OEIC system in this paper. Moreover, the transmission rate of 12 Gbit/s can be achieved with a very small chip area and low consumption power. Measured results demonstrate that the TIA has a transimpedance gain of 49.2 dB Ω with a 3 dB bandwidth of 9 GHz. The measured average equivalent input noise current density is 28.1 pA/Hz $^{1/2}$. The DNFFCG differential TIA can be applied to low cost, low power and high speed optical communication systems.

Tab. 1 Performance comparison of CMOS UWB TIA

Reference	CMOS technology/ μm	$Z_T/\text{dB}\Omega$	3-dB BW/ GHz	Core area/ mm^2	P_{DC}/mW	$I_{\text{noise}}/(\text{pA} \cdot \text{Hz}^{-1/2})$	Topology	C_{PD}/pF	$\text{FoM}/(\text{GHz} \cdot \text{dB}\Omega \cdot \text{pA}^{-1} \cdot \text{Hz}^{1/2} \cdot \text{mW}^{-1} \cdot \text{mm}^2)$
Ref. [7]	0.18	55.0	7	0.100 0	18.6	17.5	Single	0.30	11.8
Ref. [8]	0.13	50.1	7	0.016 0	7.5	31.3	Single	0.25	93.4
Ref. [9]	0.18	46.0	4	0.035 0	10.7	10.0	Single	0.25	49.1
Ref. [11]	0.13	55.3	6	0.040 0	2.0	24.0	Single	0.25	172.8
This work	0.18	49.2	9	0.003 6	14.6	28.1	Differential	0.83	299.8

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12 Gbit/s CMOS DNFFCG 差分跨阻放大器的设计

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摘要:提出了一种 12-Gbit/s 的低功耗、宽带 CMOS 具有双反馈结构的前馈共栅差分跨阻放大器,用于甚短距离传输光电集成电路接收机. 通过将输入节点的主极点提高到一个较高的频率,增大了放大器带宽. 此外,采用 2 个反馈环路降低输入等效电阻,从而进一步提高了带宽. 提出的跨阻放大器采用 TSMC 0.18 μm CMOS 工艺制造. 整个电路具有较小的芯片面积,其核心面积仅为 0.003 6 mm^2 . 在不考虑两级差分的缓冲放大器时,其功耗为 14.6 mW. 测试结果表明,在 1.8 V 的电源电压下,实现了 9 GHz 的 3 dB 带宽和 49.2 dB Ω 的跨阻增益. 测量的平均输入噪声电流功率谱密度为 28.1 pA/Hz^{1/2}. 在相同的工艺条件下,与已发表的文献相比,DNFFCG 差分跨组放大器具有最佳的增益带宽积.

关键词:短距离;光电集成电路;负反馈;前馈共栅;跨阻增益

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