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A weighted averaging method for signal probability of logic circuit combined with reconvergent fan-out structures

Xiao Jie Ma Weifeng William Lee Shi Zhanhui

(College of Computer Science and Technology, Zhejiang University of Technology, Hangzhou 310023, China)

Abstract: By analyzing the structures of circuits, a novel approach for signal probability estimation of very large-scale integration (VLSI) based on the improved weighted averaging algorithm (IWAA) is proposed. Considering the failure probability of the gate, first, the first reconvergent fan-ins corresponding to the reconvergent fan-outs were identified to locate the important signal correlation nodes based on the principle of homologous signal convergence. Secondly, the reconvergent fan-in nodes of the multiple reconverging structure in the circuit were identified by the sensitization path to determine the interference sources to the signal probability calculation. Then, the weighted signal probability was calculated by combining the weighted average approach to correct the signal probability. Finally, the reconvergent fan-out was quantified by the mixed-calculation strategy of signal probability to reduce the impact of multiple reconvergent fan-outs on the accuracy. Simulation results on ISCAS85 benchmarks circuits show that the proposed method has approximate linear time-space consumption with the increase in the number of the gate, and its accuracy is 4.2% higher than that of the IWAA.

Key words: improved weighted averaging algorithm; signal probability estimation; gate error rate; combinational logic circuits

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With the development of deep submicron and nanometers technology in VLSI, the reliability evaluation for high level circuits has increasingly become the focus of attention[1]. Furthermore, the circuits in newer VLSI manufacturing technologies are more prone to dynamic errors caused by reduced noise margin, lower supply voltage and a low stored charge in circuit nodes[2]. This makes VLSI become very sensitive to the signal probability (SP) of logic circuits, such as soft (transient) errors and random process variation[3].

However, the complexity of the exact calculation for the signal probability grows exponentially with the circuit size, which is caused by the signal correlations arising from reconvergent fan-outs (RFOs). Therefore, the task of signal probability computation was regarded as a sharp-P-complete problem[4], which is possibly even more difficult than a NP-complete problem.

To deal with the complex problem, several algorithms have been proposed for signal probability computation in search for a good trade-off between accuracy and computational complexity, such as the weighted averaging algorithm (WAA)[5], the improved weighted averaging algorithm (IWAA)[6-7], the probabilistic gate model (PGM)[8-9], probabilistic transfer matrices (PTM)[10-11], Bayesian networks (BN)[12], probabilistic decision diagrams (PDD)[13], and stochastic computational models (SCM)[14]. The several aforementioned algorithms have certain impact, but they are inaccurate or have high computational complexity.

In this paper, a new method based on the IWAA is proposed to calculate the signal probability of logic circuits under multiple independent errors, where a failure in each gate is assumed to affect the output with a probability, i.e., gate error rate, regardless of other gate failures. The steps are as follows: First, calculate the initial signal probability of each lead by a simple logic function that provides a transform of the signal probability from input to output. Secondly, find the reconvergent fan-ins (RFIs) where the fan-out branch is convergent for the first time. Then, calculate the signal probability of RFIs with the weighted average. Finally, introduce some correction terms into the signal probability equation for RFIs to improve the accuracy of the algorithm. Our proposed method is probably suitable for circuits without RFOs. The empirical evidence indicates that our approach improves computational efficiency and its accuracy is acceptable.

1 Background

1.1 Signal probability

The main difficulty of the signal probability computation is the presence of the reconvergent fan-out[5], including the effects of the fan-out branch, multiplicity dependencies and signal correlation, which are the main

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Biography: Xiao Jie (1984—), male, doctor, lecturer, xiaojiexqj@foxmail.com.

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sources of error. Monte Carlo (MC) simulation is an accurate method recognized by the VLSI community and is often used to simulate circuit behaviors[15]. Therefore, it is applied to calculate the signal probability.

However, large simulations in MC are needed to ensure its accuracy due to its random sampling. The approach of algebraic operations upon probabilities is used to the signal probability computation. It is simple and generic due to the fact that this approach associates variable names with each of the input leads representing the signal probability of the input lead[5] and computing the signal probability of each output lead with algebraic expressions including these variables.

In this paper, we assume that the binary input or output signal of the gate is associated with a variable that denotes the signal probability of the gate. The signal probability is defined as the probability that the signal is a logical "1", i.e. p (signal = 1)[3].

For convenience, unless otherwise stated, the signal probability of lead A called p_A refers to the probability that the logic signal of A is "1" in the following sections.

The formula of the signal probability calculation for the logic gates with two-input and fault-free was proposed in Ref. [16]. For instance, if the signal probabilities of the inputs for AND gate are p_1 and p_2, the signal probability of the output is p_1p_2. In the case of the OR gate, the signal probability of the output is equal to $1-(1-p_1)(1-p_2)$. In general, the formulas of the signal probability calculation are shown in the Tab. 1. For the XOR gate, the simplified formula is complicated due to the multiple input gates, so only gates with two inputs are given.

In fact, any gates in a circuit may fail, namely a von Neumann error, which flips the correct output of a gate and resembles the behavior of a soft error[14]. Therefore, the computation formula of the signal probability s_A for the logic gate can be expressed as[8]

$$s_A = p_A(1-\varepsilon) + (1-p_A)\varepsilon \tag{1}$$

where p_A is the output signal probability of lead A with fault-free computed by the rules in Tab. 1 and ε is a constant error rate of the gate.

Tab. 1 Set of rules for calculating the lead signal probabilities of the logic circuits which are fault-free

Gate	Signal probabilities of input leads	Probabilistic equation
NOT	p	$1-p$
AND	$p_1, p_2, p_3, \cdots, p_n$	$p_1p_2p_3, \cdots, p_n$
NAND	$p_1, p_2, p_3, \cdots, p_n$	$1-p_1p_2p_3, \cdots, p_n$
OR	$p_1, p_2, p_3, \cdots, p_n$	$1-(1-p_1)(1-p_2), \cdots, (1-p_n)$
NOR	$p_1, p_2, p_3, \cdots, p_n$	$(1-p_1)(1-p_2), \cdots, (1-p_n)$
XOR	p_1, p_2	$1-p_1p_2-(1-p_1)(1-p_2)$

Indeed, if a logic circuit is fan-out free, the signal probability can be computed correctly in linear time[3,6], and the calculation process in Ref. [8] is as follows.

Algorithm 1 A signal probability estimation for logic circuits with fan-out free

Input: A logic circuit;

Output: An estimation of the signal probability of each lead in the logic circuit.

Compile the circuit by organizing it into levels.

Assign signal probabilities of 1/2 to all the primary inputs (PIs) and set the value of the error rate of ε.

Compute the signal probability of each lead from the PIs to the primary outputs (POs) in the circuit using the formulas shown in Tab. 1 and Eq. (1).

End the algorithm.

We further illustrate Algorithm 1 using a simple circuit as follows. As shown in Fig. 1, the circuit has no RFO and the gate error rate $\varepsilon = 0.1$. First, the circuit is compiled and partitioned into three levels. Then the signal probabilities of PIs are set to be 0.5, namely, $p_A = p_B = p_C = p_D = 0.5$, which are also used in later cases in this paper. Finally, the signal probability of each lead in the circuit can be computed by Algorithm 1. The calculation procedures are as follows: 1) $p_E = p_Ap_B = 0.25$, $s_E = p_E(1-\varepsilon) + (1-p_E)\varepsilon = 0.3$; 2) $p_F = 1-(1-p_C)(1-p_D) = 0.75$, $s_F = p_F(1-\varepsilon) + (1-p_F)\varepsilon = 0.7$; 3) $p_G = s_Es_F = 0.21$, $s_G = p_G(1-\varepsilon) + (1-p_G)\varepsilon = 0.268$.

Particularly, if the logic circuit is fan-out free, Algorithm 1 yields exact signal probabilities. By contrast, Algorithm 1 yields an approximation for the signal probability[2-3]. Hence, Algorithm 1 can be successfully applied to the parts of general circuits that are fan-out free, otherwise it results in an approximate result.

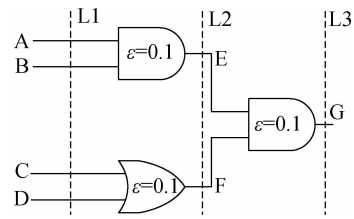

Fig. 1 Schematic of a simple circuit

1.2 Basic idea of the IWAA

Ref. [6] proposed the IWAA based on the WAA which overcomes the drawback of the WAA, but it is inaccurate in estimating the effects of RFOs on the circuit, since the WAA uses a weighted average as the value of signal probabilities associated with the PIs.

Given a logic circuit, if lead A is a reconvergent fan-out, then the signal probability computation of Algorithm 1 for lead S beyond that reconvergent node is likely to be erroneous due to the multiple dependencies on A[5]. There is a simple modification of Algorithm 1 to avoid and reduce such error. The signal probability equation is given as[3-4]

$$S_A = S_{A(0)}(1-p_A) + S_{A(1)}p_A \tag{2}$$

where S_A is the signal probability of S associated with A; $S_{A(0)}$ and $S_{A(1)}$ are the signal probability of S when the signal probability of A is set to be 0 and 1, respectively.

There is only one RFO in a circuit that is similar to the circuit presented in Fig. 1. As shown in Fig. 2, S_A is equal to 0.268 when it is calculated by Algorithm 1. However, the result of S_A is incorrect, caused by the signal correlation of the fan-out branch (A1 and A2). However, the real value of S_A is equal to 0.6, which can be computed by Algorithm 2[4,6]. However, for the circuit with multiple RFOs, Algorithm 2 cannot obtain a good calculation precision.

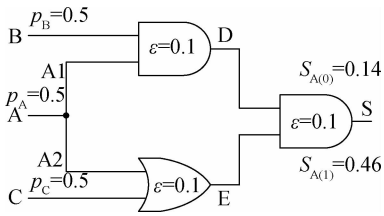

Fig. 2 A simple circuit with one RFO

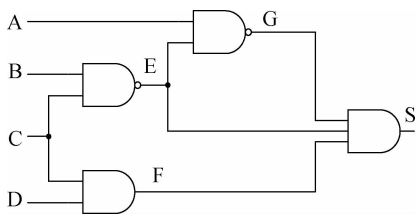

Fig. 3 A circuit with two RFOs

Algorithm 2 A signal probability estimation method associated with the reconvergent fan-out

Input: A logic circuit with only one RFO, a reconvergent fan-out A, lead S beyond the reconvergent node;

Output: An estimation of the signal probability of S in the logic circuit.

Calculate the signal probability p_A of A by Algorithm 1.

Compute $S_{A(0)}$ and $S_{A(1)}$ from A to S using the formulas shown in Tab. 1 and Eq. (1) when the signal probability of A is set to 0 and 1, respectively.

Calculate S_A of S using Eq. (2).

End the algorithm.

Ref. [6] defined dependency as a partial order relationship if there is a path from lead C to the POs and lead E in this path, E depending on C (see Fig. 3). Furthermore, for lead S, the minimum reconvergent fan-out set (MRFS)[6] of S is a set; i.e., (MRFS(S) is {C}, as shown in Fig. 3) where each element, which is reconvergent fan-out, reconverges at S for the first time and does not depend on any other reconvergent fan-outs in the MRFS.

In the IWAA[6], if A_1, A_2, A_3, ⋯, A_m are the elements in the MRFS of lead S, the signal probability S of S can be calculated according to the following steps: 1) Compute the signal probability S_1 of S by Algorithm 1; 2) Calculate $S_{A,i}$ ($1 \leqslant i \leqslant m$) by Algorithm 2; 3) Compute the weighted average estimate S of the signal probability of lead S by the following formula[6].

$$S = \begin{cases} S_1 & \sum_{j=1}^{m} |S_1 - S_{A,j}| = 0 \\ \sum_{i=1}^{m} w_i S_{A,i} & \text{otherwise} \end{cases} \quad (3)$$

where

$$w_i = \frac{|S_1 - S_{A,i}|}{\sum_{j=1}^{m} |S_1 - S_{A,j}|} \quad (4)$$

In view of the above-mentioned discussion, finding the MRFS of lead S is the crucial part. The importance of finding the MRFS(S) is to find the minimum reconvergent fan-out from these RFOs which are between PIs and S.

To a certain extent, the IWAA improves the precision of the signal probability estimation. It calculates the signal probability of lead S by the weighted average method associated with elements of MRFS(S). However, it only considers the effects of the reconvergent fan-outs in the MRFS and obtains the corrected signal probability of S. However, it does not consider the effects of some interesting RFOs. Taking Fig. 3 as an example, the IWAA estimates the signal probability of lead S without considering the reconvergent fan-out E. Furthermore, it does not consider the effects of the reconvergent fan-ins which are in the paths from elements of MRFS(S) to S. For example, the IWAA estimates the signal probability of lead L (see Fig. 5) without considering the impact of the reconvergent fan-in H.

Hence, an improved method based on the IWAA[6] is proposed in this paper to improve its computational accuracy and reduce time complexity.

2 Structure of Reconvergent Fan-Out

The main problem of signal probability calculation for logic circuits is the need to consider the mutual effects of RFOs, since the gate inputs are correlated at the reconvergent nodes. Furthermore, there is more than one RFO in generic, so the correlations of the inputs of reconvergent fan-ins are complex. For ease of understanding, in this section, we introduce some concepts about the basic structures of RFO.

2.1 Single structure with reconvergent fan-out

The single structure with reconvergent fan-out consists of one RFI and one RFO corresponding to the RFI. It can be divided into completely independent reconvergent fan-out and half embedded reconvergent fan-out, according to the relationship between reconvergent fan-outs and reconvergent fan-ins.

There is a single structure with reconvergent fan-out of

the circuit, as shown in Fig. 4. It is B→F with the structure of completely independent reconvergent fan-out. In this structure, there is no other reconvergent fan-ins in the path from reconvergent fan-out B to reconvergent fan-in F.

In Fig. 5, there are two structures of univocal reconvergent fan-out. B→H is the structure of completely independent reconvergent fan-out and C→L is the structure of half embedded reconvergent fan-out. H is a reconvergent fan-in in the structures of B→H and C→L. However, the reconvergent fan-out of B, which is part of the structure of B→H, is not in the path of C→L.

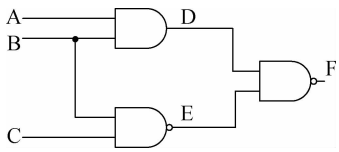

Fig. 4 Structure of completely independent reconvergent fan-out

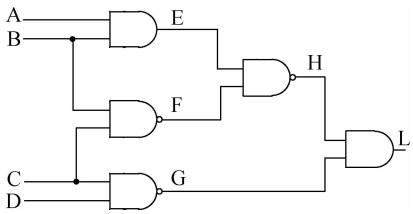

Fig. 5 Structure of half embedded reconvergent fan-out

2.2 Multiple structure with reconvergent fan-out

For the circuit that contains two or more structures with reconvergent fan-out, they can be divided into the independent, parallel and embedded types[17] by the relationship between the structures with reconvergent fan-out.

The structures of B→G and C→H are completely independent reconvergent fan-out (see Fig. 6), and they have no common nodes.

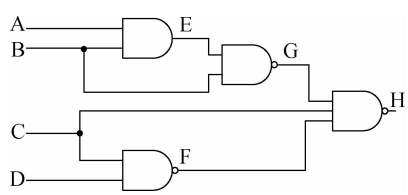

Fig. 6 Structure of independent reconvergent fan-out

The structure of parallel reconvergent fan-out has two or more structures with the same RFI. For example, in the structures of A→E and B→E (see Fig. 7), they have some common nodes and the same RFI E.

The structure of the embedded structure is that other single structures are included in the structure. As shown in Fig. 8, E→H is the structure of completely independent reconvergent fan-out and it is contained in the structure of C→I.

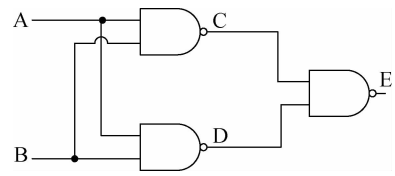

Fig. 7 Structure of parallel reconvergent fan-out

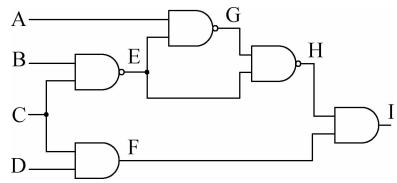

Fig. 8 Structure of embedded reconvergent fan-out

3 Signal Probability Calculation

For a simple circuit with a structure of embedded reconvergent fan-out, it will be straightforward for us to iteratively calculate the accurate signal probability of each lead in the circuit by Algorithm 2. However, the actual circuit contains many structures of reconvergent fan-out and its scale is very large, so it requires high time and space complexity to compute the signal probability by using this approach.

In this paper, we present a concept of the nearest reconvergent fan-out set (NRFS): the NRFS(S) is a RFO set of lead S called FRFI which is RFI in the logic circuit, and each element in the set is RFO and converges at S for the first time. For example, the NRFS(S) is {C, E} (see Fig. 3). Compared with MRFS, NRFS does not consider the dependencies between elements in the set.

3.1 A weighted average method

It is not acceptable to consider the influence of each structure of reconvergent fan-out as a whole and calculate the signal probability of each gate of the logic circuit.

We propose a weighted average algorithm based on NRFS for the signal probability calculation. In our proposed approach, the signal probability of the reconvergent fan-in is estimated by considering the effect of recent several RFOs, namely the NRFS of the RFI. The proposed method, developed to implement the idea as indicated earlier in this paper, consists of the following main details.

Algorithm 3 The weighted average algorithm with the reconvergent fan-in

Input: A logic circuit;

Output: An estimation of the signal probability of each lead in the logic circuit.

Step 1 Parse circuit and initialize the related parameters.

1.1 Compile the circuit and organize it into levels. Then determine the order in which the leads of the circuit

are to be processed.

1.2 Assign signal probabilities of 1/2 to all the PIs and set the value of gate error rate ε. Add the RFO to the reconvergent fan-out set, namely RFOS, at once.

Step 2 Find the FRFI of each RFO of RFOS, and mark the FRFI, then add this RFO to the NRFS of the FRFI.

Step 3 Compute the SP for each lead from the PIs to the POs in the circuit.

3.1 Traverse the circuit, if it reaches the end of the circuit, then go to step 4; else go to 3.2;

3.2 Extract the i-th lead (denoted as g_i) from the circuit, if g_i is FRFI, then go to 3.4; else go to 3.3;

3.3 Compute the SP of g_i using the formulas in Tab. 1 and Eq. (1), then go to 3.6;

3.4 For each element of NRFS of g_i ($A_{i,1}$, $A_{i,2}$, $A_{i,3}$, $\cdots$, $A_{i,m}$), calculate the relative signal probability $S_{A_{i,j}}$ ($1 \leqslant j \leqslant m$) with Algorithm 2;

3.5 Compute the weighted average signal probability $S_{w,i}$ of g_i with Eqs. (3) and (4), then make the SP of g_i equal $S_{w,i}$;

3.6 Perform $i = i + 1$ and go to 3.1.

Step 4 End the algorithm.

From the above, the circuit is traversed once in Step 1 of Algorithm 3, then the basic information (lead) of the logic circuit is extracted and the related parameters are initialized. Therefore, the time complexity of Step 1 can be $O(L)$. In Step 1, the main information that needs to be stored is the lead information of the circuit, the information of the RFOs and other intermediate variables, so that the space complexity of Step 1 is $O(L + F_O + c)$. For each RFO, the circuit is traversed from the location of the RFO and the FRFI of the RFO in Step 2 is found, so the time complexity is less than or equal to $O(LF_O)$. In addition, in the process of computing, for each of the FRFI needs, the information of its corresponding RFOs is stored. Therefore, the space complexity of Step 2 is $O(F_O)$. Step 3 is the signal probability calculation of the lead. For the FRFI, the lead, which is in the path from the NRFS of the FRFI to the FRFI, is calculated twice. For other leads, the SP can be computed by Eq. (1) and the formulas in Tab. 1. Therefore, the time complexity of Step 3 is less than or equal to $O(2LF_O + L - F_I)$. In the analysis, the total time-space complexity of Algorithm 3 is less than or equal to $O((3F_O + 2)L - F_I)$ and $O(gn + 2F_O + c)$, respectively, where L is the number of leads; F_O is the number of RFOs; F_I is the number of FRFIs; and c is a constant. In other words, from PIs to POs, Algorithm 3 is always calculated in each lead in units of basic gates. In addition, since F_I and F_O are far smaller than L, the time and space complexities of Algorithm 3 have approximate linear growth with the number of leads.

In Algorithm 3, it is a critical step to make sure that the FRFI can be found quickly and accurately. Therefore, we select one RFO that is only selected once and find the corresponding FRFI. In order to illustrate the process, we take the circuit of Fig. 6 as an example. First, identify the RFOs (B, C) while compiling the circuit. Then, find the corresponding FRFI from these RFOs, and G is the FRFI of B and H is the FRFI of C. Finally, correct the SP of the lead which depends on RFIs. Therefore, we should quickly mark the positions of the RFOs and the corresponding FRFI before correcting the signal probability. It will avoid unnecessary computation and improve the efficiency of execution.

Nevertheless, for each lead which depends on RFOs (such as E, F, G and H in Fig. 6), the IWAA will execute this step of finding the MRFS while the SP of this lead is calculated. Compared with the IWAA, Algorithm 3 avoids repeated judgment and greatly reduces the processing time.

3.2 A strategy correction method

Moreover, there are some distinct deviations in the signal probability calculation of the FRFIs using Algorithm 3. The reason is that there is a correlation between the input signals of FRFIs. Therefore, for each RFI in a circuit, we should correct these inaccuracies in addition to using the weighted average approach.

Nevertheless, during signal transmission, the signal of fan-out branches from the same RFOs may constantly converge or branch which results in the signal correlation accumulation and increases the computing complexity. Besides, for lead S, not only the effect of the RFOs in the NRFS of S but also that of the input signals of S is crucial. Also, other RFOs on which S depends have certain impact on the signal probability of S.

Therefore, the estimated value obtained by the weighted average approach is still imprecise and should be corrected, if there are other FRFIs in the path from the FRFI to its corresponding NRFS, such as the two examples shown in Fig. 5 and Fig. 6; or if the correlation of the input signals of the RFI is complex, such as the example shown in Fig. 5. Some correction terms are introduced into the equation based on the weighted average approach.

The signal probability of lead S estimation formula is as follows:

$$s_S = \begin{cases} S_u + \beta & \text{if } |\beta| \leqslant 0.1S_u,\ S_u + \beta \leqslant 1 \\ S_u & \text{otherwise} \end{cases} \tag{5}$$

where

$$S_u = \begin{cases} S_w & |S_w - S_1| > 0.1S_w \\ S'_w & \text{otherwise} \end{cases} \tag{6}$$

$$\beta = \partial s' s_{\min} s_\alpha \tag{7}$$

where S_u is the estimated signal probability; S'_w is a weighted average of S_w and S_1. For the signal probabilities S_w,

S_1 and s_i (s_i is the initial signal probability without considering the effect of RFOs), in most cases, S_w has the highest accuracy, so $S_u = S_w$. However, in the case of $|S_w - S_1| \leqslant 0.1S_w$, that is $S_u = S'_w$. β is the correction term which can make a few modifications to the influence from NRFS and the correlation of the input signal of S; ∂ is the symbol item, of which the value is 0, 1 or -1; s' is the product of the signal probability of the elements in NRFS of S; s_{min} is the minimum element of a set which is made up of the input signal probabilities of S and the absolute values for the difference between the input signal probabilities and 1; s_α is one of signal probabilities of all input signals or the average value of signal probabilities of some input signals. Furthermore, the selection principle of input signals is to minimize parameter θ ($\theta = |1 - s'/s_S|$).

As shown in Tab. 2, the value of ∂ is determined by S_1, S_w and s. If $S_1 + S_w - 2s' > 0$, the exact signal probability of S is likely to be higher than the three signal probabilities, so we can slightly modify S_u and make it larger. When $S_1 + S_w - 2s' < 0$, we do the opposite of what we do for S_u. However, if $S_1 + S_w - 2s = 0$, we cannot determine the relationship between the exact signal probability and the three signal probabilities, so we do not carry out any modification for S_u.

Tab. 2 Values of ∂ for the difference among S_1, S_w and s' of FRFI

$S_1 + S_w - 2s'$	Value of ∂
>0	1
<0	-1
$=0$	0

Since the signal probability of FRFIs may be affected by other FRFIs compared with Algorithm 3, we introduce some correction terms into the weighted average equation of Algorithm 3. The algorithm of the strategic correction method for signal probability estimation based on Algorithm 3 is given below.

Algorithm 4 The hybrid strategy combined with circuit structure for signal probability estimation

Input: A logic circuit;

Output: An estimation of the signal probability of each lead in the logic circuit.

Step 1 Perform Steps 1 and 2 of Algorithm 3.

Step 2 Calculate the initial signal probability s_i of each lead by performing Step 3 of Algorithm 1.

Step 3 Compute the SP for each lead from the PIs to the POs in the circuit.

3.1 Traverse the circuit, if it reaches the end of the circuit, then go to Step 4; otherwise go to 3.2;

3.2 Extract the i-th lead (denoted as g_i) from the circuit, then calculate the probability S_1 of g_i with the formulas in Tab. 1 and Eq. (1), then make the SP of g_i equal S_1;

3.3 If g_i is FRFI, then go to 3.4; otherwise go to 3.5;

3.4 Recalculate the SP of g_i;

3.4.1 For each element of NRFS of g_i ($A_{i,1}$, $A_{i,2}$, $A_{i,3}$, $\cdots$, $A_{i,m}$), calculate the relative signal probability $S_{A_{i,j}}$ ($1 \leqslant j \leqslant m$) using Algorithm 2. If there are other RFIs between the RFOs of NRFS of g_i and g_i, then mark g_i;

3.4.2 Compute the weighted average signal probability $S_{w,i}$ of g_i with Eqs. (3) and (4);

3.4.3 If g_i is marked, then go to 3.4.4; otherwise make the SP of g_i equal $S_{w,i}$, then go to 3.5;

3.4.4 Compute the signal probability s_{g_i} of g_i with Eqs. (5) to (7), then make the SP of g_i equal s_{g_i}.

3.5 Perform $i = i + 1$ and go to 3.1.

Step 4 End the algorithm.

As seen from the above, Step 1 of Algorithm 4 is the Steps 1 and 2 of Algorithm 3. Therefore, the time and space complexities of Step 1 are less than or equal to $O(LF_O + L)$ and $O(L + 2F_O + c)$, respectively. Step 2 is the initial signal probability calculation of the lead. Therefore, the time and space complexities of Step 2 are $O(L)$ and $O(1)$, respectively. Step 3 is the signal probability recalculation of the lead. The SP of each lead is computed again by Eq. (1) and the formulas in Tab. 1. For some FRFIs, Algorithm 4 calculates the signal probability based on the weighted average signal probability. Therefore, the time complexity of Step 3 is less than or equal to $O(2LF_O + L + F_I)$. In addition, there is some information about other RFIs for some RFIFs, so the space complexity of Step 3 is less than or equal to $O(F_I^2)$. In the analysis, the total time-space complexity of Algorithm 4 is less than or equal to $O((3F_O + 4)L + F_I)$ and less than or equal to $O(L + 2F_O + F_I^2 + c)$, respectively. Therefore, the time and space complexities of Algorithm 4 are slightly larger than those of Algorithm 3.

4 Simulation Results

To verify the effectiveness and applicability of the proposed method, in a computer with Windows Server 2012 Standard system, 2.3 GHz Intel Xeon E312xx (Sandy Bridge) and 8 GB of RAM memory, we chose some ISCAS85 benchmark circuits for the experiment. All the gates are assumed to have the same gate error rate ε and gates fail each other independently.

First, by comparing with the IWAA[6], the effectiveness of the algorithms proposed in this paper is tested when the gate error rate $\varepsilon = 0$, and the results are shown in Tab. 3. Then, experiments are performed on Algorithms 3 and 4 for different values of ε. The comparison results of the IWAA[7] are shown in Tab. 4. Furthermore, considering that the IWAA[6] can also be used to calculate the SP for the circuit with a gate error rate by using Eq. (1), we conduct some experiments based on Algorithm 3, Algorithm 4 and the IWAA[6], respectively. Simula-

tion results are shown in Figs. 9 and 10.

In these experiments, the signal probability of the PIs is 0.5. And each fan-out branch is treated as a gate and has the same gate error rate as other gates. In order to measure the quality of our results, we adopt the mean percentage error (MPE) as the standard.

For the MC, faults are injected into the circuit in pseudo-random mode and the approximation of the signal probability is obtained by counting the ratio of the output signal which is logical "1". However, for the larger circuit, the time consumption of the MC method with exhaustive failure injection will be difficult to accept. Furthermore, in a small circuit, the loss of precision for the MC is larger[18]. Therefore, in order to obtain a good experimental reference object, for the small-scale circuit of c17, the MC simulation runs more than 10^7 times. For other benchmark circuits, the times of MC simulation is 10^6.

Tab. 3 shows the evaluation results for some ISCAS85 benchmark circuits with the gate error rate $\varepsilon = 0$. The first column is the circuit name, the second column gives the MPE of signal probabilities of POs in our proposed two algorithms (Algorithms 3 and 4) and the IWAA[6]. Tab. 4 shows the simulation results of Algorithm 3, Algorithm 4 and the IWAA[7] with different ε used for comparison.

Tab. 3 Comparison of the results obtained by different methods ($\varepsilon = 0$)

Circuit	MPE/%		
	Algorithm 3	Algorithm 4	IWAA[6]
C17	0	0	0
C432	20.292 1	20.455 2	20.199 6
C499	0	0	0
C880	2.418 4	2.003 3	2.456 2
C1355	0.293 5	0.502 2	0.265 9
C1908	3.104 8	2.653 8	3.109 4
C2670	11.025 1	9.963 6	12.867 0
C3540	32.782 7	32.630 2	32.843 7
C5315	13.097 9	12.805 5	12.972 3
C6288	12.633 3	12.291 9	12.633 1
C7552	2.979 2	2.927 6	3.055 2
Average	8.966 1	8.748 5	9.128 6

Tab. 4 Comparison of the MPE obtained from Algorithm 3, Algorithm 4 and IWAA[7] for different ε

Circuit	ε = 0.001			ε = 0.01			ε = 0.1		
	Algorithm 3	Algorithm 4	IWAA[7]	Algorithm 3	Algorithm 4	IWAA[7]	Algorithm 3	Algorithm 4	IWAA[7]
C499	0	0	5.3	0	0	25.0	0	0	26.69
C1355	4.35	1.08	4.5	1.63	5.52	22.3	2.62	2.65	26.50
C1908	2.97	2.54	1.4	2.46	2.17	8.6	1.17	0.99	9.38
C2670	12.57	11.95	0.9	6.17	5.91	6.0	0.74	0.75	11.45
C3540	31.85	31.68	2.2	27.01	27.00	16.1	3.69	5.15	18.97
Average	10.34	9.45	2.9	7.45	8.12	15.6	1.64	1.91	18.60

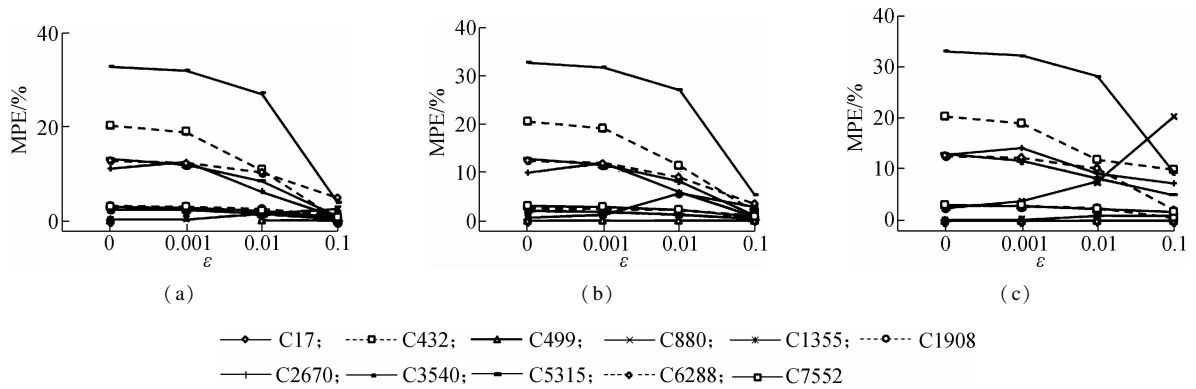

Fig. 9 MPE vs. gate error ε. (a) For Algorithm 3; (b) For Algorithm 4; (c) For the novel IWAA

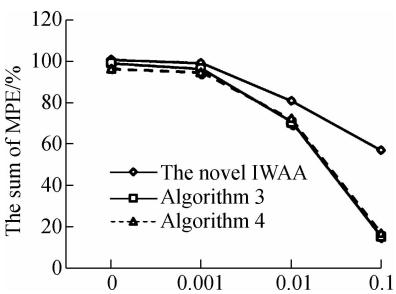

Fig. 10 Sum of MPE vs. gate error ε for ISCAS85 benchmarks

Tab. 3 reveals that Algorithm 3 and Algorithm 4 have higher accuracy than the approach of IWAA[6] in general. For the MPE, Algorithm 3 has 1.8% improvement and Algorithm 4 has 4.2% improvement relative to the IWWA[6]. In Tab. 4, Algorithm 3 and Algorithm 4 are more accurate than the IWWA[7] when the gate error rate ε is greater than 0.01. It demonstrates that when taking the effect of the NRFS of Algorithm 3 and using the mixed-calculation strategy of Algorithm 4, the accuracy of the proposed approaches is improved when $\varepsilon < 0.01$.

However, the MPE of C432 and C3540 for these three approaches are higher in Tab. 3, which may be caused by

the structure of the circuit. The simulation results of C17 and C499 indicate that the proposed approach can calculate the exact signal probabilities for the circuit with fan-out free or with the coupling relationship of RFOs.

Tab. 5 shows the runtime and the memory requirement of the proposed approaches and the IWAA[6] for the ISCAS85 benchmark circuits with 50 experiments and a gate error rate $\varepsilon = 0$. The first column is the circuit name, the second column is the number of leads in the circuit, the third column is the number of RFOs in the circuit, and the fourth column gives the average cost of different methods. Since the IWAA[7] is based on the correlation coefficient method (CCM)[4] and has higher computational complexity than the IWAA in Ref. [6], the runtime and the memory requirement of the IWAA in Ref. [7] are not given to compare with this proposed approach.

Tab. 5 reveals that the runtime of Algorithm 3 and Algorithm 4 are much shorter than the IWAA[6], which indicates that our proposed approaches have significant advantages in dealing with large circuits. In most circuits, compared with the IWAA[6], the memory overhead of our approaches are smaller. Previous simulation results indicate that the average speed of our proposed methods is 256× faster than the IWAA[6] and their memory requirements are smaller. The mean accuracy of Algorithm 4 is improved to a certain extent compared with the IWAA[6-7].

In the IWAA[6], the signal probability calculation does not take into account the gate error rate. Therefore, if the circuit is not fault-free, the signal probability can be calculated by the novel IWAA which is based on the IWAA proposed in Ref. [6] and considers the signal probability of the gate calculated by Eq. (1). In order to verify the applicability of the proposed approaches, we conduct the experiment using the novel IWAA and the proposed approaches under the gate error rate of 0.001, 0.01 and 0.1, respectively. The simulation results are shown in Fig. 9 and 10.

Tab. 5 Comparison of the average time and space consumptions for different methods ($\varepsilon = 0$)

Circuit	Number of Leads	RFOs	Runtime/s			Memory/MB		
			Algorithm 3	Algorithm 4	IWAA[6]	Algorithm 3	Algorithm 4	IWAA[6]
C17	17	2	0.015	0.015	0.016	1.003	1.003	1.003
C432	432	89	0.044	0.047	0.177	3.514	3.514	3.513
C499	499	59	0.049	0.053	0.409	4.014	4.014	4.014
C880	880	125	0.064	0.069	0.862	5.018	5.018	6.021
C1355	1 355	259	0.067	0.084	1.539	7.024	7.024	8.029
C1908	1 908	385	0.394	0.397	14.163	14.551	15.053	15.054
C2670	2 670	454	0.281	0.282	16.472	13.548	14.052	16.064
C3540	3 540	579	0.613	0.624	61.388	20.574	20.575	23.088
C5315	5 315	806	1.031	1.042	249.688	23.586	23.663	18.556
C6288	6 288	1 456	0.719	0.745	221.141	12.613	12.913	14.995
C7552	7 552	1 300	2.266	2.277	864.681	20.475	20.998	22.989
Average	2 769	501	0.503 9	0.512 3	130.048 7	11.447 3	11.620 6	12.120 6

Fig. 9 shows the MPE vs. gate error ε for the ISCAS85 benchmark circuits using our proposed approaches and the new IWAA. For the circuits of C17 and C499, these approaches can accurately calculate the signal probability of each lead. Furthermore, such approaches can also be successfully applied to the parts of general circuits that are fan-out free or only have the structures of reconvergent fan-out that are completely independent or independent types. Moreover, the accuracies of Algorithm 3 and Algorithm 4 are much better than that of the novel IWAA when the gate error $\varepsilon = 0.1$.

Fig. 10 compares the sum of MPE for ISCAS85 benchmarks, where a smaller error is observed as the gate error rate ε increases. Moreover, in contrast to the novel IWAA, the results of our proposed methods are better. Therefore, our proposed methods have better applicability. When gate error rate ε is from 0 to 0.01, the results evaluated by Algorithm 4 are the best on the whole.

5 Conclusion

A novel approach based on the IWAA is proposed to calculate the signal probability of the logic circuit. The signal probability for each lead in the circuit is calculated by using a weighted averaging method which attempts to take into account the effect of the NRFS and the gate error rate. In addition, some correction terms are introduced into the weighted averaging equation in order to reduce the influence of the signal correlation. The goals of good scalability, low memory requirements and high computational speed are achieved in the proposed method.

The simulation results reveal that the proposed method has approximate linear time computational complexity in terms of the circuit size and the number of RFOs, and its accuracy is higher than that of the IWAA. Theoretical analysis and experimental results demonstrate that our proposed approach is advantageous in terms of efficiency and is easy to implement.

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一种考虑重汇聚结构的电路信号概率加权平均计算方法

肖 杰 马伟峰 李 伟 施展辉

(浙江工业大学计算机科学与技术学院,杭州 310023)

摘要:通过对电路结构的分析,提出了一种新的基于改进型加权平均算法的超大规模集成电路信号概率估算方法. 在考虑基本门故障概率水平的基础上,首先基于同源信号汇聚原则标识重汇聚扇出源对应的第一重汇聚扇入节点,以定位重要的信号相关性节点.通过敏化通路标识电路中多重汇聚结构的重汇聚扇入节点,以确定信号概率计算干扰源. 然后,结合加权平均思想计算节点的加权信号概率,以修正其信号概率. 最后,通过信号概率混合计算策略量化了扇出重汇聚,以减少多重汇聚对精度的影响. 在 ISCAS85 基准电路上的实验结果表明,所提方法的计算时空开销随基本门数量的增加呈线性增长的趋势,且其精度比改进型加权平均算法提高了 4.2%.

关键词:改进型加权平均算法;信号概率估算;门单元故障率;组合逻辑电路

中图分类号:TP331